WHAT IS CLAIMED IS:

1. An amplifier circuit for carrier aggregation, comprising

a first input node, a second input node, and an output node;

a first current converter and a second current converter, each configured to provide transconductance amplification for a radio-frequency signal received through the respective input node and generate a current representative of the respective amplified radio-frequency signal; and

an adder circuit implemented to combine the respective currents from the first and second current converters and provide an output radio-frequency signal at the output node.

2. The amplifier circuit of claim 1 wherein a first amplification path including the first input node, the first current converter, the adder circuit, and the output node, is free of switches, and a second amplification path including the second input node, the second current converter, the adder circuit, and the output node, is free of switches.

3. The amplifier circuit of claim 1 wherein each of the first current converter and the second current converter includes an amplifying transistor having an input coupled to the respective input node, and an output coupled to the adder circuit.

4. The amplifier circuit of claim 3 wherein the adder circuit includes an amplifying transistor having an input coupled to either or both of the outputs of the respective amplifying transistors of the first and second current converters.

5. The amplifier circuit of claim 4 wherein the amplifying transistor of the adder circuit is a common amplifying transistor having its input coupled to the outputs of the respective amplifying transistors of the first and second current converters.

6. The amplifier circuit of claim 5 wherein the amplifying transistor of the first current converter and the common amplifying transistor of the adder circuit are implemented in a cascode configuration, and the amplifying transistor of the second current converter and the common amplifying transistor of the adder circuit are implemented in a cascode configuration.

7. The amplifier circuit of claim 4 wherein the amplifying transistor of the adder circuit is a separate amplifying transistor having its input coupled to the output of one of the respective amplifying transistors of the first and second current converters, and the adder circuit further includes an additional separate amplifying transistor having an input coupled to the output of the other one of the respective amplifying transistors of the first and second current converters.

8. The amplifier circuit of claim 7 wherein the amplifying transistor of the first current converter and the respective separate amplifying transistor of the adder circuit are implemented in a cascode configuration, and the amplifying transistor of the second current converter and the respective separate amplifying transistor of the adder circuit are implemented in a cascode configuration.

9. The amplifier circuit of claim 4 wherein the each of the amplifying transistor of the first current converter, the amplifying transistor of the second current converter, and the amplifying transistor of the adder circuit is implemented as a bipolar-junction transistor having a base, an emitter, and a collector.

10. The amplifier circuit of claim 9 wherein the base is the input, and the collector is the output, of the amplifying transistor of each of the first and second current converters.

11. The amplifier circuit of claim 10 wherein the emitter is the input, and the collector is the output, of the amplifying transistor of the adder circuit.

12. The amplifier circuit of claim 9 wherein each of the first and second current converters includes a switchable biasing path configured to provide a bias signal to the base of the respective amplifying transistor.

13. The amplifier circuit of claim 12 wherein the switchable biasing path is configured to be enabled or disabled to enable or disable the respective amplifying transistor.

14. The amplifier circuit of claim 13 wherein the switchable biasing paths of the first and second current converters are configured to enable both of the respective amplifying transistors in a carrier aggregation mode, and to enable one and disable the other of the respective amplifying transistors in a non-carrier aggregation mode.

15. A radio-frequency module comprising:

a packaging substrate configured to receive a plurality of components; and

an amplifier circuit implemented on the packaging substrate and configured to support carrier aggregation, the amplifier circuit including a first input node, a second input node, and an output node, the amplifier circuit further including a first current converter and a second current converter, each configured to provide transconductance amplification for a radio-frequency signal received through the respective input node and generate a current representative of the respective amplified radio-frequency signal, the amplifier circuit further including an adder circuit implemented to combine the respective currents from the first and second current converters and provide an output radio-frequency signal at the output node.

16. The radio-frequency module of claim 15 further comprising a first filter having an output coupled to the first input node, and a second filter having an output coupled to the second input node.

17. The radio-frequency module of claim 16 wherein each of the first and second filters includes an input, the inputs of the first and second filters coupled to a common signal input node.

18. A wireless device comprising:

an antenna; and

an radio-frequency module in communication with the antenna and including an amplifier circuit configured to support carrier aggregation, the amplifier circuit including a first input node, a second input node, and an output node, the amplifier circuit further including a first current converter and a second current converter, each configured to provide transconductance amplification for a radio-frequency signal received through the respective input node and generate a current representative of the respective amplified radio-frequency signal, the amplifier circuit further including an adder circuit implemented to combine the respective currents from the first and second current converters and provide an output radio-frequency signal at the output node.

19. The wireless device of claim 18 wherein the amplifier circuit is configured to support carrier aggregation involving first and second cellular bands.

20. The wireless device of claim 19 wherein the antenna is a diversity antenna, and the first and second cellular bands include first and second cellular receive bands.