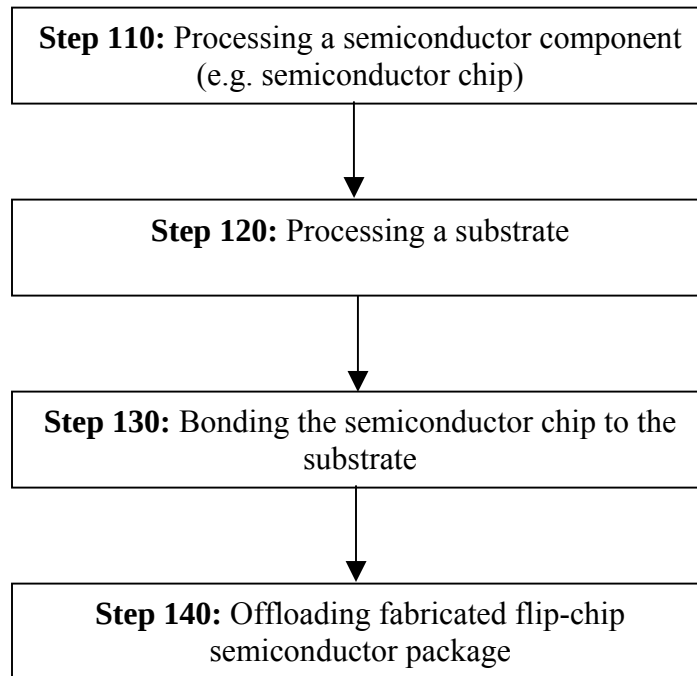


**FIG. 1**

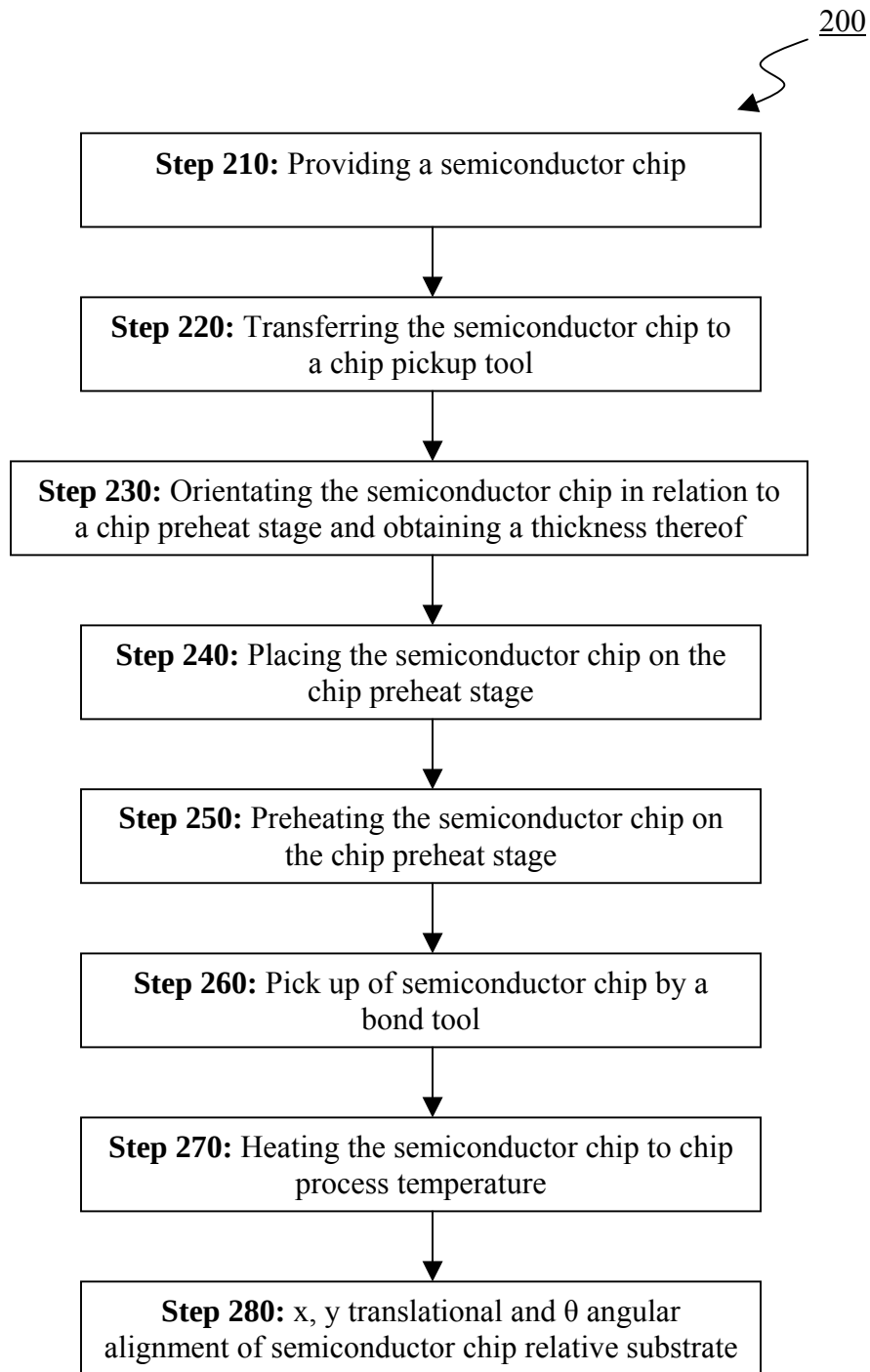
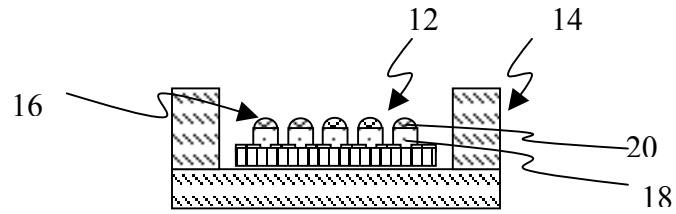
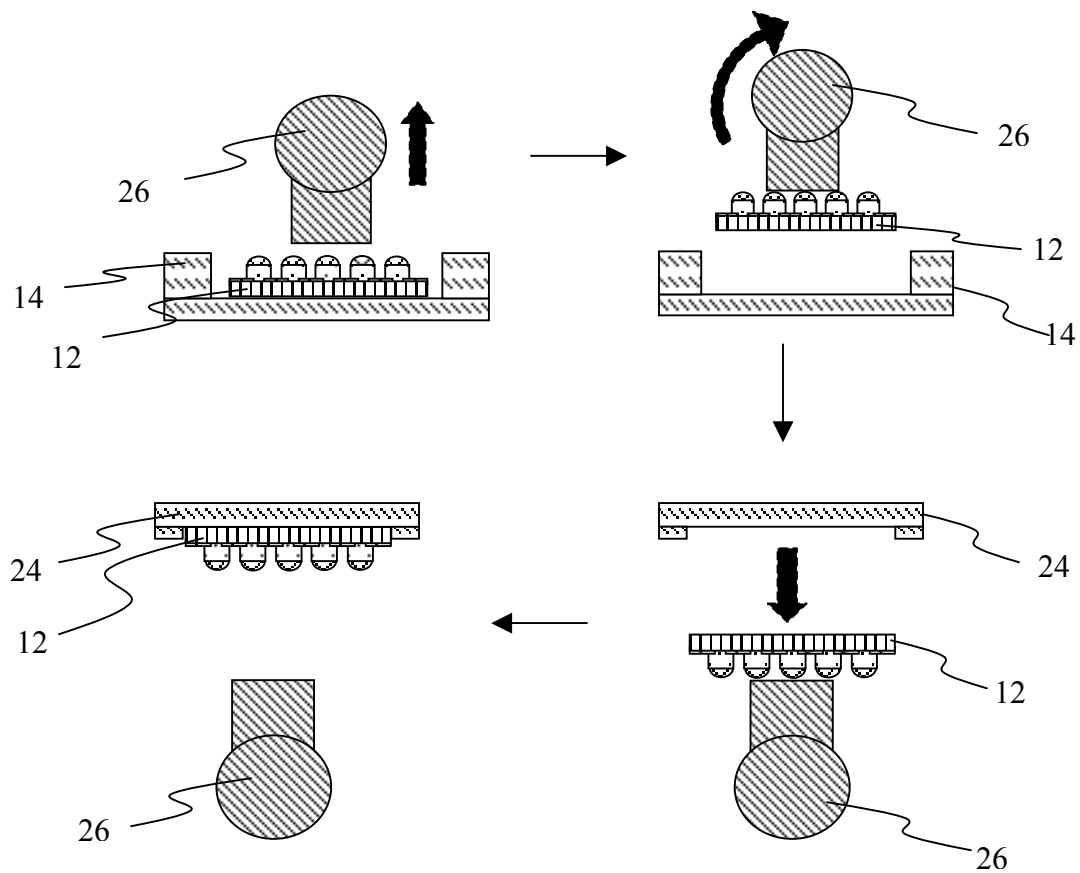
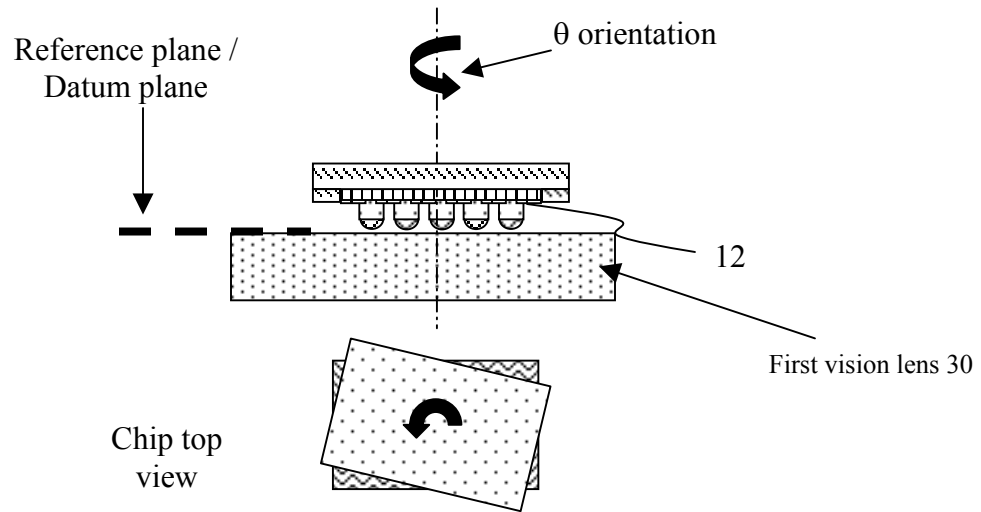
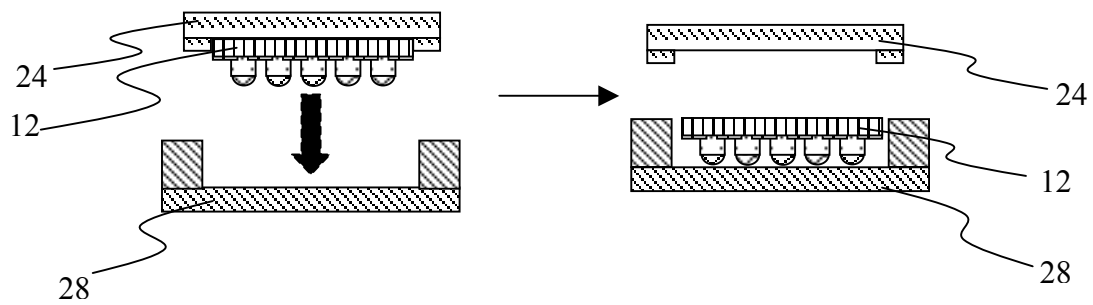
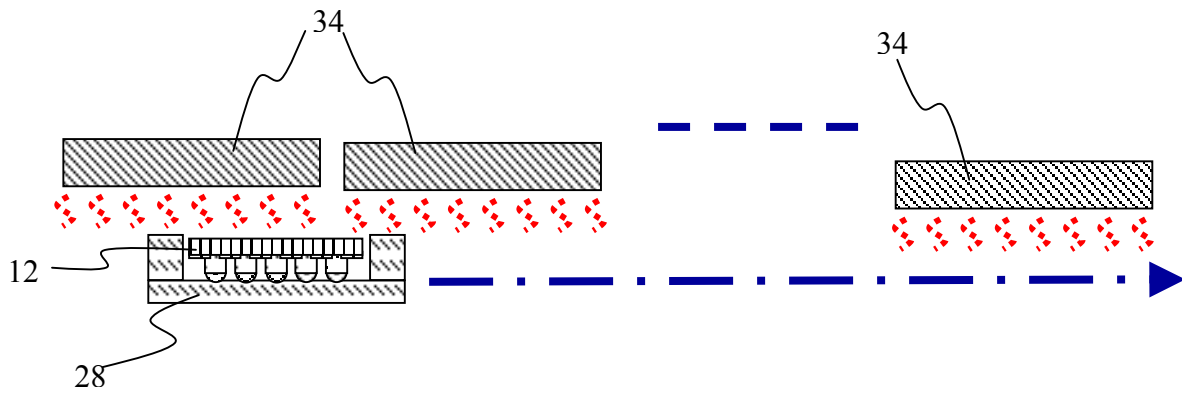
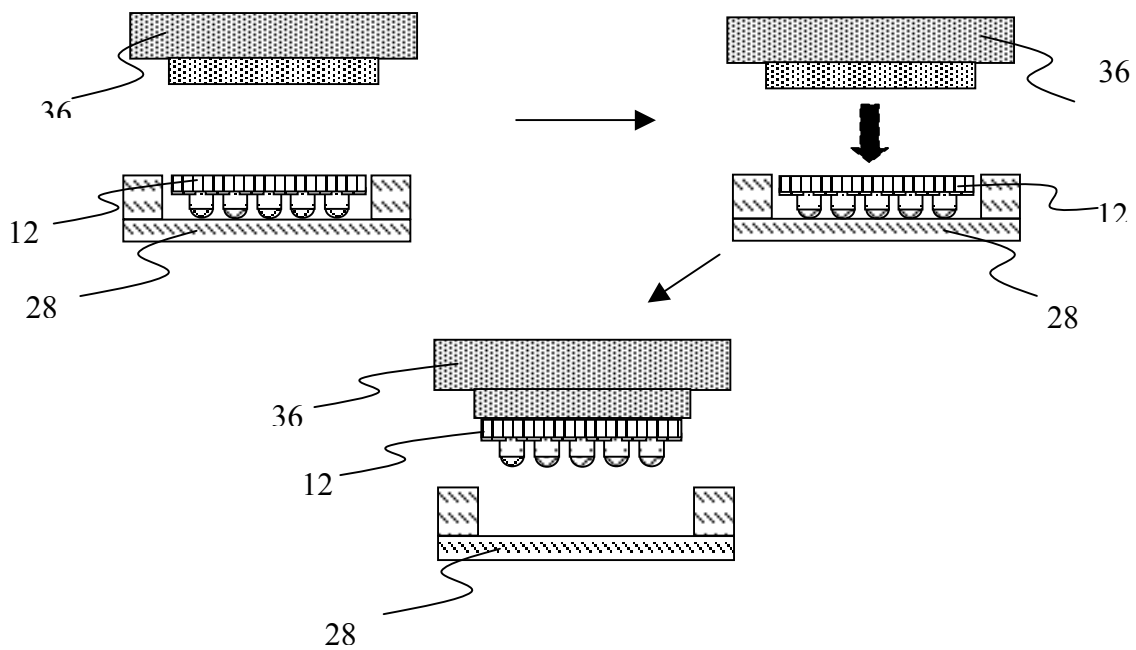


FIG. 2

Step 210: Providing a semiconductor chip**FIG. 3a.**Step 220: Transferring semiconductor chip from chip tray to chip pickup tool**FIG. 3b**

Step 230: Orientating and positioning semiconductor chip**FIG. 3c**Step 240: Placing semiconductor chip on chip preheat stage**FIG. 3d**

Step 250: Preheating semiconductor chip**FIG. 3e**Step 260: Picking up of semiconductor chip by bond tool**FIG. 3f**

Step 270: Heating of semiconductor chip to bonding temperature

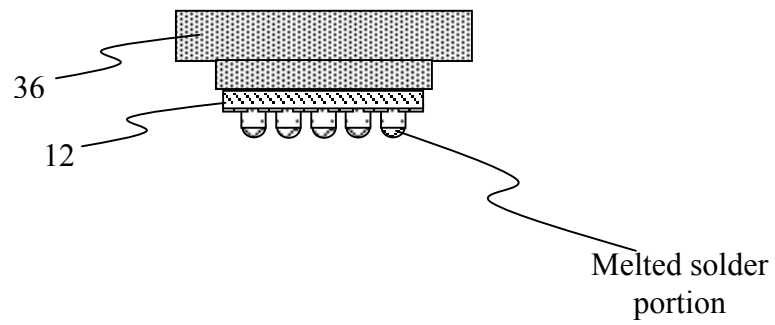


FIG. 3g

Step 280: Positioning of semiconductor chip to bonding temperature

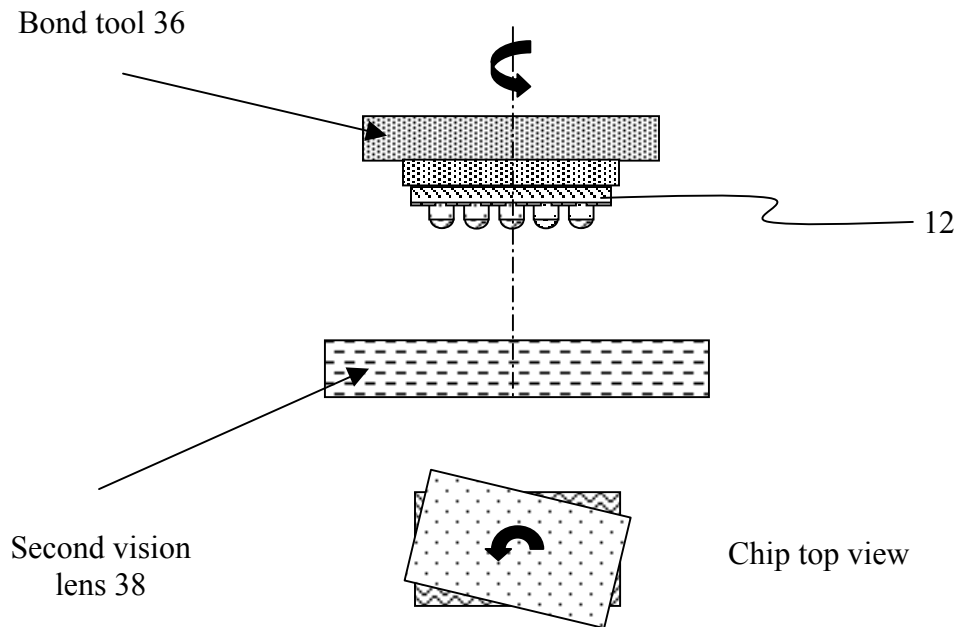
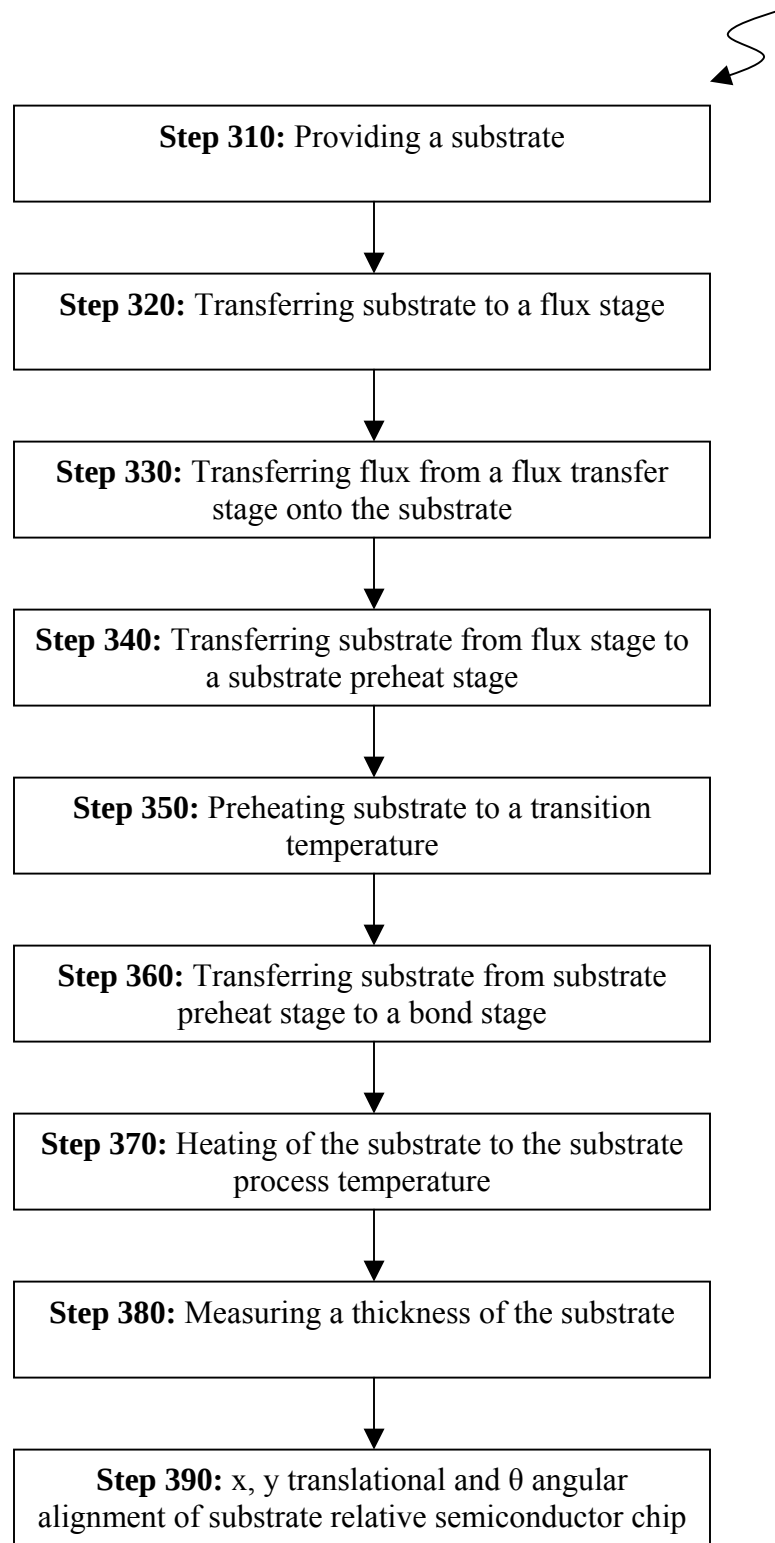


FIG. 3h

**FIG. 4**

Step 310: Providing the substrate

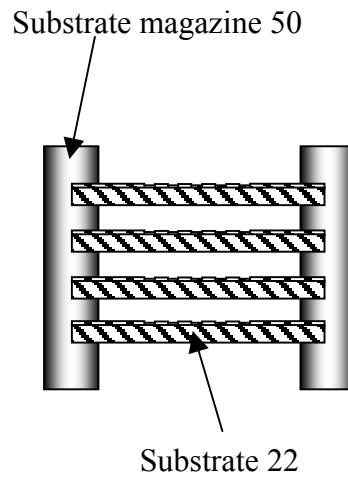


FIG. 5a

Step 320: Transferring substrate to flux stage

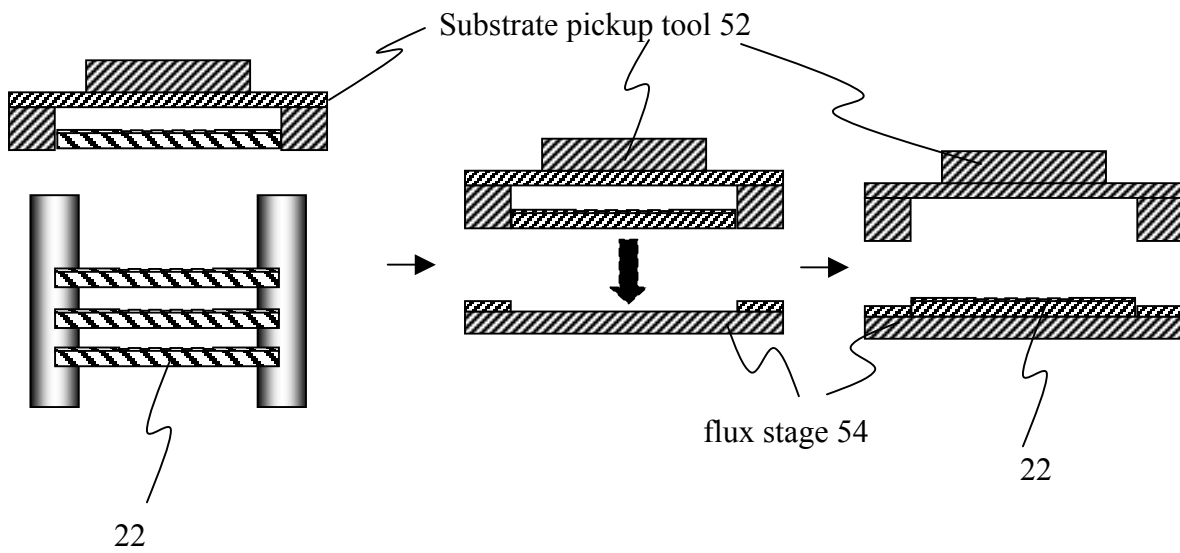


FIG. 5b

Step 330: Transferring flux onto surface of substrate

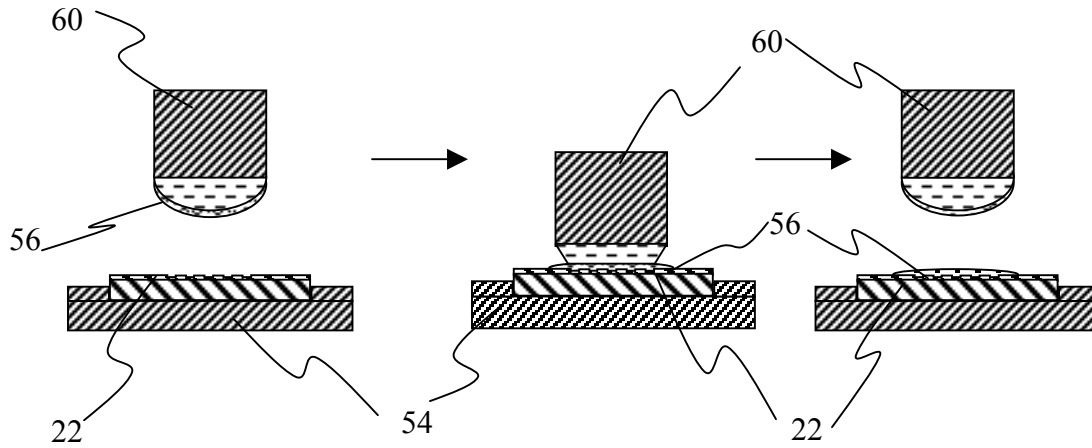


FIG. 5c

Step 340: Transferring substrate to substrate preheat stage

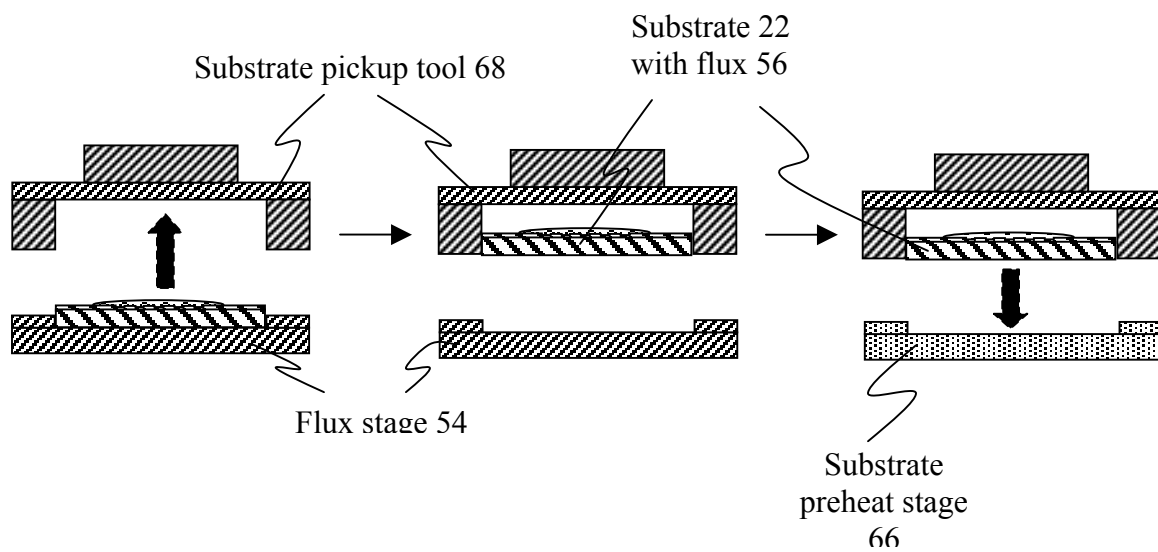
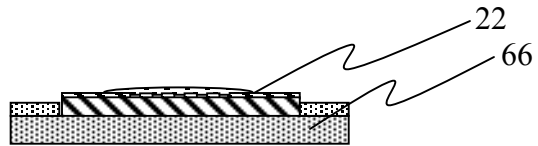


FIG. 5d

Step 350: Heating substrate to transition temperature



Transition
temperature

FIG. 5e

Step 360: Transferring substrate from substrate preheat stage to bond stage

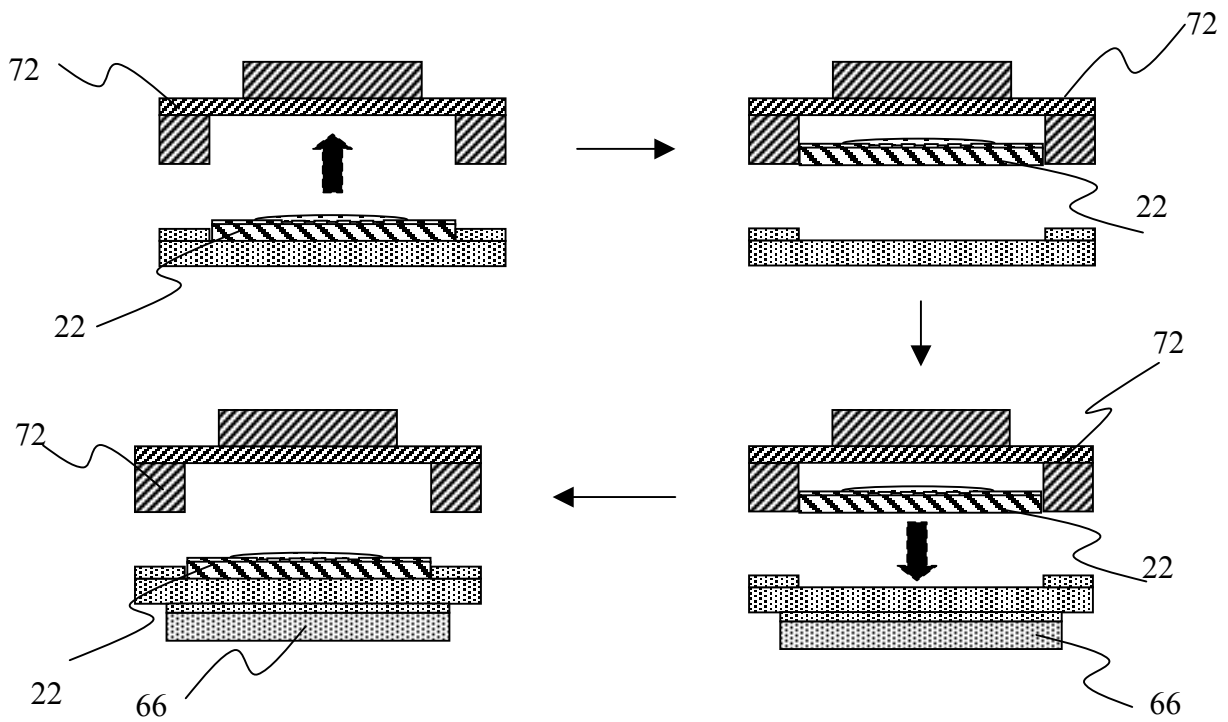


FIG. 5f

Step 370: Heating substrate to second bonding temperature

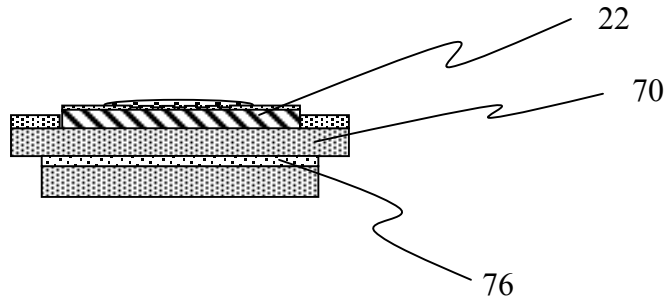


FIG. 5g

Step 380: Measuring thickness of the substrate

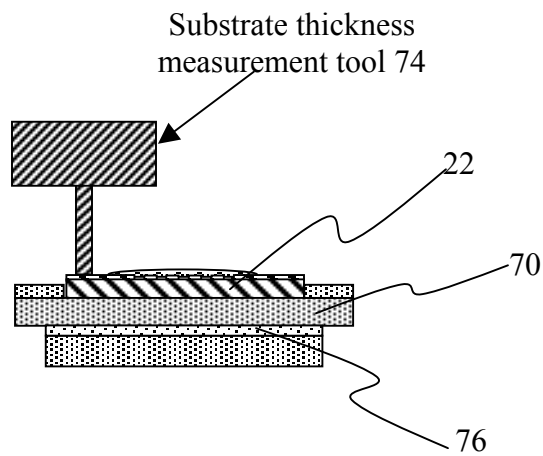


FIG. 5h

Step 390: Positioning of the substrate below second vision lens

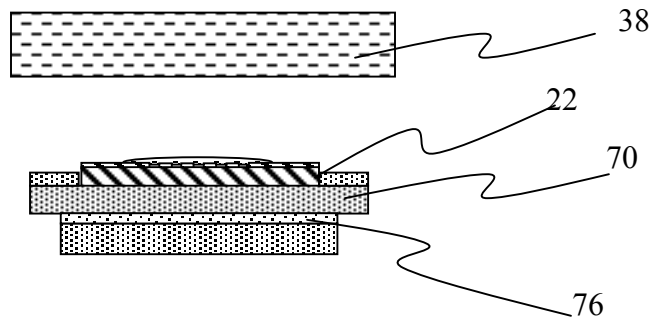
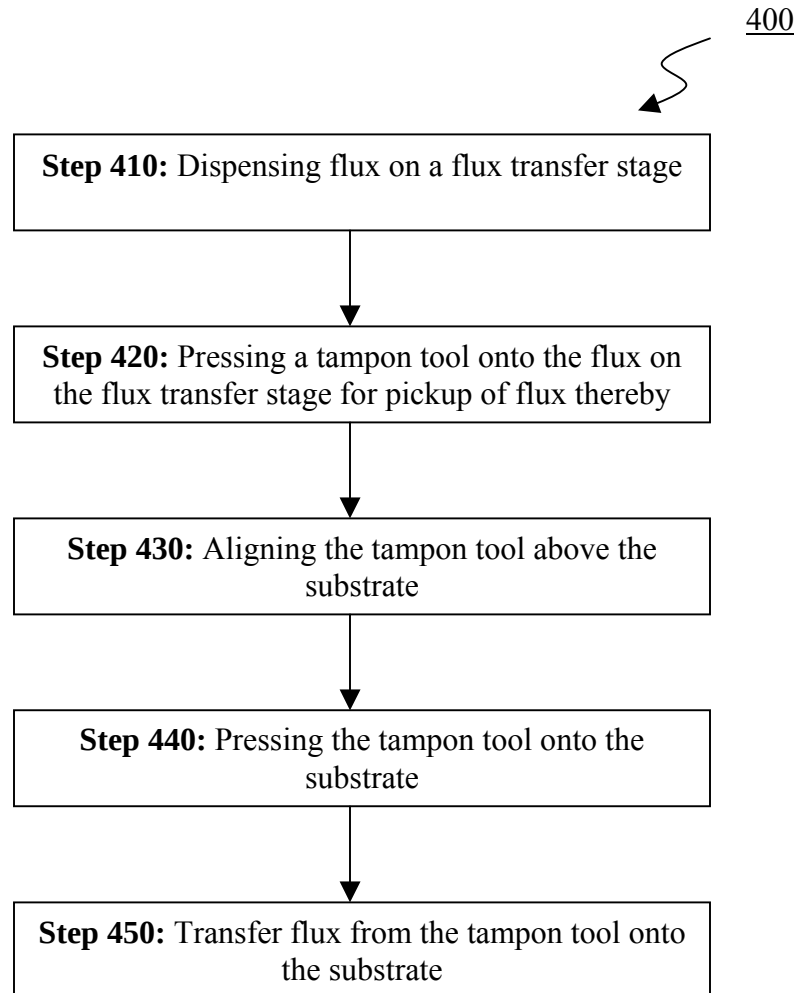


FIG. 5i

**FIG. 6**

Step 410: Dispensing Flux onto flux transfer stage

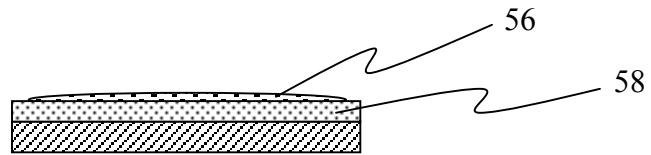


FIG 7a

Step 420: Pressing tampon tool onto flux for pickup flux thereby

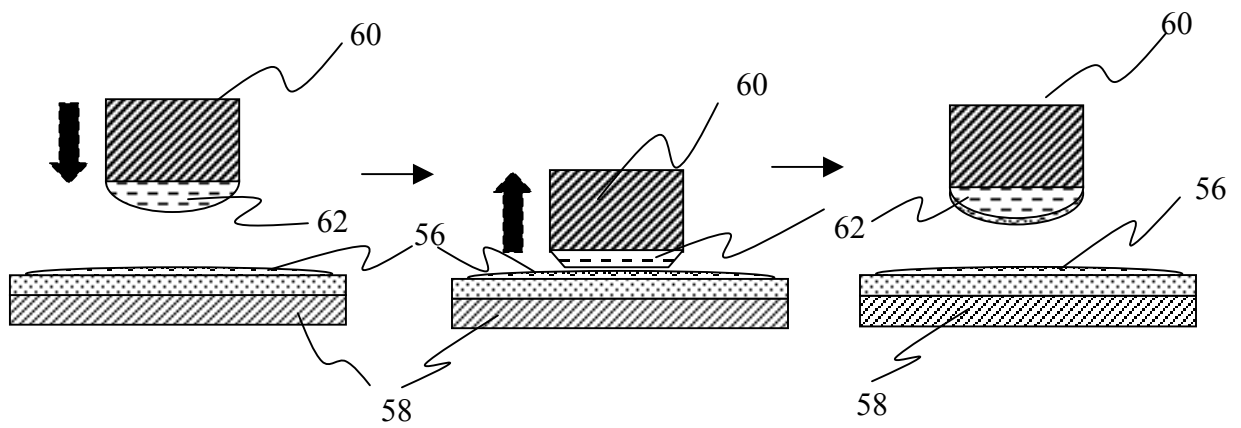


FIG. 7b

Step 430: Aligning tampon tool above the substrate

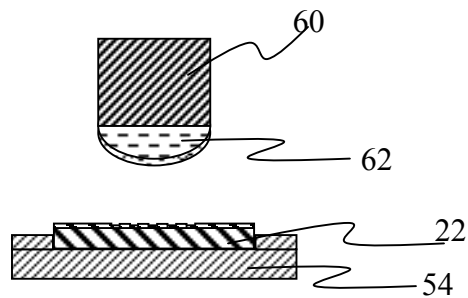


FIG. 7c

Step 440: Pressing the tampon tool onto surface of substrate

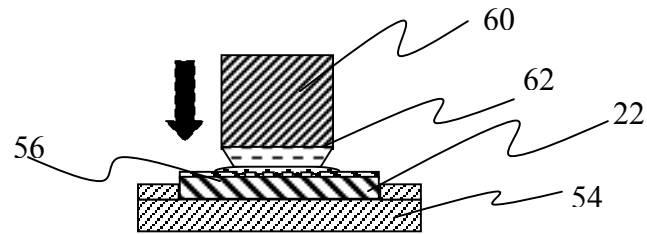


FIG. 7d

Step 450: Transfer of flux from tampon tool to the surface of the substrate

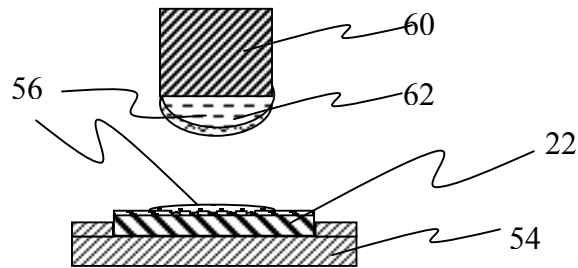
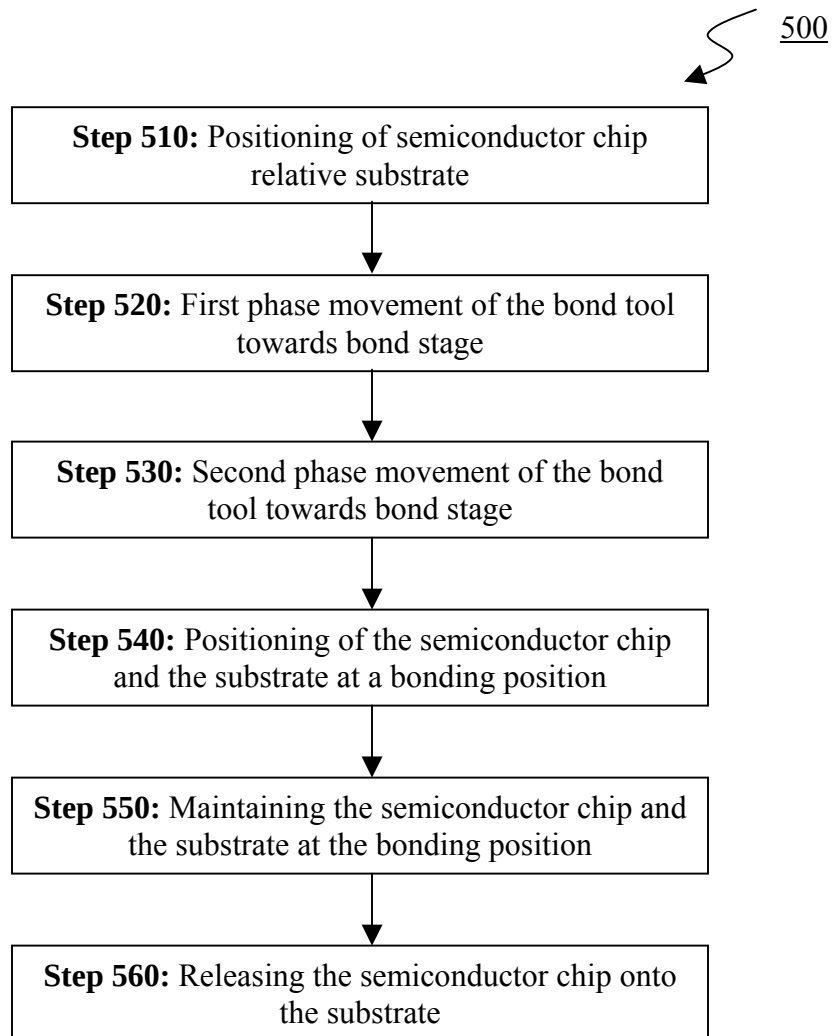


FIG. 7e

**FIG. 8**

Step 510: Positioning of semiconductor chip relative substrate

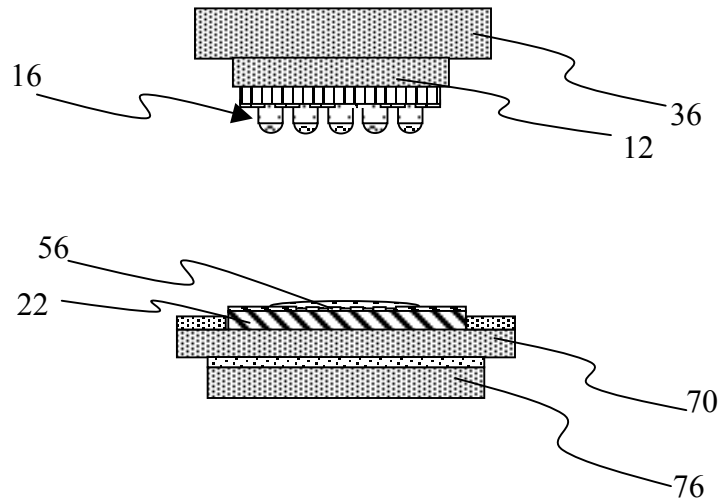


Fig. 9a

Steps 520 and 530: First and second phase movement of the bond tool

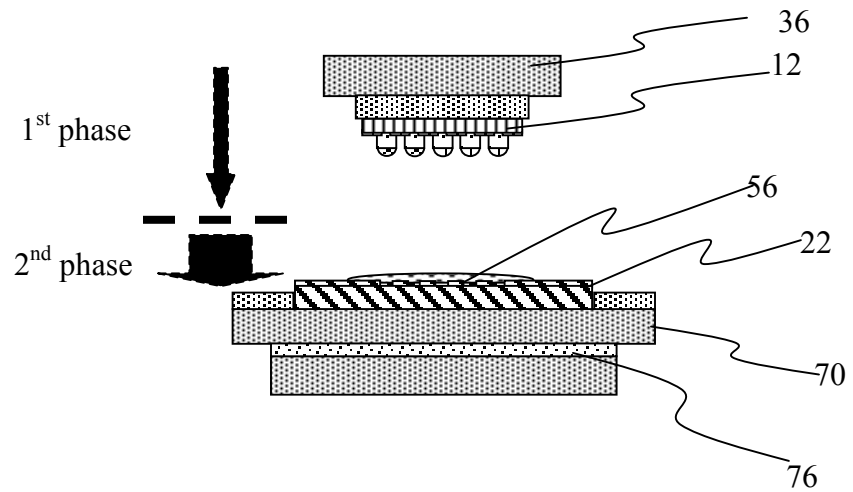


FIG. 9b

Steps 540 and 550: Positioning and maintaining the semiconductor chip and the substrate at a bonding position

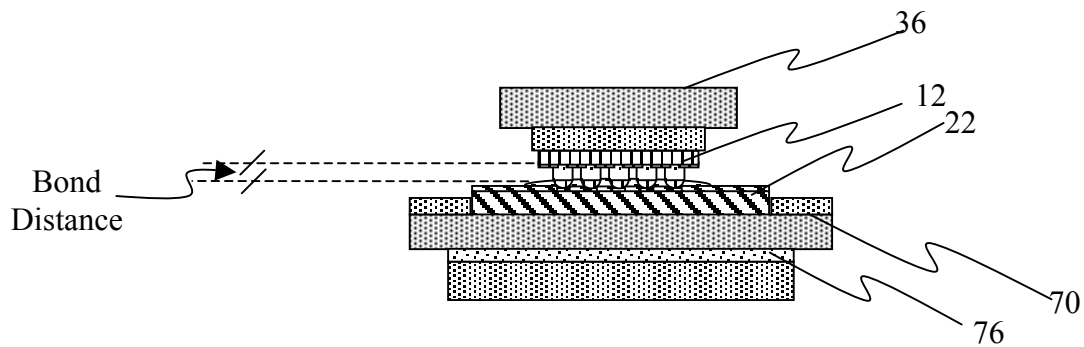


FIG. 9c

Steps 560: Releasing the semiconductor chip onto the substrate

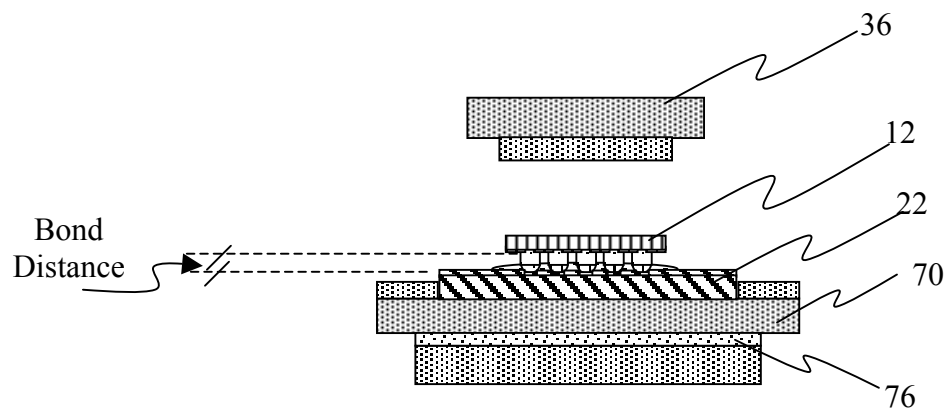
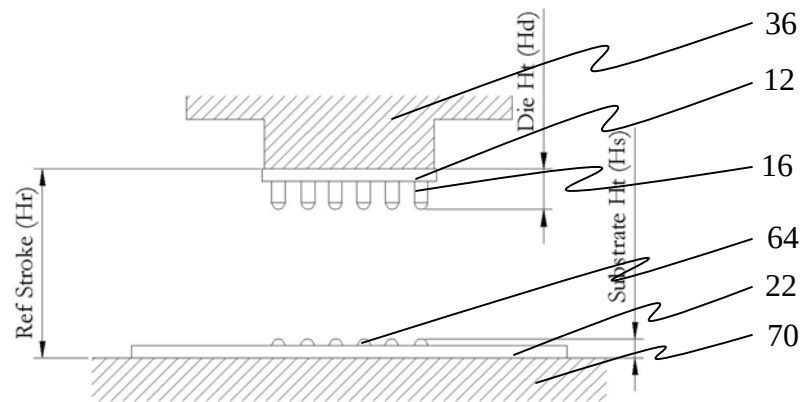


FIG. 9d



$$\text{Actual Stroke} = H_r - H_s - H_d + \text{Compression offset}^*$$

**Compression offset is to overcome any co-planarity variances from the Die and the Substrate*

FIG. 10

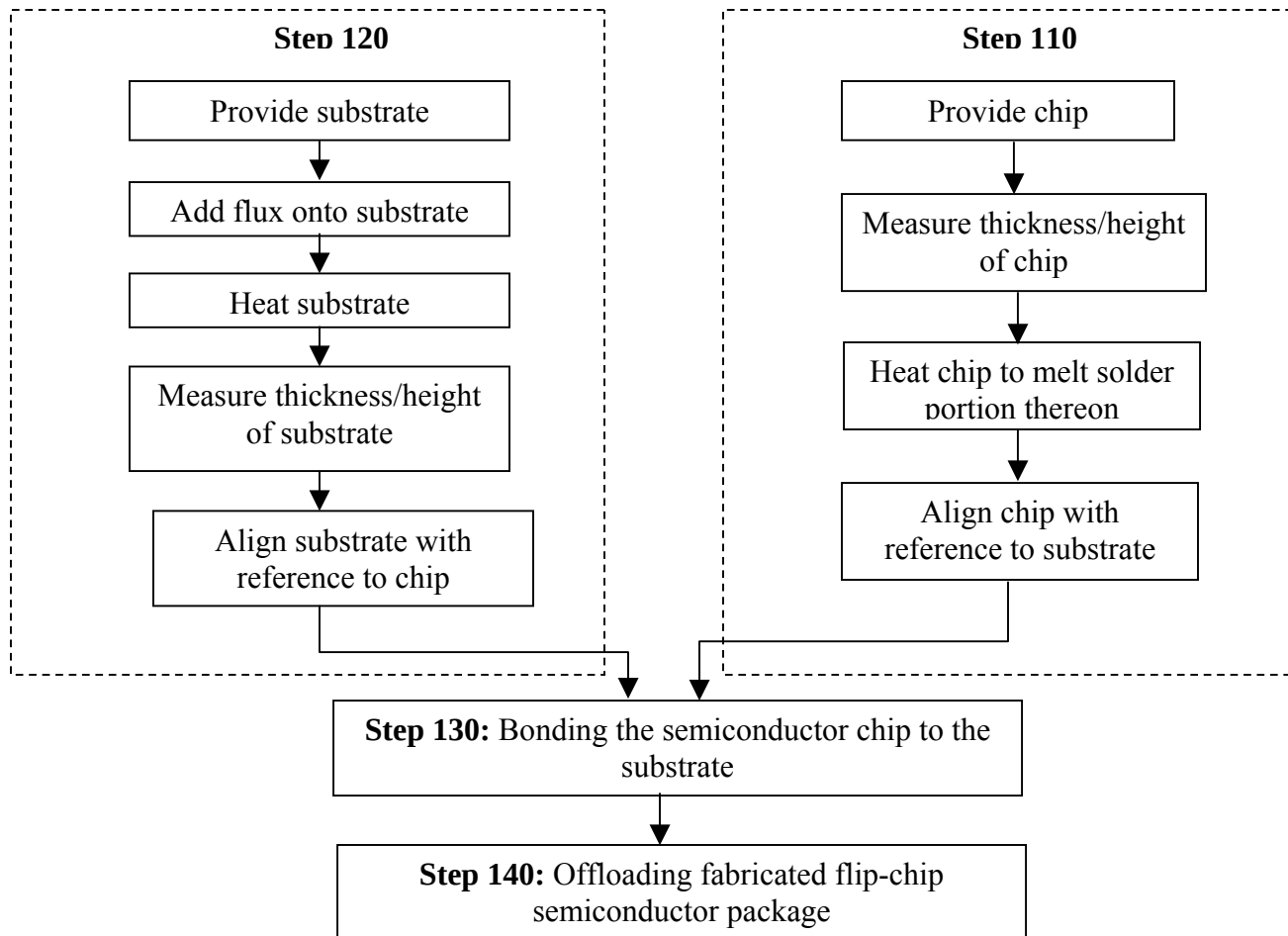


FIG. 11

Temperature Profile During Method 100

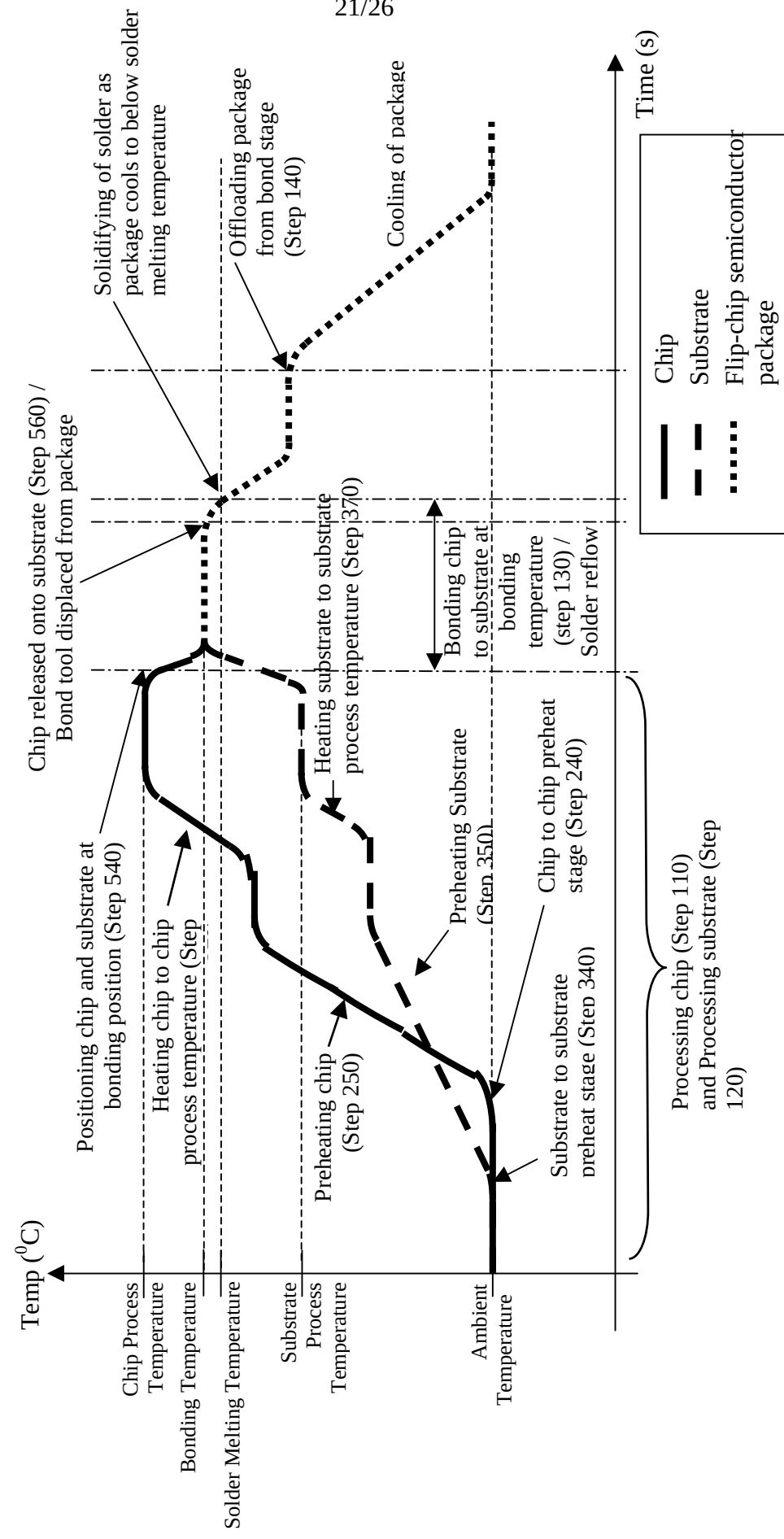


FIG. 12

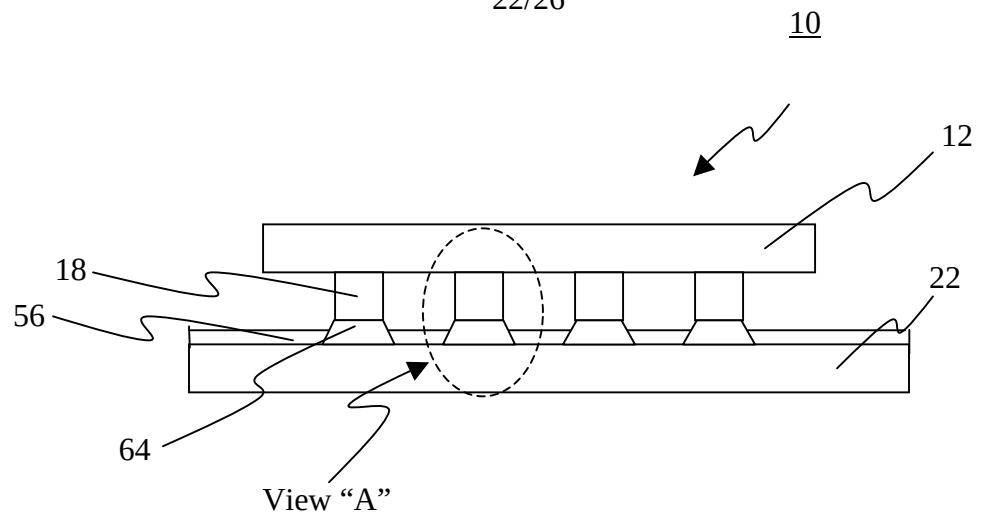


FIG. 13

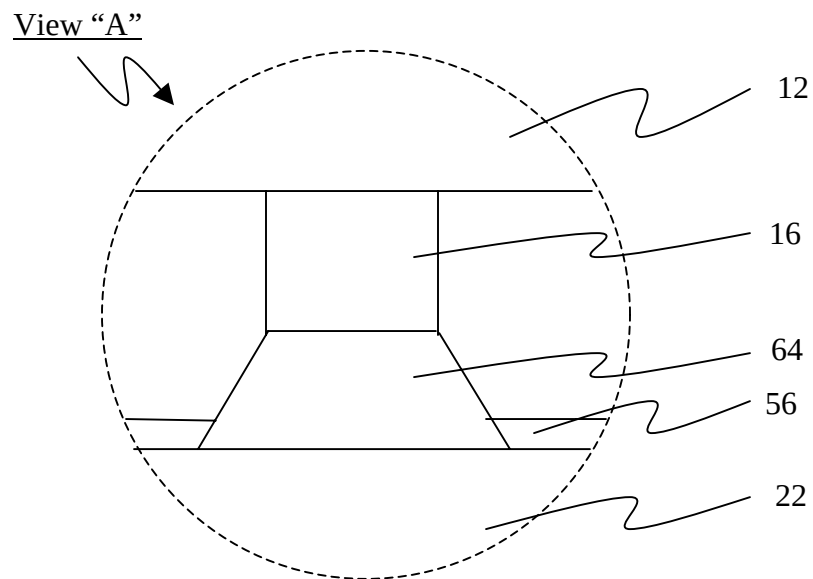


FIG. 14

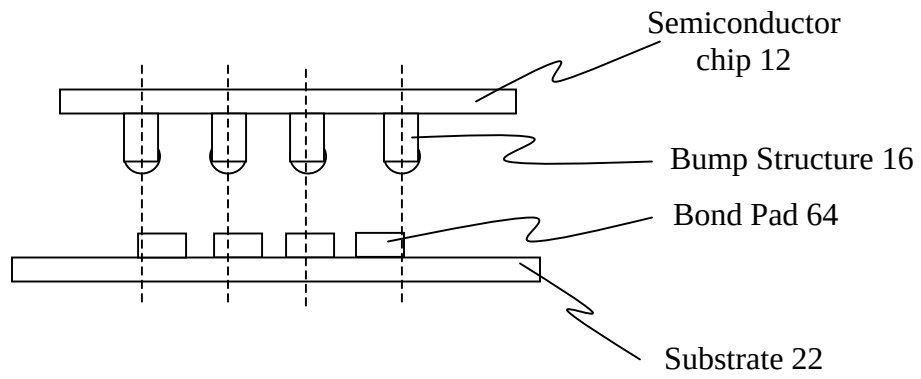


FIG. 15a

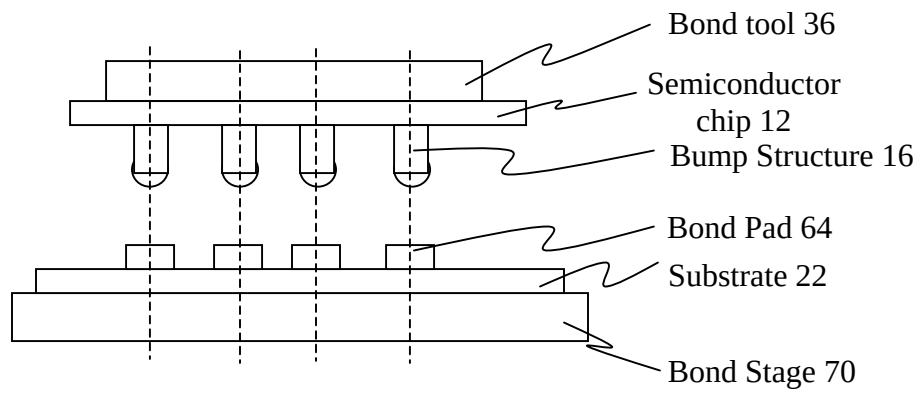


FIG. 15b

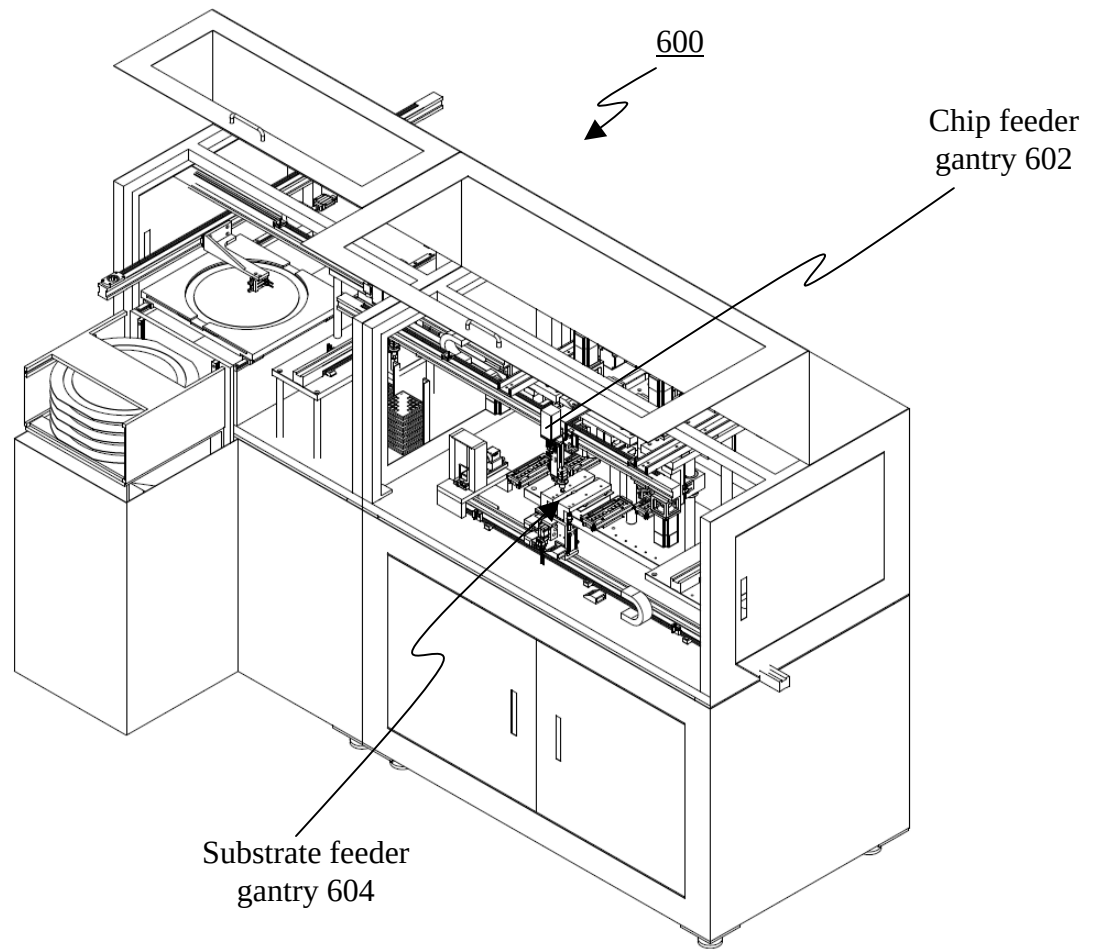


FIG. 16

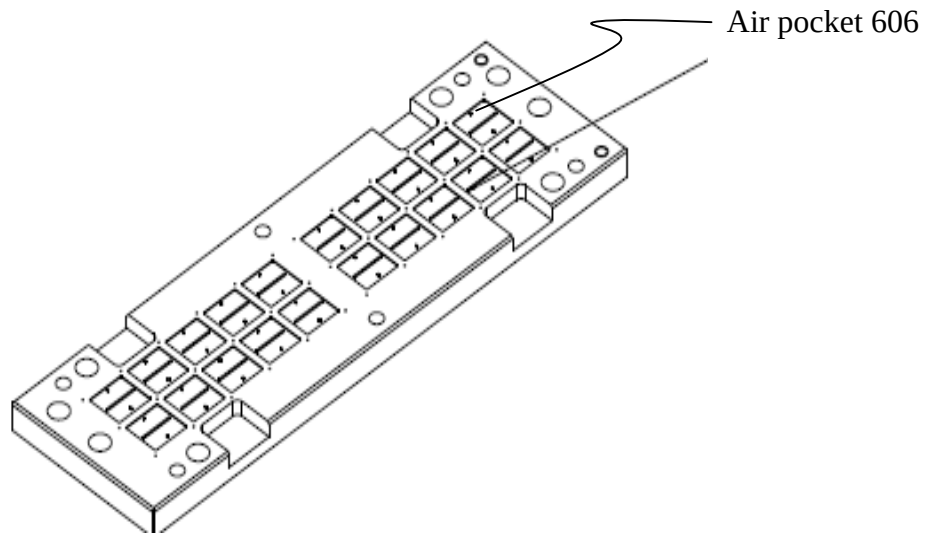


FIG. 17

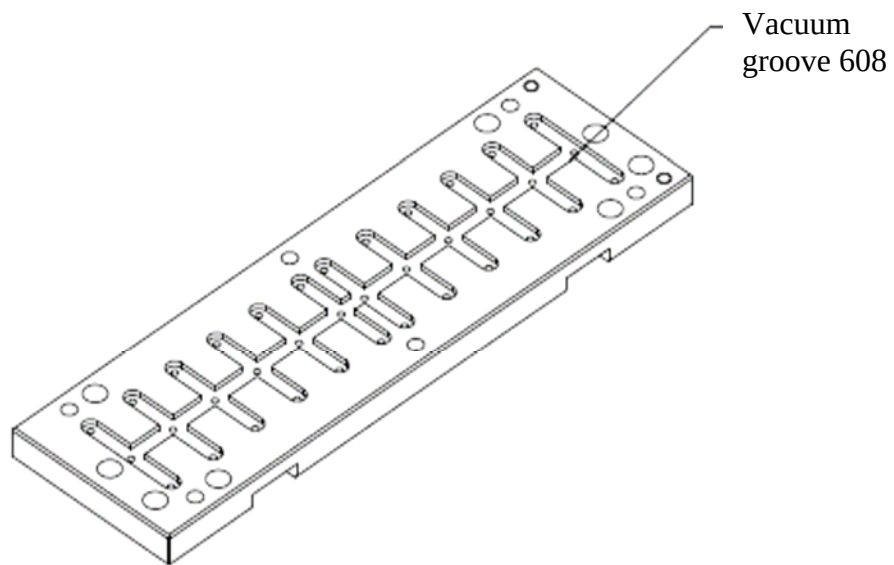


FIG. 18

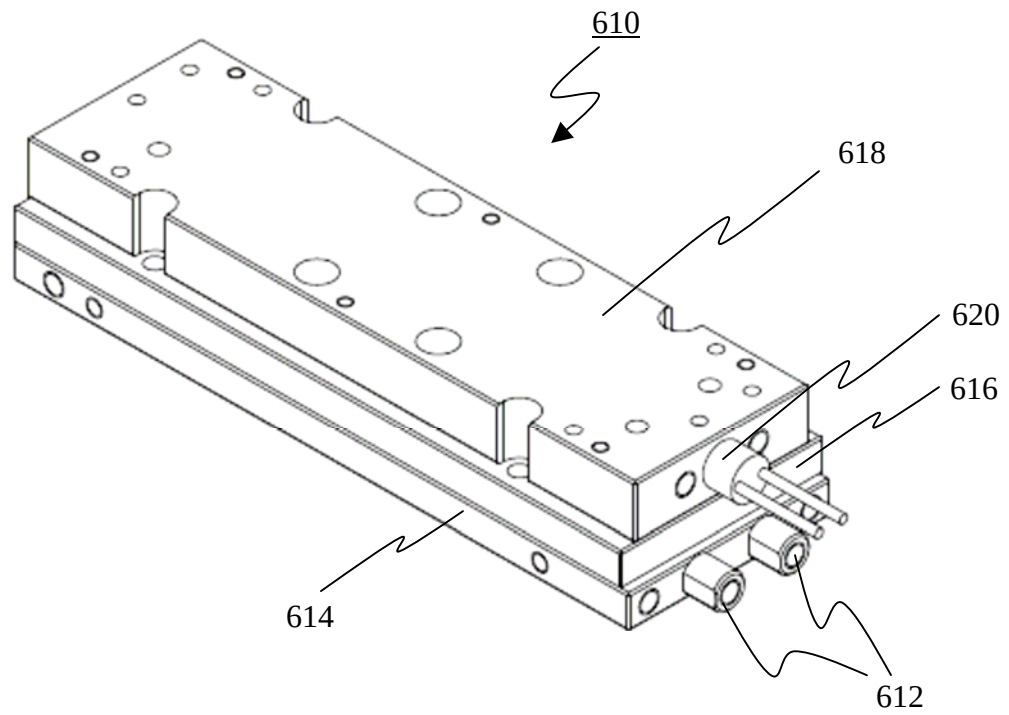


FIG. 19