Capacitor Constructions, Methods of Forming Capacitor Constructions, and Methods of Forming Constructions Comprising Dielectric Materials

TECHNICAL FIELD

[0001] The invention pertains to capacitor constructions and methods of forming capacitor constructions. The invention also pertains to methods of forming constructions comprising dielectric materials.

BACKGROUND OF THE INVENTION

[0002] There is a continuing interest to incorporate oxide dielectrics into semiconductor constructions. Among the dielectrics that are of particular interest are those represented by the formula MO_z, where M represents a metal, O is oxygen, and z is a number greater than 0, and typically less than or equal to 8. The metal can be a transition metal, such as, for example, hafnium, or a non-transition metal, such as, for example, aluminum. The dielectric materials can be useful in, for example, capacitor constructions.

[0003] A difficulty in utilizing metal oxide dielectrics (MO_z) is that diffusion can occur between the dielectric materials and structures proximate to the dielectric materials, and such diffusion can adversely affect properties of the dielectric material and/or the structures proximate to the dielectric material. For instance, if a conductive structure comprises conductively-doped silicon and MO_z is formed directly on the conductively-doped silicon, oxygen from the MO_z can interact with the silicon to oxidize the silicon. The oxidized silicon will no longer have the desired conductive properties of conductively-doped silicon.

[0004] The problems discussed above can be alleviated, and even prevented, through utilization of a metal nitride barrier layer. The metal nitride can be represented as MN_y, where M is metal, N is nitrogen, and y is a number greater than 0 and typically less than 8. The metal nitride is frequently referred to as a diffusion barrier layer, as the metal nitride alleviates, and frequently even prevents, diffusion to and/or from a metal oxide dielectric. U.S. Patent 5,741,721 describes exemplary structures in which metal oxide dielectric materials are formed over metal nitride barrier layers. Patent 5,741,721 specifically describes processes in which a metal nitride layer is formed over a semiconductor substrate, and subsequently a surface of the metal nitride layer is oxidized to form a metal oxide dielectric material.

[0005] The processing described in U.S. Patent 5,741,721 can be difficult to incorporate into various semiconductor fabrication processes. Accordingly, it would be

desirable to develop alternative methods for forming metal oxide dielectric material adjacent diffusion barrier layers.

SUMMARY OF THE INVENTION

[0006] In one aspect, the invention encompasses a method of forming a construction which includes a dielectric material. A layer comprising one or more of MC_x, MB_q and MN_y is formed, with M being a metal, and with q, x and y being numbers greater than 0. A dielectric material comprising MO_z is deposited over and directly against the layer, with z being a number greater than 0. In particular aspects, the layer and the dielectric material can comprise a metal (for example, hafnium or aluminum) in common.

[0007] In one aspect, the invention pertains to a method of forming a capacitor construction. A first electrically conductive material is formed over a semiconductor substrate. An intermediate layer is formed over the first electrically conductive material. The intermediate layer predominantly comprises a composition of a metal and one or more of boron, nitrogen and carbon. A dielectric layer is deposited over and directly against the intermediate layer, with the dielectric layer predominantly comprising a composition of the metal and oxygen. A second electrically conductive material is formed over the dielectric layer. The second electrically conductive material is capacitively connected with the first electrically conductive material.

[0008] In one aspect, the invention encompasses a capacitor construction. The construction includes a first electrically conductive material, and a first intermediate layer over the first electrically conductive material. The first intermediate layer predominantly comprises a composition of aluminum and one or more of boron, nitrogen and carbon. A dielectric material is over and directly against the first intermediate layer. The dielectric material predominantly comprises a composition of aluminum and oxygen. A second intermediate layer is over the dielectric material, with the second intermediate layer predominantly comprising the composition of aluminum and one or more of boron, nitrogen and carbon. A second electrically conductive material is over the second intermediate layer. The second electrically conductive material is capacitively connected with the first electrically conductive material. The capacitor construction can be incorporated into a dynamic random access memory (DRAM) cell. The DRAM cell can be utilized in an electronic system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0010] Fig. 1 is a diagrammatic cross-sectional view of a semiconductor wafer fragment at a preliminary processing stage of an exemplary method of the present invention.

[0011] Fig. 2 is a view of the Fig. 1 wafer fragment shown as a processing stage subsequent to that of Fig. 1.

[0012] Fig. 3 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 2.

[0013] Fig. 4 is a view of the Fig. 1 water fragment shown at a processing stage subsequent to that of Fig. 3.

[0014] Fig. 5 is a diagrammatic cross-sectional view of an apparatus that can be utilized for conducting a deposition in accordance with various exemplary aspects of the present invention.

[0015] Fig. 6 is a diagrammatic view of a computer illustrating an exemplary application of the present invention.

[0016] Fig. 7 is a block diagram showing particular features of the motherboard of the Fig. 6 computer.

[0017] Fig. 8 is a high-level block diagram of an electronic system according to an exemplary aspect of the present invention.

[0018] Fig. 9 is a simplified block diagram of an exemplary electronic system according to an aspect of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] The invention includes structures in which a layer comprising metal carbide, metal boride and/or metal nitride is provided proximate a metal oxide dielectric material. The metal carbide can be referred to as MC_x, where M is a metal, C is carbon, and x is a number greater than 0 and typically less than 8; the metal boride can be referred to as MB_q, where M is metal, B is boron, and q is a number greater than 0 and typically less than 8; the metal nitride can be referred to as MN_y, where M is a metal, N is nitrogen, and y is a number greater than 0 and typically less than 8; and the metal oxide can be referred to as MO_z, where M is a metal, O is oxygen, and z is a number greater than 0 and typically less than 8.

[0020] The metal oxide dielectric material has a metal in common with the layer comprising metal carbide, metal boride and/or metal nitride, and such can improve stacking of the dielectric material when the dielectric material is directly against the layer comprising metal carbide, metal boride and/or metal nitride. The layer comprising metal carbide, metal boride and/or metal nitride can be a barrier layer between the metal oxide dielectric material and another material, and/or can be a nucleation layer utilized for

growth of the metal oxide dielectric material in a deposition process. Exemplary metals of the metal oxide, metal carbide, metal boride and metal nitride include aluminum, hafnium and lanthanide metals, with the lanthanide metals including lanthanum and the elements of the lanthanide series for purposes of interpreting this disclosure and the claims that follow.

[0021] The invention includes methods of forming the layer comprising metal carbide, metal boride and/or metal nitride together with the metal oxide dielectric layer. The invention also includes constructions utilizing the layer comprising metal nitride, metal boride and/or metal carbide in combination with the metal oxide dielectric layer, with exemplary constructions being capacitor constructions.

[0022] An exemplary process of the present invention is described with reference to Fig. 1-5. The exemplary process fabricates an exemplary capacitor construction.

[0023] Referring to Fig. 1, a semiconductor wafer fragment 10 is illustrated at a preliminary processing stage of the exemplary process of the present invention. Fragment 10 comprises a semiconductor substrate 12. Substrate 12 can comprise, for example, monocrystalline silicon lightly doped with background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0024] A transistor device 14 is shown supported by substrate 12. Device 14 comprises a pair of source/drain regions 16 and 18 extending into substrate 12. The source/drain regions each include a heavily doped region 20 extending relatively deep into substrate 12 and a lightly doped region 22 extending less deep into substrate 12 than the heavily doped region. A channel region 24 is between source/drain regions 16 and 18, and a transistor gate 26 is over the channel region. Transistor gate 26 includes an insulative material 28 (which can be, for example, silicon dioxide, and can be referred to as gate oxide), a conductive material 30 over the insulative material (the conductive material can comprise one or more layers, and in particular aspects will comprise conductively-doped silicon and/or various metals), and an electrically insulative cap 32 over the conductive material (the insulative cap 32 can comprise, for example, silicon nitride and/or silicon dioxide).

[0025] A pair of sidewall spacers 34 and 36 extend along sidewalls of gate 26 and over lightly-doped regions 22. Spacers 34 and 36 can comprise any suitable electrically insulative material, including, for example, silicon dioxide and/or silicon nitride. Transistor structure 14 is an exemplary conventional structure, and can be fabricated using conventional methodologies. Other transistor structures can be utilized in place of transistor structure 14.

[0026] An electrically conductive pedestal 38 is provided over source/drain region 16. Pedestal 38 can comprise any suitable electrically conductive material, including, for example, conductively-doped silicon and/or various metals. Pedestal 38 has an upper surface 40 which defines an electrical node. It is to be understood that pedestal 38 is optional. If pedestal 38 is eliminated, then the electrical node can be considered to be an upper surface of the diffusion region corresponding to source/drain region 16.

[0027] An electrically insulative material 42 is provided over transistor 14, and an opening 44 is formed through insulative material 42 to expose electrical node 40. Insulative material 42 can comprise any suitable material, including, for example, borophosphosilicate glass (BPSG).

[0028] Referring to Fig. 2, an electrically conductive material 46 is provided over an upper surface of insulative material 42 and within opening 44. Electrically conductive material 46 can ultimately be utilized as a capacitor electrode in a capacitor construction formed in accordance with an exemplary aspect of the invention. Conductive material 46 can comprise any suitable electrically conductive material, including, for example, conductively-doped silicon and/or various metals. If material 46 comprises metals, the metals can be utilized either in elemental form, or as conductive compounds. Layer 46 can be referred to as a first electrically conductive material in the discussion that follows, to distinguish layer 46 from conductive materials formed subsequent to layer 46.

[0029] Although layer 46 is shown having a smooth outer surface, it is to be understood that layer 46 can also have a roughened (or rugged) outer surface in particular aspects of the invention. For instance, if layer 46 comprises conductively-doped silicon, the outer surface of layer 46 can correspond to hemispherical grain silicon, and accordingly would be a rugged surface.

[0030] A barrier layer 48 is formed over conductive material 46. Barrier layer 48 comprises one or more of metal carbide (MC_x), metal boride (MB_q) and metal nitride (MN_y). The metal of barrier layer 48 can comprise a transition metal (such as, for example, hafnium, titanium, tantalum, lanthanides, etc.) or a non-transition metal (such as, for example, aluminum, etc.). Barrier layer 48 is shown to be electrically conductive, but it is to be understood that layer 48 could alternatively be electrically insulative. The

conductivity of layer 48 depends on the particular metal composition utilized in the layer, and it is to be understood that some metal carbides and/or metal nitrides suitable for utilization in layer 48 would be electrically insulative rather than electrically conductive. If layer 48 is electrically conductive, layer 46 can be omitted in some aspects of the invention. If layer 46 is omitted, material 48 can physically contact electrical node 40.

[0031] Layer 48 is referred to above as a "barrier" as layer 48 is preferably a barrier which prevents reaction between substances associated with a dielectric material (described below) provided on one side of layer 48 with substances from other structures (such as, for example, the shown layer 46) provided on the other side of layer 48. It is to be understood, however, that the invention encompasses aspects in which layer 48 is utilized for other physical characteristics alternatively to, or in addition to, the barrier properties of the layer. For instance, the dielectric material formed over layer 48 typically comprises a metal oxide having a metal in common with the metal nitride, metal boride and/or metal carbide of layer 48. Layer 48 can be utilized for the preferred stacking characteristics of having a metal in common between a metal oxide dielectric material and an underlying metal nitride, metal boride and/or metal carbide material. Layer 48 can be referred to as an intermediate layer in the discussion that follows, rather than as a barrier layer, and in other aspects of the description that follows, layer 48 can be referred to as a diffusion barrier layer.

[0032] Layer 48 can have any suitable composition of metal carbide, metal boride and/or metal nitride. In particular aspects, layer 48 will consist essentially of, or consist of metal carbide; in other aspects layer 48 will consist essentially of, or consist of metal boride; and in other aspects, layer 48 will consist essentially of, or consist of metal nitride. In specific applications, layer 48 can comprise, consist essentially of, or consist of hafnium carbide and/or hafnium nitride. In other aspects, layer 48 can comprise, consist essentially of, or consist of aluminum carbide and/or aluminum nitride. In yet other aspects, layer 48 can comprise, consist essentially of, or consist of one or more lanthanide metal carbides and/or one or more lanthanide metal nitrides. It is emphasized, however, that the metal utilized in layer 48 can be any suitable metal, including, for example, hafnium, lanthanide metals or aluminum; but is not limited to the exemplary metals of hafnium, aluminum and lanthanide metals.

[0033] Layer 48 can comprise any suitable thickness, and typically would comprise a thickness of from about 5Å to about 200Å. Layer 48 can be formed by any suitable method, and typically would be formed utilizing chemical vapor deposition (CVD) and/or atomic layer deposition (ALD).

[0034] Although only one layer 48 is shown, it is to be understood that multiple layers comprising metal carbide, metal boride and/or metal nitride could be formed. If

multiple layers are formed, the metals within the multiple layers can vary within the stack of multiple layers. In processing described below, a material oxide is formed over the one or more layers comprising metal nitride, metal boride and/or metal carbide. The top layer of a stack of multiple layers of metal nitride, metal boride and/or metal carbide will preferably have a metal in common with the metal oxide contacting such top layer.

[0035] Referring to Fig. 3, layers 46 and 48 are removed from over an upper surface of insulative material 42, while being retained within opening 44. A suitable process for removing layers 46 and 48 from over the upper surface of insulative material 42 can be, for example, chemical-mechanical polishing.

[0036] Referring next to Fig. 4, a layer of dielectric material 50 is deposited over the upper surface of insulative material 42 and over a surface of barrier layer 48 within opening 44. Dielectric material 50 can be formed directly against an upper surface of layer 48, as shown. Layer 50 comprises metal oxide (MO_z) and has at least one metal in common with the metal nitride (MN_y), metal boride (MB_q) and/or metal carbide (MC_x) of layer 48. Layer 50 can, for example, consist of a single metal oxide which has a metal in common with metal of layer 48; or comprise multiple metal oxides, of which only a subset has metal in common with one or more metals of layer 48; or can comprise multiple metal oxides of which all have metal in common with metals of layer 48. In particular exemplary aspects, layer 48 can comprise, consist essentially of, or consist of one or both of hafnium nitride and hafnium carbide, and layer 50 can comprise, consist essentially of, or consist of hafnium oxide. In other exemplary aspects, layer 48 can comprise, consist essentially of, or consist of one or more lanthanide metal nitrides and/or one or more lanthanide metal carbides, and layer 50 can comprise, consist essentially of, or consist of one or more lanthanide metal oxides. In other exemplary aspects, layer 48 can comprise, consist essentially of, or consist of aluminum nitride and/or aluminum carbide, and layer 50 can comprise, consist essentially of, or consist of aluminum oxide. In another exemplary aspect, layer 48 can predominantly comprise a composition of a metal and nitrogen, boron or carbon, with the term "predominantly comprise" indicating that more than 50 atomic percent of the layer is the stated composition. In such aspect, dielectric material 50 can predominantly comprise a composition of the metal and oxygen. Dielectric material 50 is typically formed to a thickness of from about 20Å to about 60Å.

[0037] Although only one layer 50 is shown, it is to be understood that multiple layers comprising metal oxide could be formed. If multiple layers are formed, the metals within the multiple layers can vary within the stack of multiple layers. The bottom layer of a stack of multiple layers of metal oxide (i.e., the layer of the metal oxide stack that is in contact with metal carbide, metal boride and/or metal nitride of layer 48) will

preferably have a metal in common with the metal carbide, metal boride and/or metal nitride contacting such bottom layer.

[0038] In some aspects of the invention, metal oxide layer 50 can be formed in a common deposition process with the metal nitride, metal boride and/or metal carbide of layer 48. In such aspects, the processing of Fig. 3 is omitted (specifically, layers 46 and 48 are not patterned prior to formation of dielectric material 50). In an exemplary process, layer 48 is formed utilizing one or both of CVD and ALD in reaction chamber, and subsequently dielectric material 50 is deposited utilizing one or both of CVD and ALD in situ in the same reaction chamber utilized for deposition of layer 48. The term "in situ" is utilized to indicate that vacuum to the reaction chamber is not broken between the deposition of layer 48 and the deposition of layer 50.

[0039] Since layers 48 and 50 have a metal in common, the deposition of layers 48 and 50 can occur in a continuous and uninterrupted process. Specifically, the deposition of layer 48 can occur by flowing a metal-containing precursor into a reaction chamber in combination with precursors of one or more of carbon, boron and nitrogen. After layer 48 has been formed to a desired thickness, the flow of nitrogen, boron and/or carbon precursor is replaced by a flow of oxygen precursor to initiate formation of layer 50. If the processing utilized for formation of layer 48 is an ALD process, then layer 48 can be formed utilizing a reaction sequence in which metal-containing precursor is flowed into a reaction chamber in an alternating sequence with carbon, boron and/or nitrogen precursors to build up layers of desired metal nitride, metal boride and/or metal carbide materials. After layer 48 is built to a desired thickness, the flow of nitrogen, boron and/or carbon precursor can be replaced with a flow of oxygen precursor. The metal precursor can then be flowed in an alternating sequence with the oxygen precursor to the build up layers of dielectric material 50.

[0040] An exemplary reaction chamber which can be utilized for chemical vapor deposition and/or atomic layer deposition is described with reference to Fig. 5. Specifically, Fig. 5 shows a cross-sectional view of an apparatus 100 comprising a reaction chamber 102. A wafer holder 104 is provided within the reaction chamber, and is shown supporting a semiconductor wafer substrate 106. Chamber 100 has an inlet 108 extending into reaction chamber 102 and an outlet 110 extending from the reaction chamber. Inlet 108 and outlet 110 are controllably blocked with valves 112 and 114, respectively.

[0041] In operation, precursor is flowed into chamber 102 through inlet 108 (as represented by an arrow 116 in the diagram of Fig. 5), and is utilized to form a desired layer (not shown) over exposed surfaces of substrate 106. At appropriate times, reaction by-products and/or unreacted precursor is removed from chamber 102 through

outlet 110 (as indicated by arrow 118 in the diagram of Fig. 5). In a CVD process, two or more precursors would be introduced into reaction chamber 102 to react with one another and form a desired layer over substrate 106. In an ALD process, the precursors would be introduced sequentially into reaction chamber 102, and would be provided within the chamber separate from one another. Accordingly, in an ALD process there would be no reaction (or at least no detectable reaction) of precursors with one another in chamber 102, but rather the precursors would be utilized to build up monolayers over a surface of substrate 106.

[0042] Referring again to Fig. 4, a second barrier layer 52 is formed over dielectric material 50. Second barrier layer 52 can, like the first barrier layer 48, comprise metal nitride, metal boride and/or metal carbide, and can have a metal in common with dielectric material 50. In particular aspects, second barrier layer 52 comprises an identical composition to first barrier layer 48. Layer 52 can, like layer 48, be referred to as an intermediate layer, rather than as a barrier layer, to emphasize that layer 52 can be utilized for other properties in addition to, or alternatively to, its barrier properties.

[0043] Layer 52 is shown as a conductive layer, but it is to be understood that layer 52 can alternatively be electrically insulative depending on the particular composition utilized in layer 52.

[0044] Layer 52 can be formed in a CVD and/or ALD process common to that utilized for layer 50. In other words, layer 52 can be formed in the same reaction chamber utilized for deposition of layer 50, and in particular aspects, will be formed in situ relative to layer 50 in a continuous process relative to that utilized for forming layer 50. In some aspects of the invention, layers 48, 50 and 52 can all be formed in a continuous deposition process (such as, for example, a deposition process utilizing CVD and/or ALD). Specifically, all of layers 48, 50 and 52 can be formed in a common reaction chamber without breaking a vacuum to the chamber from the time that deposition of layer 48 is started until the time that deposition of layer 52 is completed.

[0045] A second electrically conductive electrode 54 is formed over layer 52. Electrode 54 can comprise, consist essentially of, or consist of conductively-doped silicon and/or various metals and/or metal compositions. In aspects in which layer 52 is electrically conductive, layer 54 can be omitted, and layer 52 can be utilized as the second electrode. However, even when layer 52 is electrically conductive it can be advantageous to form layer 52 relatively thin (such as, for example, to a thickness from about 5Å to about 200Å), and to use layer 52 in combination with another conductive material 54 as a capacitor electrode.

[0046] Layers 46, 48, 50, 52 and 54 together define a capacitor construction 60. Conductive materials 46 and 48 can be considered to be a first electrode of the capacitor, and conductive materials 52 and 54 can be considered to be a second electrode of the capacitor. The second electrode is capacitively connected to the first electrode, and spaced from the first electrode by dielectric material 50. In constructions in which layers 48 and 52 comprise dielectric materials, the layers 48, 50 and 52 can together be a dielectric material separating a first capacitor electrode defined by layer 46 from a second capacitor electrode defined by layer 54.

[0047] Capacitor construction 60 can be incorporated into a DRAM cell. Specifically, the source/drain region 18 can be connected to a bitline 70. Capacitor construction 60 can thus be gatedly connected with bitline 70 through transistor 14.

[0048] The present approach can provide numerous advantages. For instance, the present invention can provide the ability to do high temperature oxide depositions (which can give denser, better quality oxide films) since the deposition can start with reducing chemistry that will not oxidize the bottom cell plate (i.e., that will not oxidize electrode 46). After the bottom oxygen barrier (nitride, boride and/or carbide) is deposited (i.e., after deposition of layer 48), the chemistry can be changed to an oxidizing one and the dielectric deposition can be conducted to form material 50. Methodology of the present invention can additionally enable a good lattice match to be obtained between a nitride, boride and/or a carbide layer relative to a metal oxide material. Also, the layer 48 can prevent oxidation of underlying layer 46 which otherwise occur if layer 50 were provided directly against layer 46. Additionally, it is noted that in applications in which aluminum oxide is utilized as the dielectric material, and aluminum carbide and/or nitride is utilized for layers 48 and 52, the layers 48 and 52 will be electrically insulative. The permittivity of layers 48 and 52 will be comparable to that of the aluminum oxide layer 50, which can allow a better quality dielectric material (better permittivity) to be obtained than can be obtained utilizing other insulative nitrides, such as, for example, silicon nitride.

[0049] It is noted that the thickness of the nitride, boride and/or carbide layers 48 and 52 can vary according to a desired use, or combination of uses of the layers. For instance, if layers 48 and 52 are utilized as the sole electrodes of a capacitor construction, the layers are preferably formed relatively thick (i.e., have a thickness greater than about 50Å). In contrast, if the layers are utilized in combination with other conductive materials in capacitor electrodes, the layers can be formed very thin, such as, for example, to a thickness of less than about 10Å, and even to a thickness of less than about 5Å.

[0050] Devices comprising constructions formed in accordance with methodology of the present invention (such as the above-described DRAM cell) can be utilized in numerous assemblies, including, for example, computer systems and other electronic systems.

[0051] Fig. 6 illustrates generally, by way of example, but not by way of limitation, an embodiment of a computer system 400 according to an aspect of the present invention. Computer system 400 includes a monitor 401 or other communication output device, a keyboard 402 or other communication input device, and a motherboard 404. Motherboard 404 can carry a microprocessor 406 or other data processing unit, and at least one memory device 408. Memory device 408 can comprise various aspects of the invention described above, including, for example, the DRAM cell described with reference to Fig. 4. Memory device 408 can comprise an array of memory cells, and such array can be coupled with addressing circuitry for accessing individual memory cells in the array. Further, the memory cell array can be coupled to a read circuit for reading data from the memory cells. The addressing and read circuitry can be utilized for conveying information between memory device 408 and processor 406. Such is illustrated in the block diagram of the motherboard 404 shown in Fig. 7. In such block diagram, the addressing circuitry is illustrated as 410 and the read circuitry is illustrated as 412.

[0052] In particular aspects of the invention, memory device 408 can correspond to a memory module. For example, single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) may be used in the implementation which utilizes the teachings of the present invention. The memory device can be incorporated into any of a variety of designs which provide different methods of reading from and writing to memory cells of the device. One such method is the page mode operation. Page mode operations in a DRAM are defined by the method of accessing a row of a memory cell arrays and randomly accessing different columns of the array. Data stored at the row and column intersection can be read and output while that column is accessed.

[0053] An alternate type of device is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. This memory can increase some communication speeds by allowing shorter access signals without reducing the time in which memory output data is available on a memory bus. Other alternative types of devices include SDRAM, DDR SDRAM, SLDRAM, VRAM and Direct RDRAM, as well as others such as SRAM or Flash memories.

[0054] Fig. 8 illustrates a simplified block diagram of a high-level organization of various embodiments of an exemplary electronic system 700 of the present invention.

System 700 can correspond to, for example, a computer system, a process control system, or any other system that employs a processor and associated memory. Electronic system 700 has functional elements, including a processor or arithmetic/logic unit (ALU) 702, a control unit 704, a memory device unit 706 and an input/output (I/O) device 708. Generally, electronic system 700 will have a native set of instructions that specify operations to be performed on data by the processor 702 and other interactions between the processor 702, the memory device unit 706 and the I/O devices 708. The control unit 704 coordinates all operations of the processor 702, the memory device 706 and the I/O devices 708 by continuously cycling through a set of operations that cause instructions to be fetched from the memory device 706 and executed. In various embodiments, the memory device 706 includes, but is not limited to, random access memory (RAM) devices, read-only memory (ROM) devices, and peripheral devices such as a floppy disk drive and a compact disk CD-ROM drive. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that any of the illustrated electrical components are capable of being fabricated to include DRAM cells in accordance with various aspects of the present invention.

[0055] Fig. 9 is a simplified block diagram of a high-level organization of various embodiments of an exemplary electronic system 800. The system 800 includes a memory device 802 that has an array of memory cells 804, address decoder 806, row access circuitry 808, column access circuitry 810, read/write control circuitry 812 for controlling operations, and input/output circuitry 814. The memory device 802 further includes power circuitry 816, and sensors 820, such as current sensors for determining whether a memory cell is in a low-threshold conducting state or in a high-threshold non-conducting state. The illustrated power circuitry 816 includes power supply circuitry 880, circuitry 882 for providing a reference voltage, circuitry 884 for providing the first wordline with pulses, circuitry 886 for providing the second wordline with pulses, and circuitry 888 for providing the bitline with pulses. The system 800 also includes a processor 822, or memory controller for memory accessing.

[0056] The memory device 802 receives control signals 824 from the processor 822 over wiring or metallization lines. The memory device 802 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 802 has been simplified to help focus on the invention. At least one of the processor 822 or memory device 802 can include a DRAM cell of the type described previously in this disclosure.

[0057] The various illustrated systems of this disclosure are intended to provide a general understanding of various applications for the circuitry and structures of the present invention, and are not intended to serve as a complete description of all the

elements and features of an electronic system using memory cells in accordance with aspects of the present invention. One of ordinary skill in the art will understand that the various electronic systems can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device(s).

[0058] Applications for memory cells can include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

CLAIMS

The invention claimed is:

1. A method of forming a construction which includes a dielectric material, the method comprising:

forming a layer comprising one or more of MC_x, MN_y and MB_q over a substrate; where M is a metal, and where x, y and q are numbers greater than 0; and

after forming the layer, depositing a dielectric material comprising MO_z directly against the layer, where z is a number greater than 0.

2. The method of claim 1 wherein the layer consists essentially of MC_x.

3. The method of claim 1 wherein the layer consists of MC_x.

4. The method of claim 1 wherein the layer consists essentially of MN_y.

5. The method of claim 1 wherein the layer consists of MN_y.

6. The method of claim 1 wherein the layer consists essentially of MB_q.

7. The method of claim 1 wherein the layer consists of MB_q.

8. The method of claim 1 wherein M is a transition metal.

9. The method of claim 1 wherein M is hafnium.

10. The method of claim 1 wherein M is aluminum.

11. The method of claim 1 wherein M is a lanthanide metal.

12. The method of claim 1 wherein the layer is formed by chemical vapor deposition in a reaction chamber; and wherein the deposition of the dielectric material comprises chemical vapor deposition occurring in situ in the reaction chamber relative to the formation of the layer.

13. The method of claim 1 wherein the layer is formed by atomic layer deposition in a reaction chamber; and wherein the deposition of the dielectric material comprises atomic layer deposition occurring in situ in the reaction chamber relative to the formation of the layer.

14. The method of claim 1 wherein the layer is a first layer, and further comprising forming a second layer over the dielectric material; the second layer comprising one or more of MC_x, MB_q and MN_y.

15. The method of claim 14 wherein the second layer consists essentially of MC_x.

16. The method of claim 14 wherein the second layer consists of MC_x.

17. The method of claim 14 wherein the second layer consists essentially of MN_y.

18. The method of claim 14 wherein the second layer consists of MN_y.

19. The method of claim 14 wherein the second layer consists essentially of MB_q.

20. The method of claim 14 wherein the second layer consists of MB_q.

21. The method of claim 14 wherein the first and second layers consist essentially of MC_x.

22. The method of claim 14 wherein the first and second layers have the same chemical composition as one another.

23. The method of claim 14 wherein the first and second layers consist of MC_x.

24. The method of claim 14 wherein the first and second layers consist essentially of MN_y.

25. The method of claim 14 wherein the first and second layers consist of MN_y.

26. The method of claim 14 wherein the first and second layers consist essentially of MB_q.

27. The method of claim 14 wherein the first and second layers consist of MB_q.

28. A method of forming a semiconductor construction, comprising:

forming a first layer over a semiconductor substrate; the first layer predominantly comprising a composition containing metal and nitrogen, a composition containing metal and boron, or a composition containing metal and carbon; and

after forming the first layer, depositing a second layer directly against the first layer, the second layer predominantly comprising a composition of the metal and oxygen.

29. The method of claim 28 wherein the first layer consists essentially of the metal and carbon.

30. The method of claim 29 wherein the first layer is formed utilizing one or both of chemical vapor deposition and atomic layer deposition in a reaction chamber; and wherein the deposition of the second layer comprises chemical vapor deposition or atomic layer deposition occurring in situ in the reaction chamber relative to the formation of the first layer.

31. The method of claim 28 wherein the first layer consists essentially of the metal and nitrogen.

32. The method of claim 31 wherein the first layer is formed utilizing one or both of chemical vapor deposition and atomic layer deposition in a reaction chamber; and wherein the deposition of the second layer comprises chemical vapor deposition or atomic layer deposition occurring in situ in the reaction chamber relative to the formation of the first layer.

33. The method of claim 28 wherein the first layer consists essentially of the metal and boron.

34. The method of claim 28 wherein the metal is a transition metal.

35. The method of claim 28 wherein the metal is aluminum.

36. The method of claim 28 further comprising forming a third layer directly against the dielectric layer; the third layer predominantly comprising a composition of the metal and one or more of nitrogen, boron and carbon.

37. The method of claim 36 wherein the first and third layers consist essentially of the metal and carbon.

38. The method of claim 36 wherein the first and third layers consist essentially of the metal and nitrogen.

39. The method of claim 36 wherein the first and third layers consist essentially of the metal and boron.

40. A method of forming a capacitor construction, comprising:

providing a semiconductor substrate;

forming a first electrically conductive material over the semiconductor substrate;

forming an intermediate layer over the first electrically conductive material; the intermediate layer predominantly comprising a composition of a metal and one or more of nitrogen, boron and carbon;

depositing a dielectric layer directly against the intermediate layer, the dielectric layer predominantly comprising a composition of the metal and oxygen; and

forming a second electrically conductive material over the dielectric layer; the second electrically conductive material being capacitively connected with the first electrically conductive material.

41. The method of claim 40 wherein the intermediate layer consists essentially of the metal and carbon.

42. The method of claim 41 wherein the intermediate layer is formed utilizing one or both of chemical vapor deposition and atomic layer deposition in a reaction chamber; and wherein the deposition of the dielectric layer comprises chemical vapor deposition or atomic layer deposition occurring in situ in the reaction chamber relative to the formation of the intermediate layer.

43. The method of claim 40 wherein the intermediate layer consists essentially of the metal and nitrogen.

44. The method of claim 43 wherein the intermediate layer is formed utilizing one or both of chemical vapor deposition and atomic layer deposition in a reaction chamber; and wherein the deposition of the dielectric layer comprises chemical vapor deposition or atomic layer deposition occurring in situ in the reaction chamber relative to the formation of the intermediate layer.

45. The method of claim 40 wherein the intermediate layer consists essentially of the metal and boron.

46. The method of claim 40 wherein the metal is a transition metal.

47. The method of claim 40 wherein the metal is aluminum.

48. The method of claim 40 wherein the intermediate layer consists essentially of aluminum nitride.

49. The method of claim 40 wherein the intermediate layer consists essentially of aluminum carbide.

50. The method of claim 40 wherein the intermediate layer consists essentially of hafnium nitride.

51. The method of claim 40 wherein the intermediate layer consists essentially of hafnium carbide.

52. The method of claim 40 wherein the intermediate layer is a first intermediate layer, and further comprising forming a second intermediate layer over the dielectric layer prior to forming the second conductive material; the second intermediate layer predominantly comprising a composition of the metal and one or more of nitrogen, boron and carbon.

53. The method of claim 52 wherein the second intermediate layer is formed directly against the dielectric layer.

54. The method of claim 53 wherein the second electrically conductive material is formed directly against the second intermediate layer.

55. The method of claim 52 wherein the first and second intermediate layers consist essentially of the metal and carbon.

56. The method of claim 52 wherein the first and second intermediate layers consist essentially of the metal and nitrogen.

57. The method of claim 52 wherein the first and second intermediate layers consist essentially of the metal and boron.

58. The method of claim 52 wherein the first and second intermediate layers consist essentially of aluminum nitride.

59. The method of claim 52 wherein the first and second intermediate layers consist essentially of aluminum carbide.

60. The method of claim 52 wherein the first and second intermediate layers consist essentially of hafnium nitride.

61. The method of claim 52 wherein the first and second intermediate layers consist essentially of hafnium carbide.

62. The method of claim 52 wherein the first and second intermediate layers consist essentially of lanthanide metal nitride.

63. The method of claim 52 wherein the first and second intermediate layers consist essentially of lanthanide metal carbide.

64. A capacitor construction, comprising:

a first electrically conductive material;

a first intermediate layer over the first electrically conductive material; the first intermediate layer predominantly comprising a composition of a metal and carbon;

a dielectric material over and directly against the first intermediate layer, the dielectric material predominantly comprising a composition of the metal and oxygen;

a second intermediate layer over the dielectric material; the second intermediate layer predominantly comprising the composition of the metal and carbon; and

a second electrically conductive material over the second intermediate layer; the second electrically conductive material being capacitively connected with the first electrically conductive material.

65. The capacitor construction of claim 64 wherein the second intermediate layer physically contacts the dielectric material.

66. The capacitor construction of claim 65 wherein the second electrically conductive material physically contacts the second intermediate layer.

67. The capacitor construction of claim 64 wherein the metal is a transition metal.

68. The capacitor construction of claim 64 wherein the first and second intermediate layers consist essentially of aluminum carbide.

69. The capacitor construction of claim 64 wherein the first and second intermediate layers consist essentially of hafnium carbide.

70. A DRAM cell comprising the capacitor construction of claim 64.

71. An electronic system comprising the DRAM cell of claim 70.

72. A capacitor construction, comprising:

a first electrically conductive material;

a first intermediate layer over the first electrically conductive material; the first intermediate layer predominantly comprising a composition of aluminum and one or more of nitrogen, boron and carbon;

a dielectric material over and directly against the first intermediate layer, the dielectric material predominantly comprising a composition of aluminum and oxygen;

a second intermediate layer over the dielectric material; the second intermediate layer predominantly comprising the composition of aluminum and one or more of boron, nitrogen and carbon; and

a second electrically conductive material over the second intermediate layer; the second electrically conductive material being capacitively connected with the first electrically conductive material.

73. The capacitor construction of claim 72 wherein the second intermediate layer physically contacts the dielectric material.

74. The capacitor construction of claim 73 wherein the second electrically conductive material physically contacts the second intermediate layer.

75. The capacitor construction of claim 72 wherein the first and second intermediate layers consist essentially of aluminum carbide.

76. The capacitor construction of claim 72 wherein the first and second intermediate layers consist essentially of aluminum boride.

77. The capacitor construction of claim 72 wherein the first and second intermediate layers consist essentially of aluminum nitride.

78. A DRAM cell comprising the capacitor construction of claim 72.

79. An electronic system comprising the DRAM cell of claim 78.