Claims

1. Process for fabricating an image sensor, comprising:

- providing a receiver substrate ~~(1)~~ comprising a base substrate ~~(10)~~ and an active layer comprising pixels ~~(11)~~, each pixel comprising a doped region ~~(12)~~ for collecting the electric charges generated in the pixel, said receiver substrate ~~(1)~~ being devoid of metal interconnections,

- providing a donor substrate ~~(2)~~ comprising a weakened zone ~~(200)~~ delimiting a monocrystalline semiconductor layer ~~(201)~~,

- bonding the donor substrate ~~(2)~~ to the receiver substrate ~~(1)~~,

- detaching the donor substrate ~~(2)~~ along the weakened zone ~~(200)~~ so as to transfer the semiconductor layer ~~(201)~~ to the receiver substrate ~~(1)~~,

- implementing a finishing treatment on the transferred semiconductor layer ~~(201)~~, said finishing treatment comprising (i) thinning of the transferred layer by sacrificial oxidation followed by chemical etching and (ii) smoothing of the transferred semiconductor layer by means of at least one rapid annealing.

2. Process according to Claim 1, wherein each rapid annealing is controlled in order to prevent diffusion of the dopants from the doped regions ~~(12)~~ of the pixels ~~(11)~~.

3. Process according to Claim 1 or 2, wherein each rapid annealing is implemented at a temperature of between 1100 and 1250°C for a duration of between 15 and 60 s.

4. Process according to one of Claims 1 to 3, wherein the sacrificial oxidation and the chemical etching are controlled in order to thin the transferred monocrystalline semiconductor layer ~~(201)~~ to a thickness of between 10 and 100 nm.

5. Process according to one of Claims 1 to 4, wherein the chemical etching for thinning the transferred monocrystalline semiconductor layer ~~(201)~~ is implemented by means of a wet etching, a plasma dry etching, an ion-beam dry etching or a cluster-ion-beam dry etching.

6. Process according to one of Claims 1 to 5, further comprising, after the finishing of the transferred monocrystalline semiconductor layer ~~(201)~~, the formation of components ~~(25)~~ of a readout circuit for reading out the pixels in or on said transferred semiconductor layer ~~(201)~~.

7. Process according to Claim 6, further comprising, after the finishing of the transferred monocrystalline semiconductor layer ~~(201)~~, the formation of interconnections ~~(26)~~ between the pixels ~~(11)~~ and said components ~~(25)~~ of the pixel readout circuit.

8. Process according to one of Claims 1 to 7, comprising the formation of the weakened zone ~~(200)~~ by implanting atomic species into the donor substrate ~~(2)~~.

9. Process according to Claim 8, wherein the finishing treatment successively comprises:

(i) a first rapid annealing,

(ii) removal of defects related to the implantation by sacrificial oxidation of the transferred layer,

(iii) a second rapid annealing, and

(iv) the thinning of the transferred layer.

10. Process according to one of Claims 1 to 9, wherein the donor substrate ~~(2)~~ further comprises at least one electrically insulating layer ~~(23)~~ on the monocrystalline semiconductor layer ~~(201)~~.

11. Process according to one of Claims 1 to 10, wherein the donor substrate ~~(2)~~ further comprises at least one semiconductor layer ~~(24)~~ on the monocrystalline semiconductor layer ~~(201)~~.

12. Process according to one of Claims 10 and 11 in combination with Claim 8, wherein the electrically insulating layer ~~(23)~~ or the semiconductor layer ~~(24)~~, respectively, is deposited on the donor substrate before the implantation.

13. Process according to one of Claims 1 to 9, wherein the receiver substrate ~~(1)~~ further comprises a semiconductor layer ~~(15)~~ on the active layer.

14. Process according to one of Claims 1 to 9 and 13, wherein the receiver substrate ~~(1)~~ further comprises an electrically insulating layer ~~(16)~~ on the active layer.

15. Process according to one of Claims 1 to 14, wherein each rapid annealing has a temperature ramp-up rate of more than 10°C per second, preferably more than or equal to 50°C per second.

16. Process according to one of Claims 1 to 15, wherein the smoothing comprises no heat treatment having a temperature ramp-up rate of less than 10°C per second.

17. Process according to one of Claims 1 to 16, wherein the smoothing is implemented individually for each structure comprising the semiconductor layer ~~(201)~~ and the receiver substrate ~~(1)~~.