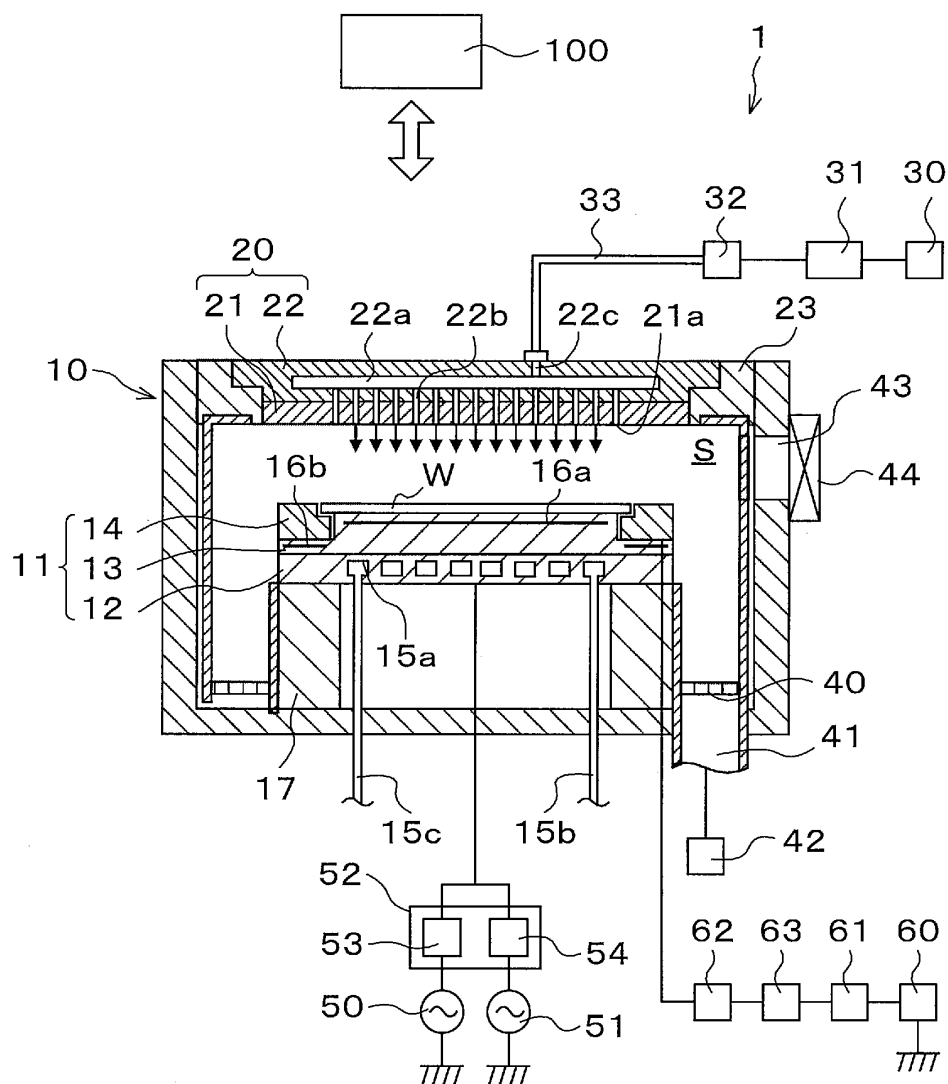
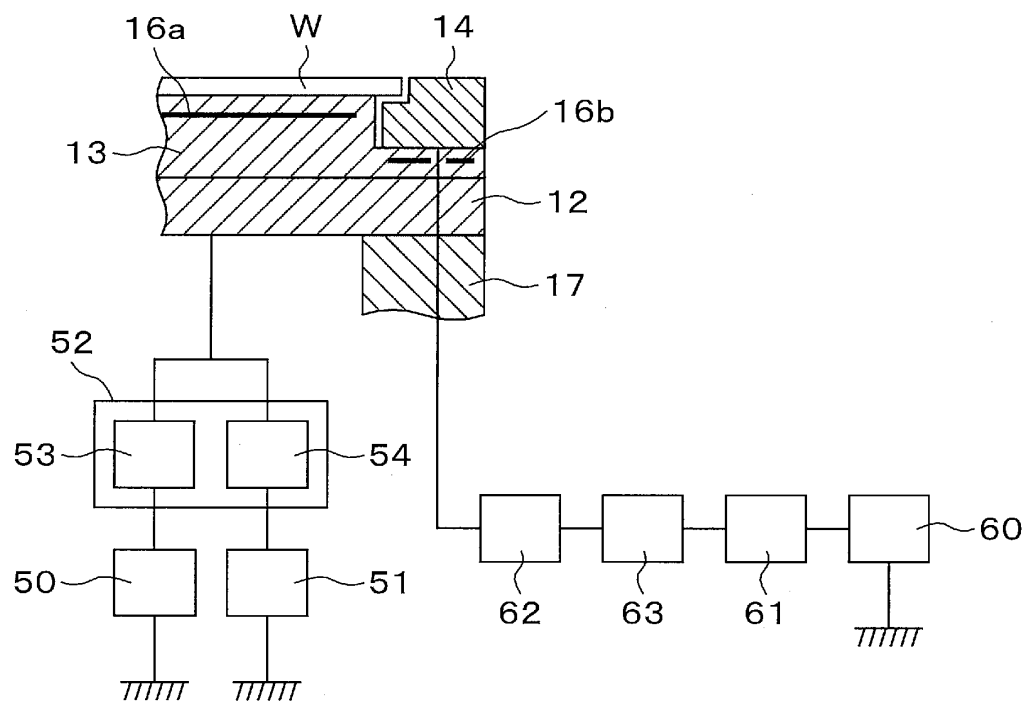


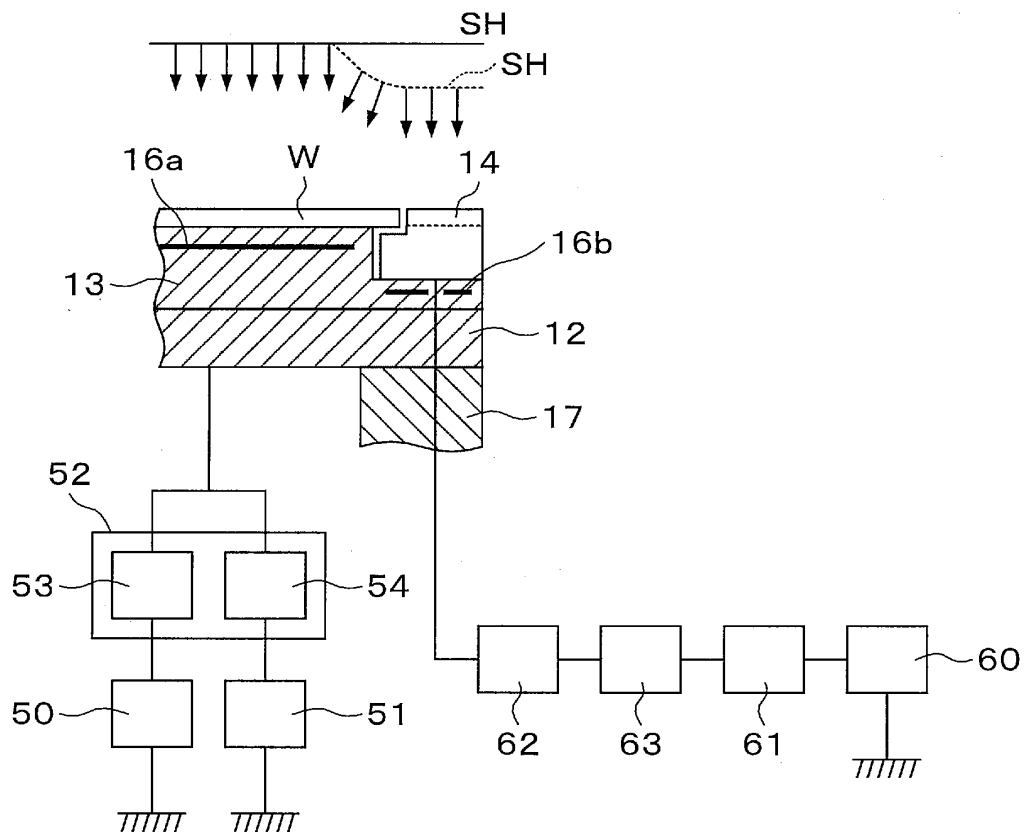
[図1]



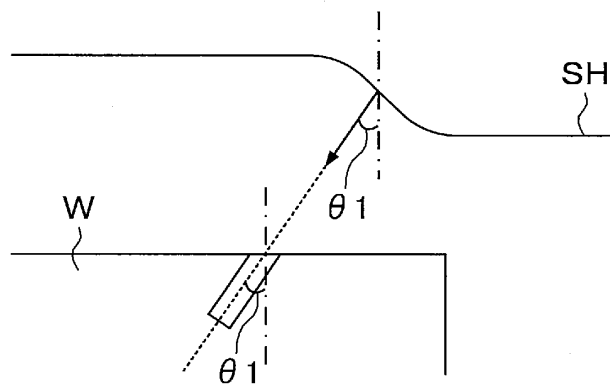
[図2]



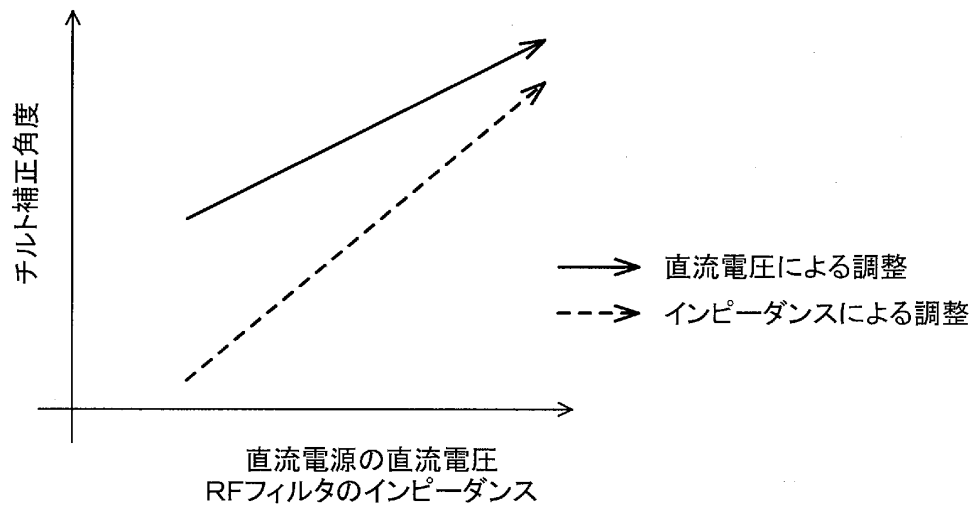
[図3A]



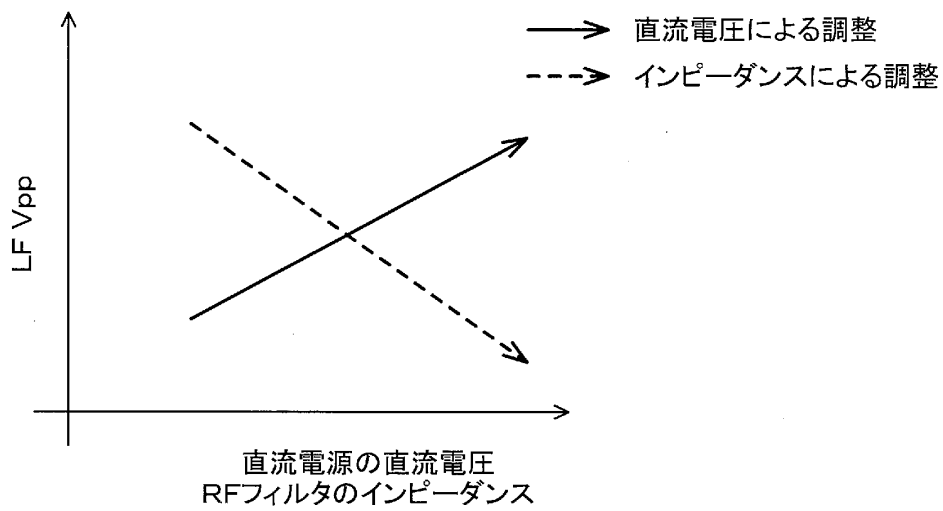
[図3B]



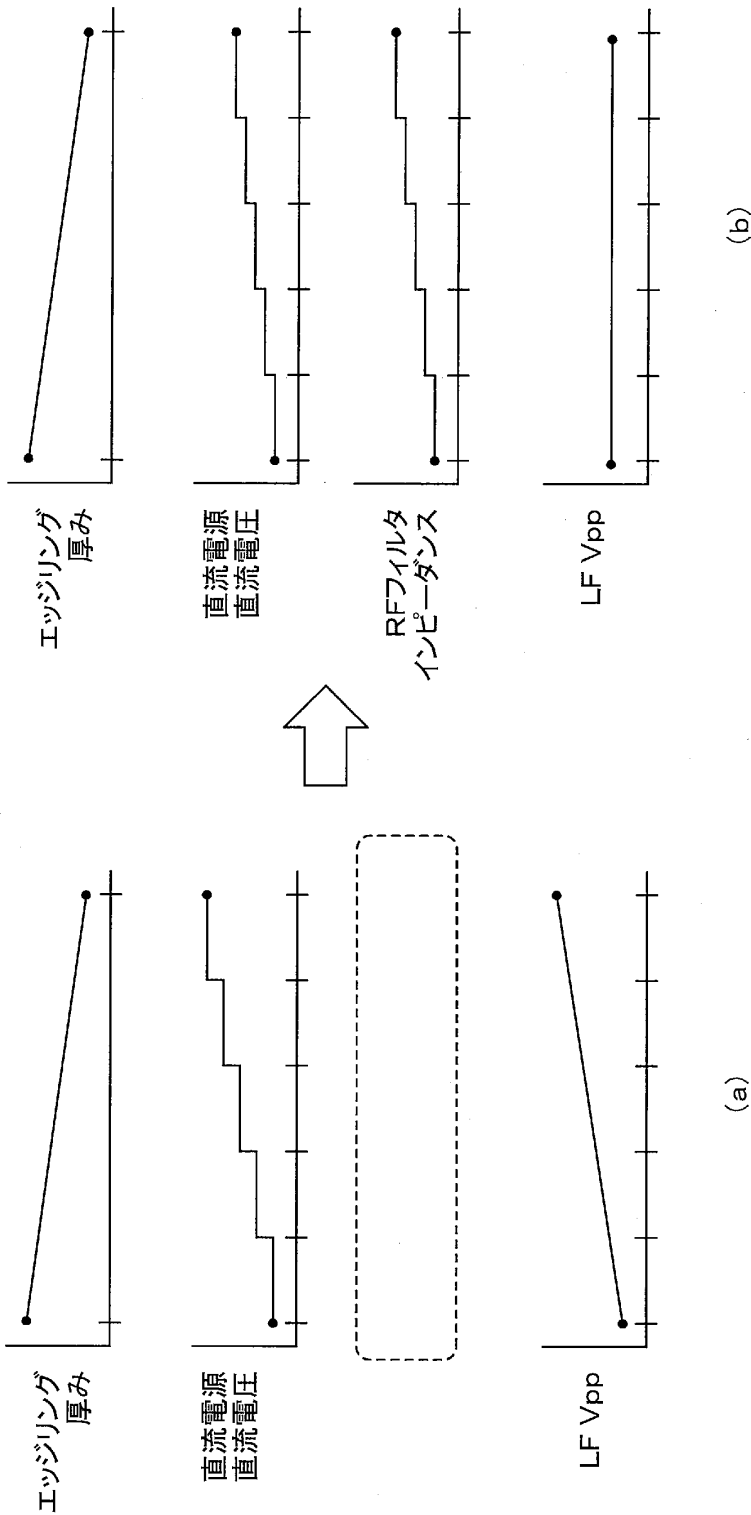
[図5]



[図6]



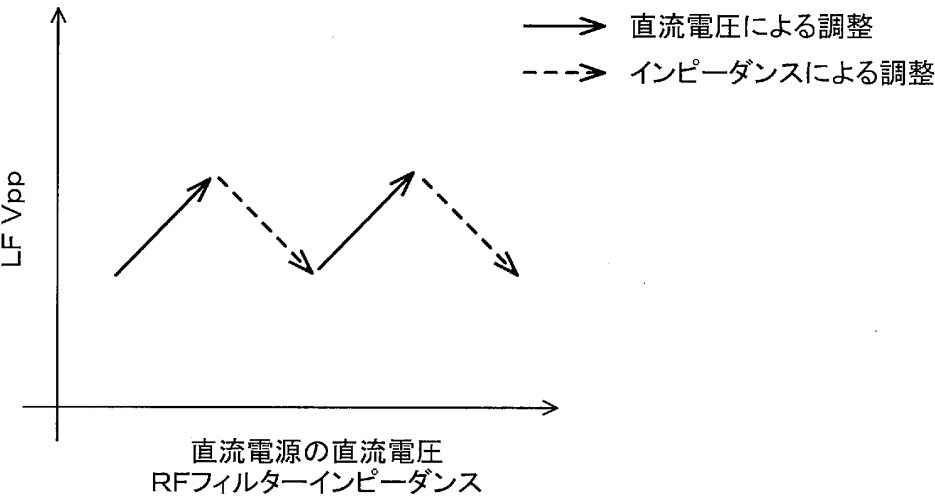
[図7]



[図8]

		RFフィルタインピーダンス			
		Z1	Z2	Z3	Z4
直流電源 直流電圧	V1			Edge ring New	
	V2				
	V3	Edge ring Life limit			
	V4				

[図9]



[図10]

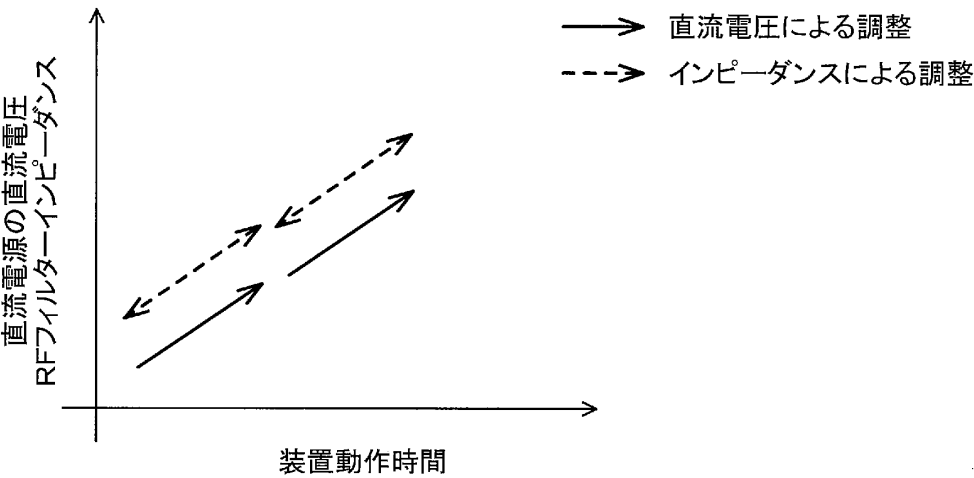
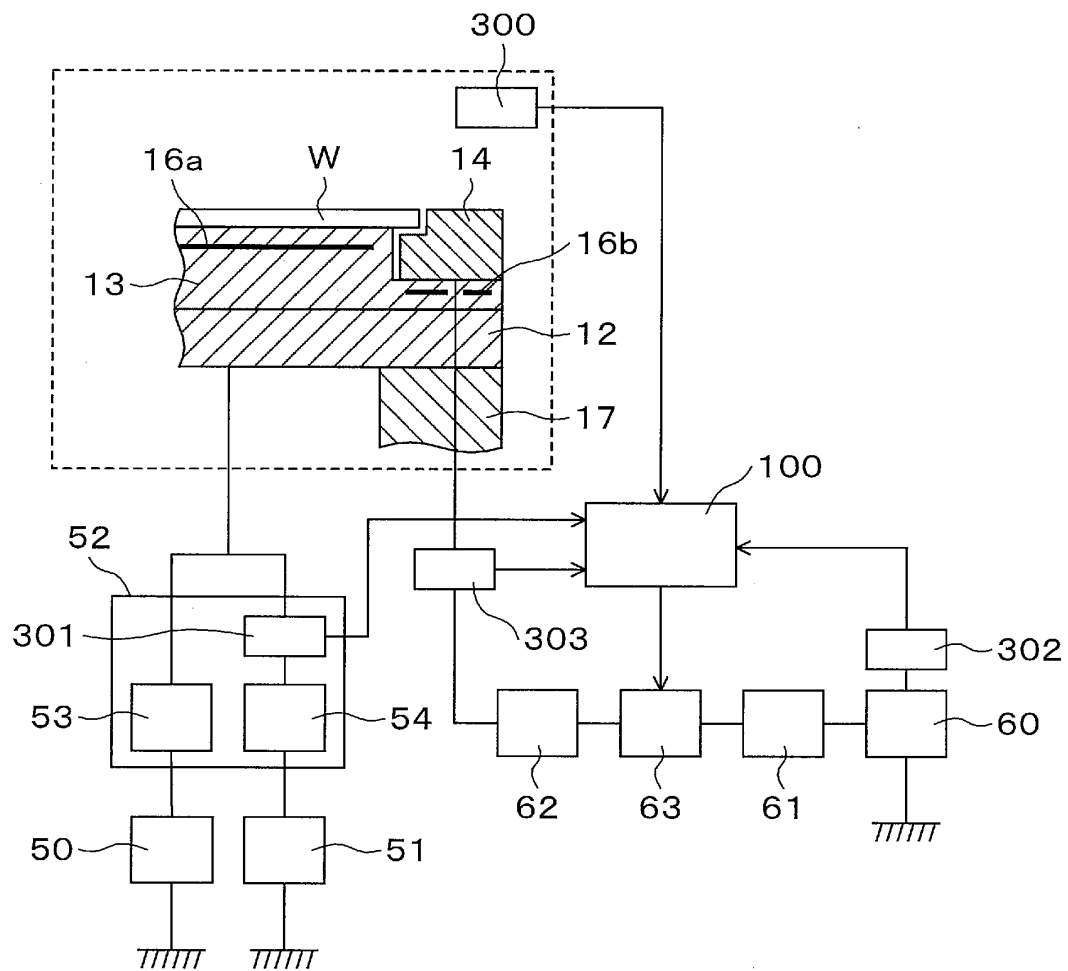
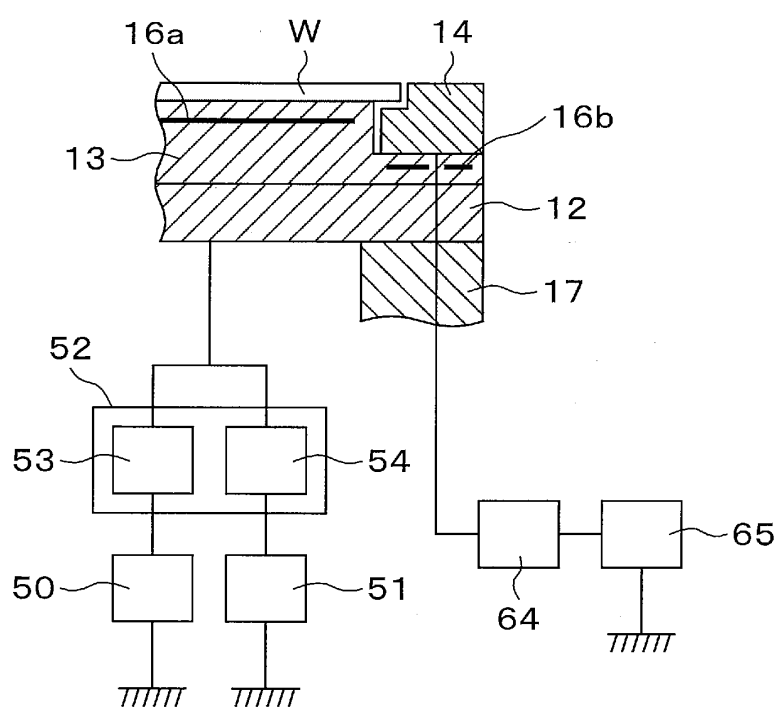


Figure 1 is a cross-sectional view of a semiconductor device and its electrical circuit. The cross-section shows a substrate 12 with a layer 13 on top. A gate structure 14 is formed on the surface, with a gate oxide 16a and a gate electrode 16b. A source/drain region 17 is formed in the substrate 12. A contact 201 is formed in the source/drain region 17, and a contact 202 is formed in the gate electrode 16b. The contact 202 is connected to a circuit. The circuit includes a transistor 50 with gate 52 and source/drain 53, 54. The transistor 50 is connected to a series of transistors 61, 62, 63, and 60. The transistor 60 is connected to ground.

[図12]



[図13]



[図14]

