QUICK PAGING CHANNEL WITH REDUCED PROBABILITY OF MISSED PAGE

Claim of Priority under 35 U.S.C. §119

[0001] This application claims the benefit of U.S. Provisional Application No.60/691,901, filed June 16, 2005, entitled "QUICK PAGING CHANNEL WITH REDUCED PROBABILITY OF MISSED PAGES," and Provisional Application Serial No. 60/731,037, filed October 27, 2005, entitled "METHODS AND APPARATUS FOR PROVIDING MOBILE BROADBAND WIRELESS HIGHER MAC," both are assigned to the assignee hereof and hereby expressly incorporated by reference herein.

BACKGROUND

[0002] In a random access wireless communication system, a communication link between an access terminal and an access point is not continuous. An access terminal can register with an access point and can remain in an idles state. The access terminal can transition from the idle state to an active state to initiate an active communication link. In the active state, the access terminal is able to receive information from the access point as well as transmit information to the access point.

[0003] For the majority of the time, the access terminal remains in the idle state, awaiting the transition into the active state. The access terminal is typically a mobile device that operates from batteries stored within the device. The access terminals can conserve energy and extend the battery operated run time by transitioning to a low power state, often referred to as a sleep state. However, in many instances, the access terminal cannot immediately transition from the sleep state to the active state.

[0004] The access terminal typically does not have the ability to monitor information transmitted by the access points when it is in the sleep state. Therefore, the access terminals typically periodically transition to an idle state to monitor for messages from the access points.

[0005] Some wireless communication systems incorporate quick paging channels that are used by the access points to indicate the presence of a paging message to an access

terminal. The paging message can direct the particular access terminal to transition to the active state to support active information exchange.

[0006] The wireless communication system can assign a particular bit in a particular message as the quick paging bit for a particular access terminal or group of access terminals. The access terminals can then awaken from a sleep state for a duration that is sufficient to receive the quick paging bit. If the access terminal detects an active quick paging bit, the access terminal becomes aware of a subsequent paging message and can remain in or transition to the idle state to monitor for the paging message. Conversely, if the access terminal fails to detect its assigned quick paging bit, it assumes that there are no imminent paging messages directed to it. In this manner, the access terminals can minimize the time that they need to be in an idle mode, thereby maximizing the time that can be dedicated to a lower power sleep state.

[0007] For example, both CDMA2000 and WCDMA wireless communication systems have a quick paging channel that allows a mobile station to periodically monitor an assigned quick paging bit to detect a presence of a page. When a page is sent to the mobile station, the base station sets the corresponding bit to 1. If the bit is set, the mobile station, which represents the access terminal, listens to the full page. However, if the access terminal improperly detects the bit to be 0, or determines an erasure indicating the inability to discern the state of the received bit, then a missed page occurs. Therefore, there is a need to reduce the probability of a missed page. However, there remains the need to maintain or increase the battery powered operational time for mobile devices.

BRIEF SUMMARY

[0008] A quick paging channel in a random access wireless communication system includes at least one bit in a quick paging frame identifying the presence of a paging message for an access terminal or group of access terminals. The quick paging bits identifying the presence of a paging message for a first access terminal is encoded with one or more quick paging bits corresponding to one or more additional access terminals to produce one or more forward error correction bits. The jointly encoded quick paging bits are broadcast to the access terminals by time division multiplexing the quick paging frame with additional frames of information.

[0009] Aspects of the disclosure include a method of notifying an access terminal. The method includes determining presence of a scheduled message for the access terminal, setting a quick paging bit from a plurality of quick paging bits in a quick paging block, the quick paging bit corresponding to the access terminal, encoding the quick paging block to generate an encoded quick paging packet, generating at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block, and transmitting the at least one OFDM symbol.

[0010] Aspects of the disclosure include a method of notifying an access terminal. The method includes setting a quick paging bit corresponding to the access terminal in a quick paging block having a plurality of bits corresponding to a plurality of access terminals, compressing the quick paging block to generate a compressed quick paging block, and encoding the compressed quick paging block to generate an encoded quick paging block.

[0011] Aspects of the disclosure include a method of processing a quick paging message. The method includes receiving a quick paging packet, decoding the quick paging packet to generate a quick paging block, decompressing the quick paging block, and determining a status of a quick paging bit associated with an access terminal based on an output of the decompressing process.

[0012] Aspects of the disclosure include a system for generating a quick paging message that includes a scheduler configured to determine scheduled a paging message for an access terminal, a quick paging block generator coupled to the scheduler and configured to assert a quick paging bit corresponding to the access terminal and configured to generate a quick paging block having at least the quick paging bit and a distinct quick paging bit corresponding to a distinct access terminal, an encoder coupled to the quick paging block generator and configured to generate an encoded quick paging packet based on the quick paging block, and a transmit processor coupled to the encoder and configured to generate at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging packet.

[0013] Aspects of the disclosure include a system for generating a quick paging message that includes means for determining presence of a scheduled message for the access terminal, means for setting a quick paging bit from a plurality of quick paging

bits in a quick paging block, the quick paging bit corresponding to the access terminal, means for encoding the quick paging block to generate an encoded quick paging packet, means for generating at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block, and means for transmitting the at least one OFDM symbol.

[0014] Aspects of the disclosure include a system for generating a quick paging message that includes means for setting a quick paging bit corresponding to the access terminal, means for jointly encoding the quick paging bit with at least one additional quick paging bit corresponding to a distinct access terminal to generate an encoded quick paging block, and means for time division multiplexing the encoded quick paging block with distinct information over a channel.

[0015] Aspects of the disclosure include a system for generating a quick paging message that includes means for receiving a quick paging packet, means for decoding the quick paging packet to generate a quick paging block, means for decompressing the quick paging block, and means for determining a status of a quick paging bit associated with an access terminal based on an output of the decompressing process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The features, objects, and advantages of embodiments of the disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like elements bear like reference numerals.

[0017] Figure 1 is a simplified functional block diagram of an embodiment of a multiple access wireless communication system.

[0018] Figure 2 is a simplified functional block diagram of an embodiment of a transmitter and receiver in a multiple access wireless communication system.

[0019] Figure 3 is a simplified functional block diagram of an embodiment of a transmitter implementing the quick paging block.

[0020] Figure 4 is a simplified functional block diagram of an embodiment of a receiver configured to process the quick paging block.

[0021] Figure 5 is a simplified flowchart of an embodiment of a method of generating a quick paging block.

[0022] Figure 6 is a simplified flowchart of an embodiment of a method of processing a quick paging block.

[0023] Figure 7 is a simplified functional block diagram of an embodiment of a transmitter implementing the quick paging block.

[0024] Figure 8 is a simplified functional block diagram of an embodiment of a receiver configured to process the quick paging block.

DETAILED DESCRIPTION

[0025] A wireless communication system can decrease the probability of missed pages by providing some form of redundancy associated with the quick paging bit. Rather than merely extending the number of quick paging bits assigned to each access terminal, the wireless communication system can provide redundancy through the joint encoding of a plurality of quick paging bits. In this manner, each access terminal or group of access terminals is assigned a single quick paging bit, but redundancy is provided through joint encoding of a plurality of quick paging bits. The wireless communication system can reduce the probability of a missed paging message by increasing the number of redundant bits, which can be forward error correction bits. There is no theoretical limit to the number of redundant bits that may be added from the joint encoding process. However, from a practical perspective, the number of redundant bits is likely less than the number of bits required to send the actual paging messages.

[0026] The wireless communication system can periodically transmit a quick paging block having the jointly encoded quick paging message. The number of quick paging bits set in each quick paging block is likely relatively low, provided the wireless communication system schedules a quick paging block at a sufficiently high rate. The relative sparse population of set quick paging bits in any particular quick paging frame allows the wireless communication system to compress the quick paging block to further reduce the number of bits that are transmitted to the access terminals. The wireless communication system can implement any one of various compression techniques, at least one of which is discussed in further detail below.

[0027] The quick paging channel having the jointly encoded quick paging bits can be transmitted to the various access terminals using a dedicated quick paging channel. Alternatively, the quick paging channel can be multiplexed with other channels. For example, the quick paging channel can be time division multiplexed, frequency division multiplexed, code division multiplexed, or otherwise multiplexed with other information.

[0028] In an Orthogonal Frequency Division Multiplex (OFDM) wireless communication system, the quick paging block, or compressed quick paging block, can be configured to be broadcast in a predetermined number of OFDM symbols. The wireless communication system can periodically transmit the OFDM symbol having the quick paging information. Thus, the system operates to time division multiplex the quick paging information over the channels used to carry other information.

[0029] Figure 1 is a simplified functional block diagram of an embodiment of a multiple access wireless communication system 100. A multiple access wireless communication system 100 includes multiple cells, e.g. cells 102, 104, and 106. In the embodiment of Figure 1, each cell 102, 104, and 106 may include an access point 150 that includes multiple sectors.

[0030] The multiple sectors are formed by groups of antennas each responsible for communication with access terminals in a portion of the cell. In cell 102, antenna groups 112, 114, and 116 each correspond to a different sector. For example, cell 102 is divided into three sectors, 120a-102c. A first antenna 112 serves a first sector 102a, a second antenna 114 serves a second sector 102b, and a third antenna 116 serves a third sector 102c. In cell 104, antenna groups 118, 120, and 122 each correspond to a different sector. In cell 106, antenna groups 124, 126, and 128 each correspond to a different sector.

[0031] Each cell is configured to support or otherwise serve several access terminals which are in communication with one or more sectors of the corresponding access point. For example, access terminals 130 and 132 are in communication with access point 142, access terminals 134 and 136 are in communication with access point 144, and access terminals 138 and 140 are in communication with access point 146. Although each of the access points 142, 144, and 146 is shown to be in communication with two access

terminals, each access point 142, 144, and 146 is not limited to communicating with two access terminals and may support any number of access terminals up to some limit that may be a physical limit, or a limit imposed by a communications standard.

[0032] As used herein, an access point may be a fixed station used for communicating with the terminals and may also be referred to as, and include some or all the functionality of, a base station, a Node B, or some other terminology. An access terminal (AT) may also be referred to as, and include some or all the functionality of, a user equipment (UE), a user terminal, a wireless communication device, a terminal, a mobile terminal, a mobile station or some other terminology.

[0033] It can be seen from Figure 1 that each access terminal 130, 132, 134, 136, 138, and 140 is located in a different portion of it respective cell than each other access terminal in the same cell. Further, each access terminal may be a different distance from the corresponding antenna groups with which it is communicating. Both of these factors provide situations, in addition to environmental and other conditions in the cell, to cause different channel conditions to be present between each access terminal and its corresponding antenna group with which it is communicating.

[0034] Each access terminal, for example 130, typically experiences unique channel characteristics not experienced by any other access terminal because of the varying channel conditions. Furthermore, the channel characteristics change over time and vary due to changes in location.

[0035] An access point, for example 142, may broadcast a frame or block having the quick paging information. Each of the access terminals, 130 and 132 within the coverage area of the access point 142 can receive the quick paging information and process it to determine if a quick paging bit that it is assigned to is active indicating the presence of a paging message directed to the access terminal.

[0036] The differing channel conditions experienced by the access terminals 130 and 132 alter their respective abilities to accurately recover the quick paging information. However, because the quick paging information is encoded to provide redundant information, such as one or more forward error correction bits, the access terminals 130 and 132 have a greater probability of successful determination of the assigned quick paging bits, thereby minimizing the probability of a missed page to that access terminal.

[0037] The wireless communication system 100 can multiplex the quick paging information over the same channels used for other information. For example, in an OFDM system, the wireless communication system 100 can broadcast the quick paging information across a channel employing some or all of the subcarrier frequencies. The subcarrier frequencies used to carry the quick paging information can be the same subcarriers used to carry other information to the access terminals. In this manner, the wireless communication system 100 can time division multiplex the quick paging channel with other channels of the system.

[0038] The above embodiments can be implemented utilizing transmit (TX) processor 220 or 260, processor 230 or 270, and memory 232 or 272, as shown in Figure 2. The processes may be performed on any processor, controller, or other processing device and may be stored as computer readable instructions in a computer readable medium as source code, object code, or otherwise.

[0039] Figure 2 is a simplified functional block diagram of an embodiment of a transmitter and receiver in a multiple access wireless communication system 200. At transmitter system 210, traffic data for a number of data streams is provided from a data source 212 to a transmit (TX) data processor 214. In an embodiment, each data stream is transmitted over a respective transmit antenna. TX data processor 214 formats, codes, and interleaves the traffic data for each data stream based on a particular coding scheme selected for that data stream to provide coded data. In some embodiments, TX data processor 214 applies beamforming weights to the symbols of the data streams based upon the user to which the symbols are being transmitted and the antenna from which the symbol is being transmitted. In some embodiments, the beamforming weights may be generated based upon channel response information that is indicative of the condition of the transmission paths between the access point and the access terminal. The channel response information may be generated utilizing CQI information or channel estimates provided by the user. Further, in those cases of scheduled transmissions, the TX data processor 214 can select the packet format based upon rank information that is transmitted from the user.

[0040] The coded data for each data stream may be multiplexed with pilot data using OFDM techniques. The pilot data is typically a known data pattern that is processed in a known manner and may be used at the receiver system to estimate the channel

response. The multiplexed pilot and coded data for each data stream is then modulated (i.e., symbol mapped) based on a particular modulation scheme (e.g., BPSK, QPSK, M-PSK, or M-QAM) selected for that data stream to provide modulation symbols. The data rate, coding, and modulation for each data stream may be determined by instructions provided by processor 230. In some embodiments, the number of parallel spatial streams may be varied according to the rank information that is transmitted from the user.

[0041] The modulation symbols for all data streams are then provided to a TX MIMO processor 220, which may further process the modulation symbols (for example, for OFDM). TX MIMO processor 220 then provides N_T symbol streams to N_T transmitters (TMTR) 222a through 222t. In certain embodiments, TX MIMO processor 220 applies beamforming weights to the symbols of the data streams based upon the user to which the symbols are being transmitted and the antenna from which the symbol is being transmitted from that users channel response information.

[0042] Each transmitter 222a through 222t receives and processes a respective symbol stream to provide one or more analog signals, and further conditions (e.g., amplifies, filters, and upconverts) the analog signals to provide a modulated signal suitable for transmission over the MIMO channel. N_T modulated signals from transmitters 222a through 222t are then transmitted from N_T antennas 224a through 224t, respectively.

[0043] At receiver system 250, the transmitted modulated signals are received by N_R antennas 252a through 252r and the received signal from each antenna 252 is provided to a respective receiver (RCVR) 254. Each receiver 254 conditions (e.g., filters, amplifies, and downconverts) a respective received signal, digitizes the conditioned signal to provide samples, and further processes the samples to provide a corresponding "received" symbol stream.

[0044] An RX data processor 260 then receives and processes the N_R received symbol streams from N_R receivers 254 based on a particular receiver processing technique to provide the rank number of "detected" symbol streams. The processing by RX data processor 260 is described in further detail below. Each detected symbol stream includes symbols that are estimates of the modulation symbols transmitted for the corresponding data stream. RX data processor 260 then demodulates, deinterleaves, and

decodes each detected symbol stream to recover the traffic data for the data stream. The processing by RX data processor 260 is complementary to that performed by TX MIMO processor 220 and TX data processor 214 at transmitter system 210.

[0045] The channel response estimate generated by RX processor 260 may be used to perform space, space/time processing at the receiver, adjust power levels, change modulation rates or schemes, or other actions. RX processor 260 may further estimate the signal-to-noise-and-interference ratios (SNRs) of the detected symbol streams, and possibly other channel characteristics, and provides these quantities to a processor 270. RX data processor 260 or processor 270 may further derive an estimate of the "effective" SNR for the system. Processor 270 then provides estimated channel information, such as the Channel Quality Index (CQI), which may comprise various types of information regarding the communication link and/or the received data stream. For example, the CQI may comprise only the operating SNR. The CQI is then processed by a TX data processor 278, which also receives traffic data for a number of data streams from a data source 276, modulated by a modulator 280, conditioned by transmitters 254a through 254r, and transmitted back to transmitter system 210.

[0046] At transmitter system 210, the modulated signals from receiver system 250 are received by antennas 224, conditioned by receivers 222, demodulated by a demodulator 240, and processed by a RX data processor 242 to recover the CQI reported by the receiver system. The reported CQI is then provided to processor 230 and used to (1) determine the data rates and coding and modulation schemes to be used for the data streams and (2) generate various controls for TX data processor 214 and TX MIMO processor 220.

[0047] At the receiver, various processing techniques may be used to process the N_R received signals to detect the N_T transmitted symbol streams. These receiver processing techniques may be grouped into two primary categories (i) spatial and space-time receiver processing techniques (which are also referred to as equalization techniques); and (ii) "successive nulling/equalization and interference cancellation" receiver processing technique (which is also referred to as "successive interference cancellation" or "successive cancellation" receiver processing technique).

[0048] A MIMO channel formed by the N_T transmit and N_R receive antennas may be decomposed into N_S independent channels, with $N_S \leq \min\{N_T, N_R\}$. Each of the N_S independent channels may also be referred to as a spatial subchannel (or a transmission channel) of the MIMO channel and corresponds to a dimension.

[0049] In the multiple access wireless communication system 200 of Figure 2, the TX data processor 214, in combination with the processor 230 and memory 232, can operate to determine the states of the various quick paging bits corresponding to the receiver systems 250 in the coverage area. The TX data processor 214 can be configured to encode the quick paging bits to generate one or more redundant bits, which can be forward error correction bits. The error correction bits can be, for example, a parity bit, a Cyclic Redundancy Code (CRC), or some other type of bits. The encoding can be systematic encoding or can be non-systematic encoding.

[0050] Each receiver system 250 can operate to receive the encoded quick paging information and recover the corresponding quick paging bit. The RX processor 260, in combination with the processor 270 and memory 272, can decode the quick paging information and determine whether its assigned quick paging bit is set to an active state. The receiver system 250 can detect or correct some errors in the quick paging information via the decoding process, and thereby reduce the probability of a missed page due to improper decoding or erasure of the assigned quick paging bit.

[0051] Figure 3 is a simplified functional block diagram of an embodiment of a transmitter 300 configured to implement an encoded quick paging channel. The transmitter 300 can be, for example, a portion of a transmitter system of Figure 2, or a portion of an access point shown in Figure 1. The transmitter 300 can be implemented within the multiple access wireless communication system of Figure 1 to minimize the probability that the access terminals will miss a scheduled paging message through a missed or otherwise unrecovered portion of a quick paging block.

[0052] The simplified functional block diagram of Figure 3 illustrates only a portion of the transmitter system associated with the quick paging channel (QPCH). The simplified functional block diagram does not show related blocks such as those associated with generating or mapping the paging messages that are associated with active quick paging bits.

[0053] The transmitter 300 embodiment of Figure 3 includes a timing and synchronization module 302 coupled to a scheduler 304. The scheduler 304 is coupled to a quick paging block generator 310, and initiates generation of the quick paging block. The quick paging block generator 310 is optionally coupled to a quick paging block compression module 312 that can be included to generate a compressed quick paging block. The quick paging block compression module 312 is coupled to an aggregator 330, which can be a combiner. A load control block module 320 generates one or more load control bits. The output of the load control block module 320 is coupled to the aggregator 330. The aggregator 330 appends the load control bits to the quick paging block or compressed quick paging block, depending on whether the quick paging block is compressed.

[0054] The aggregator 330 couples the combined quick paging and load control bits to an encoder 340. The encoder 340 operates to encode the bits. The encoded output is coupled to a TX MIMO processor 220. The TX MIMO processor 220 couples the signal to a transmitter stage 222 that transmits the signal using an antenna 224.

[0055] The transmitter 300 embodiment of Figure 3 includes a timing and synchronization module 302 that tracks the timing of the bits, frames, blocks, or packets generated by the transmitter 300. In one embodiment, the timing and synchronization module 302 maintains a bit synchronization, such that the bits generated by the transmitter 300 have substantially the same period.. The timing and synchronization module 302 can also synchronize and track frame timing, where each frame includes a predetermined number of bits. In an OFDM system, it may be advantageous for each frame to include the information for at least one OFDM symbol.

[0056] A superframe can include a predetermined number of frames. Additionally, specific frames within the superframe can be dedicated to particular information. For example, each superframe can include a preamble of a predetermined length, such as six frames or six OFDM symbols.

[0057] The superframe preamble can be used to populate a broadcast channel that is transmitted to all access terminals within a coverage area of an access point. One portion of the superframe preamble can be allocated to the quick paging channel (QPCH). For example, the QPCH packet can be one frame or OFDM symbol within the

superframe preamble. The length of the superframe preamble and the number of bits allocated to the QPCH packet can be varied based on the size of the information block allocated to the quick paging block.

[0058] In one embodiment, the number of bits allocated to the QPCH packet is static. In another embodiment, the number of bits allocated to the QPCH packet is dynamic and determined based at least in part on the number of quick paging bits that are active. Where the number of bits allocated to the QPCH packet is dynamic, the transmitter 300 can allocate a number of bits one of a predetermined set of QPCH packet lengths. Alternatively, the transmitter 300 can be configured to allocate any number of bits to the QPCH packet within a predetermined range or in increments of a single bit.

[0059] The transmitter 300 can be configured to send the size of the QPCH packet or quick paging block within the QPCH packet or some other message. In another embodiment, the transmitter 300 does not send the size of the QPCH packet, and relies on the receiver to determine the size of the packet.

[0060] The timing and synchronization module is coupled to a scheduler 304. The scheduler 304 tracks the communication links and information that is to be transmitted by the transmitter 300, and schedules the information, based in part on the system timing. In one embodiment, the scheduler 304 determines that the wireless communication system is attempting to set up an active communication session with an access terminal that is presently in an idle state.

[0061] The wireless communication system sends a paging message to the access terminal via the transmitter 300. Additionally, the wireless communication system sets one or more quick paging bits assigned to the access terminal or group of access terminals in which the desired access terminal is a member.

[0062] Although any number of quick paging bits can be assigned to each access terminal, typically only a single bit is assigned to each access terminal or access terminal group. For example, a quick paging block can be defined has having a predetermined number of quick paging bits, and a particular access terminal within the coverage area of an access point can be assigned to the nth quick paging bit in the quick paging block.

[0063] Although the description is primarily directed towards a single quick paging bit associated with a single access terminal within the particular coverage area, the wireless communication system may assign any number of quick paging bits to an access terminal. A set quick paging bit, whether active high or active low, indicates to the associated access terminal that a subsequent paging channel is direct to the access terminal.

[0064] As described above, a quick paging bit can be associated with a single access terminal or with a group of access terminals. When a quick paging bit is asserted, or otherwise set to an active state, the one or more access terminals associated with the quick paging bit know that at least one access terminal associated with the quick paging bit can expect a paging message. The wireless communication system can assign paging bits to groups of access terminals to minimize the total number of quick paging bits and thus the length of the quick paging block.

[0065] The quick paging block generator 310 determines from the scheduler 304 which quick paging bits to assert. In one example, the quick paging block generator sets to "1" each quick paging bit that is associated with an access that can expect a paging message, typically at the next opportunity for transmitting paging messages.

[0066] The quick paging block generator 310 couples the quick paging block having the properly asserted quick paging bits to an optional quick paging block compression module 312. The quick paging block compression module 312 operates to reduce the number of bits needed to represent the asserted quick paging bits.

[0067] The quick paging block compression module 312 can implement virtually any compression technique. The compression technique can implement one or more compression algorithms that can produce lossless compression, lossy compression or some combination of lossless compression or lossy compression of the quick paging block, depending on the number of quick paging bits asserted, the position of the quick paging bits in the quick paging block, or some combination thereof.

[0068] The quick paging block compression module 312 compresses the quick paging block of length N_{QP_BLK} to generate a compressed quick paging block of length $N_{QP_MSG_COMP}$. In one embodiment, the length of the compressed quick paging block

can be variable and can be one of three possible lengths depending on the number of 1's representing set or otherwise asserted bits in the quick paging block.

[0069] In one embodiment, quick paging block compression module 312 generates the compressed quick paging block by sequentially indicating the position of each set bit in the quick paging block. The quick paging block compression module 312 can represent the position with a $\lceil \log_2(N_{QP_BLK}) \rceil$ bit field, where the value of the field indicates the set bit position. The quick paging block compression module 312 may also reserve one or more values for the bit position field that represent special cases. For example, a value of 0 indicates no further bits asserted in the quick paging block. Additionally, a value of $2^{(N_{QP_BLK_COMP})}-1$ indicates that greater than some predetermined number of quick paging bits, e.g. 5 bits, are set in the quick paging block.

[0070] Thus, in this embodiment, the total number of unique bits in the Quick paging block is limited to $N_{QP_BLK} - 2$ to account for the 2 reserved values. Allowable bit positions may be in the range approximately 1 to $N_{QP_BLK} - 2$. If greater than the predetermined number of bits, e.g. 5 bits, are set in the quick paging block, the access network may interpret the message as having all bits set to one, and may transmit a single field with the corresponding reserved value. In one embodiment, the quick paging block compression module 312 does not include any field in the quick paging block that is indicative of the number of pages or number of bits included in the quick paging block. Instead, the transmitter 300 can rely on a receiver determining the number of pages and the number of bits in the quick paging block. For example, the receiver can test a number of hypotheses and thereby determine the number of bits in the quick paging block. In another embodiment, the quick paging block compression module 312 can include a field that is indicative of the number of quick pages or the number of bits in the compressed quick paging block. The receiver determines the number of quick pages or quick paging bits by extracting the appropriate field from the compressed quick paging block.

[0071] Table 1 shows the size of the compressed quick paging block as a function of the number of set bits in the quick paging block for the embodiment that does not include a field indicating the number of quick pages.

Table 1 Lengths of Compressed Quick Paging Block

Number of set bits in Quick Paging Block	$N_{QP_MSG_COMP}$
0, 1, or >5	$\lceil \log_2(N_{QP_BLK}) \rceil$ bits
2 or 3	$3\lceil \log_2(N_{QP_BLK}) \rceil$ bits
4 or 5	$5\lceil \log_2(N_{QP_BLK}) \rceil$ bits

[0072] The output of the quick paging block compression module 312 is coupled to the aggregator 330. In the embodiment in which the quick paging block compression module 312 is omitted, the quick paging block from the quick paging block generator 310 is coupled to the aggregator 330.

[0073] The load control block module 320 concurrently generates a load control block having one or more bits. In one embodiment, the load control block is N_{LC_BLK} bits in length and is set by the access network. The load control block can represent any additional information that is directed to one or more access terminals as part of the quick paging channel information. The load control information can be virtually any type of information. For example, the load control information can indicate a class of access terminals that are permitted to access the quick paging information. Alternatively, the load control information can indicate a class of access terminals from which the quick paging information is applicable. Access terminals not belonging to the class indicated by the load control block information can ignore the message.

[0074] The aggregator 330 operates to concatenate the compressed quick paging block or the quick paging block with the load control block. In this embodiment, a QPCH packet carries two information blocks: the quick paging block and the load control block. The aggregator 330 can append the load control block to the end of the quick paging or compressed quick paging block.

[0075] The aggregator 330 couples the concatenated quick paging and load control blocks to the encoder 340. The encoder 340 operates to encode the concatenated information. The encoder 340 can implement virtually any type of encoding, and can implement, for example, systematic encoding, block coding, convolutional encoding,

turbo encoding, and the like, or some combination thereof. The output of the encoder 340 represents the quick paging packet.

[0076] The QPCH packet may be encoded, channel interleaved, repeated, data-scrambled and modulated using any one or multiple techniques. In an embodiment, a MACID of 0 and a packet format of 0 may be used to generate an initial state of a scrambler (not shown).

[0077] In one embodiment, the encoder 340 implements a systematic code, such that the redundant bits are appended to the end of the unmodified concatenated quick paging and load control blocks. A systematic code can generate, for example, a Cyclic Redundancy Code (CRC), a syndrome, a parity bit, or some other code bits that provide a level of redundancy.

[0078] The encoder 340 couples the encoded QPCH packet to the TX MIMO Processor 220. In one embodiment, the TX MIMO Processor 220 processes the encoded QPCH packet and produces an OFDM symbol having the complete QPCH packet information. The TX MIMO Processor 220 can generate the OFDM symbol allocating the QPCH packet information across all of the OFDM subcarriers, or across a predetermined subset of all of the subcarriers. In such an embodiment, the symbol having the QPCH packet is time division multiplexed with other channels in the OFDM system.

[0079] In some embodiments, the TX MIMO Processor 220 may be able to modulate the QPCH packet onto the subcarriers using any one of a predetermined set of modulation types. In one embodiment , the TX MIMO Processor 220 uses QPSK modulation for all the modulation symbols of the QPCH. In other embodiments, the TX MIMO Processor 220 may use some other type of modulation, such as BPSK.

[0080] In another embodiment, the QPCH packet information is allocated to a logical channel that is mapped to fewer than all of the subcarriers in the OFDM system. In such an embodiment, the logical channel to physical subcarrier mapping can be static or can be dynamic.

[0081] If the multiple access wireless communication system employs frequency hopping (FH), the QPCH can be assigned as a logical channel, sometimes referred to as a hop port, and the logical channel can be mapped to physical channels according to a

predetermined frequency hopping algorithm. Thus, in a frequency hopping OFDMA system , the physical subcarrier frequencies assigned to the logical channels change over time. For example, the frequency hopping algorithm can periodically update the logical channel to physical subcarrier mapping, for example, each OFDM symbol, each slot, or following some other predetermined number of OFDM symbols.

[0082] The TX MIMO Processor 220 couples the OFDM symbol to the transmitter stage 222. The transmitter stage 222 transmits the symbol including the QPCH packet using the antenna 224.

[0083] In the QPCH embodiments described above, the transmitter broadcasts the QPCH packet in n OFDM symbol occurring during a preamble portion of a superframe. The transmitter broadcasts the QPCH packet to all of the access terminals in the coverage area.

[0084] By transmitting the QPCH symbol in a preamble, a large number of access terminals may be addressed simultaneously. This is because, for example, each data bit in the QPCH packet may be addressed to a different mobile. The transmission of the QPCH in a single OFDM symbol allows several access terminals to wakeup concurrently to monitor their respective quick paging bits in the same OFDM symbol.

[0085] Further, all the bits in one TDM slot are jointly encoded and can be encoded with a strong CRC, where a strong CRC refers to redundant coding bits that provide a high probability of successful receipt of any particular quick paging bit in the packet. This has two advantages,. First, the coding gain due to joint encoding provides additional margin not available using a single bit. Second, because of the strong CRC, the probability of a missed page becomes very low.

[0086] Figure 4 is a simplified functional block diagram of an embodiment of a receiver 400 configured to process the jointly encoded QPCH packet. The receiver 400 can be a portion of each of the access terminals of Figure 1, and can be a portion of the receiver system of Figure 2. The simplified functional block diagram of Figure 4 illustrates only those portions of the receiver 400 associated with processing the QPCH packet. The receiver 400 typically includes other processing modules.

[0087] The receiver 400 operates to perform roughly the complement of the process used in the transmitter system to generate the QPCH packet. The receiver 400 receives

the OFDM symbol containing the QPCH packet and recovers the QPCH packet. The receiver 400 uses the redundant encoding information to increase the probability that the underlying bits in the quick paging block and load control block are successfully recovered. The receiver 400 uses the recovered quick paging bit information to determine whether to awaken or remain active to monitor for a subsequent paging channel message.

[0088] In one embodiment, if the CRC fails, the access terminal monitors the paging channel as a default action. If the CRC succeeds and a corresponding quick paging bit is set, the access terminal is instructed to monitor the paging channel. If the CRC succeeds, and the assigned quick paging bit is 0, or otherwise unasserted, the access terminal returns to a sleep state. The probability of misdetection is equal to the probability of misdetecting a CRC error, and that probability is very low with a strong CRC, such as a CRC having 8 or more bits.

[0089] The receiver 400 includes an antenna 252 that couples a received signal to a receiver front end 254. A synchronization module 410 operates in conjunction with the receiver front end. The synchronization module 410 determines, based on the received signal, the symbol timing and from the symbol timing the frame and superframe timing. The receiver front end 254 utilizes the synchronization information to recover the OFDM symbols, and in particular, the OFDM preamble having the OFDM symbol with the QPCH packet.

[0090] The receiver front end 254 couples the OFDM symbol having the QPCH packet to the RX MIMO data processor 260. The RX MIMO data processor 260 operates to demodulate the OFDM subcarriers on which the QPCH packet is modulated to recover the QPCH packet.

[0091] The RX MIMO data processor 260 demodulates the subcarriers in a complementary manner to which they were modulated. That is, if the subcarriers are QPSK modulated, the RX MIMO data processor 260 performs QPSK demodulation of the subcarriers.

[0092] The QPCH packet is coupled to the QPCH decoder 420. The QPCH decoder 420 operates to decode the QPCH packet in a complementary fashion to the manner in which the packet was encoded in transmitter. In general, the QPCH decoder 420

performs the complement of the processing performed in the transmitter, including the complement of any interleaving, encoding, scrambling, repetition, and the like or combination thereof performed when generating the QPCH packet.

[0093] If the QPCH is encoded with a systematic code, the receiver 400 can conditionally process the redundant coding bits based on the value of the associated quick paging bit. For example, the receiver 400 can decide not to process the coding bits if the associated quick paging bit. In such an embodiment, the receiver 400 can trade-off the processing energy associated with the decoding process for the probability of processing a false asserted bit. In other embodiments, the receiver can be configured to always examine the coding bits, such as the CRC or other redundant bits. In such an embodiment, the decoder 420 can operate to identify a presence of a received bit error, and in some instances, can identify the one or more erroneous received bits. The decoder 420can then operate to correct the identified erroneous bits.

[0094] The output of the decoder 420 or a portion of the QPCH packet can optionally be coupled to a quick paging block decompression module 430. In the embodiment in which the QPCH includes a compressed quick paging block and a load control block, the decoder 420 can couple at least the compressed quick paging block to the quick paging block decompression module 430, and need not couple any of the bits from the load control block to the decompression module.

[0095] The quick paging block decompression module 430 operates to decompress the compressed quick paging block in a manner that is complementary to the process used to compress the quick paging block. In the embodiment described above, where the quick paging block is compressed by including the positions of up to a predetermined number of quick paging bits, the quick paging block decompression module 430 operates to initially determine the number of asserted quick paging bits represented in the compressed quick paging block. The quick paging block decompression module 430 can determine the length of the compressed quick paging block and can then recover each of the positions of any asserted quick paging bits.

[0096] The quick paging block decompression module 430 can recover the quick paging block and output the quick paging block. A subsequent module such as a paging

module (not shown) can examine the quick paging block to determine if the quick paging block assigned to the access terminal is asserted.

[0097] In another embodiment, the quick paging block decompression module 430 can examine the positions of the asserted bits in the compressed quick paging block to determine whether the quick paging bit associated with the access terminal is asserted. In this embodiment, the quick paging block decompression module 430 is not required to actually recover the quick paging block.

[0098] Other modules within the receiver 400 such as the paging module (not shown) can operate on the quick paging block information. If the quick paging bit associated with the access terminal is asserted, the paging module can direct the receiver to monitor for the paging message. Alternatively, if the quick paging bit associated with the access terminal is not asserted, the paging module can direct the receiver to transition to a sleep state until the next occurrence of the QPCH.

[0099] Figure 5 is a simplified flowchart of an embodiment of a method 500 of generating a quick paging block having one or more asserted quick paging bits for notifying an access terminal of a paging message. The method 500 can be implemented, for example, in an access point of Figure 1. More particularly, the method 500 can be implemented, for example, by the transmitter system of Figure 2 or transmitter of Figure 3.

[0100] The method 500 begins at block 510 where the transmitter in an access point determines the number and identity of the access terminals scheduled to receive paging messages. Typically, the scheduled access terminals are those access terminals presently in an idle or sleep state for which a communication link is desired and there is presently scheduled a paging message that has yet to be sent or for which a prior paging message has yet to by acknowledged.

[0101] The transmitter proceeds to block 520 to determine the status of the quick paging bits in a quick paging block based on the scheduled paging messages. The transmitter can be configured to set or otherwise assert the quick paging bits associated with the one or more access terminals scheduled to receive a paging message. Additionally, the transmitter can be configured to clear or otherwise de-assert the quick paging bits associated with those access terminals for which no paging message is

scheduled. In one embodiment, the bit values may be determined by using an Idle State Protocol in a Connection Layer.

[0102] The transmitter proceeds to block 530 and generates a quick paging block having the quick paging bits associated with the scheduled access terminals asserted and all other quick paging bits de-asserted. After generating the quick paging block, the transmitter optionally proceeds to block 540 and compresses the quick paging block to generate the compressed quick paging block. In some embodiments, the transmitter does not compress the quick paging block.

[0103] The transmitter proceeds to block 550 and aggregates the compressed quick paging block with other information that is sent over the QPCH. In one embodiment, the transmitter appends a load control block to the quick paging block, which is either compressed or uncompressed, depending on the embodiment. In other embodiments, the transmitter may append or prepend other information to the quick paging block.

[0104] The transmitter proceeds to block 560 and encodes the QPCH information. The encoder operates on the quick paging block and additional information. Therefore, the encoding of the quick paging bits is performed jointly. Quick paging bits are encode with other quick paging bits as well as other information, such as the load control block. The encoded output represents the QPCH packet.

[0105] The transmitter proceeds to block 570 and schedules the QPCH packet for transmission. In one embodiment, the transmitter schedules the QPCH packet to be transmitted in a symbol from a plurality of OFDM symbols in a superframe preamble. If the QPCH packet occupies the information carrying subcarriers of the OFDM system, all of the other channels, including traffic channels and other overhead channels, in the system are time domain multiplexed with the QPCH. Similarly, if the QPCH occupies only a subset of information carrying subcarriers in the OFDM system, at least a portion of other channels are time domain multiplexed with the QPCH, provided the subcarriers are not dedicated to the QPCH.

[0106] The transmitter proceeds to block 580 and maps the QPCH packet to an OFDM symbol at the appropriate time determined by the schedule. In one embodiment, the OFDM symbol is a symbol in the first six preamble symbols occurring in a superframe. Of course, other embodiments can have other symbol positions.

[0107] The transmitter can modulate the QPCH packet onto the subcarriers using a predetermined modulation type. The modulation type can be selected to be a modulation type that is relatively noise insensitive, while supporting a modest information throughput. In one embodiment, the transmitter QPSK modulates the QPCH packet onto the subcarriers of the OFDM symbol.

[0108] After generating the OFDM symbol, the transmitter proceeds to block 590 and transmits the OFDM symbol including the QPCH packet. The transmitter can, for example, frequency convert the OFDM symbol to a desired RF operating band and wirelessly transmit the OFDM symbol in the RF operating band.

[0109] Figure 6 is a simplified flowchart of an embodiment of a method 600 of processing a quick paging block. The method 600 can be implemented, for example, in an access terminal of Figure 1, a receiver system of Figure 2, or a receiver of Figure 3. In general, the method 600 of Figure 6 operates as a complement to the QPCH generating method of Figure 5.

[0110] The method 600 begins a block 610 where the receiver receives one or more OFDM symbols. At least one symbol may include the QPCH packet. For example, in the method of Figure 5, the QPCH packet can be contained within a single OFDM symbol. In one embodiment, the receiver synchronizes with a superframe timing and extracts at least the OFDM symbol associated with the QPCH packet.

[0111] The receiver proceeds to block 620 and recovers the QPCH packet from the appropriate OFDM symbols. In one embodiment, the receiver demodulates the subcarriers of the OFDM symbol and recovers the QPCH packet information.

[0112] The receiver proceeds to block 630 and decodes the QPCH packet to determine the presence of errors, if any. Depending on the type of encoding used to generate the QPCH packet, the receiver may have the ability to correct one or more errors in the QPCH packet as a result of the decoding process. The receiver also performs the complement of any coding operation such as those that operate to scramble, interleave, repeat, or otherwise process the QPCH block information.

[0113] The receiver optionally proceeds to block 640 and decompresses the quick paging block portion of the QPCH packet. In one embodiment, the receiver determines

the length of a variable length quick paging block and decompresses the variable length compressed quick paging block.

[0114] The receiver proceeds to block 650 and determines the status of the quick paging bits to determine if the quick paging bit associated with the receiver, or access terminal having the receiver, is asserted. The process of decompressing the quick paging block can be optional, depending on the manner in which the block is compressed. In the embodiment in which the quick paging block is compressed by indicating the position of the asserted quick paging bits, the receiver can determine if the associated quick paging bit is asserted without needing to recover the uncompressed quick paging block.

[0115] After the receiver determines the state of the associated quick paging bit, the receiver proceeds to block 660 to direct the operation of the receiver based on the status f the bit. If the associated quick paging bit is asserted, the receiver can monitor a paging channel at an appropriate time for a paging message. If the receiver determines that the associated quick paging bit is not asserted, the receiver may transition to a sleep state until the next scheduled QPCH packet.

[0116] Figure 7 is a simplified functional block diagram of an embodiment of a transmitter 700 implementing the quick paging block. The transmitter 700 includes means for synchronizing timing with a system time 702 that is coupled to a means for scheduling information 704 according to the means for synchronizing timing 702. The means for scheduling information 704 can be configured to determine which of a plurality of access terminals has paging messages scheduled for transmission.

[0117] The means for scheduling information 704 is coupled to a means for generating a QPCH block 710 that is configured to generate a quick paging block based on the scheduled paging channel transmissions. The means for scheduling information 704 operates as a means for determining a presence of a scheduled message for an access terminal. The means for generating a QPCH block 710 is configured as a means for setting a quick paging bit from a plurality of quick paging bits in a quick paging block. The means for generating a QPCH block 710 sets the quick paging bit corresponding to the access terminal having a scheduled message. The means for

generating a QPCH block 710 couples the quick paging block to a means for aggregating information 730.

[0118] A means for generating additional information 720 is configured to generate one or more bits, blocks, or fields of information that is to be included with the QPCH packet. The means for generating additional information 720 couples the additional information to the means for aggregating information 730.

[0119] The means for aggregating information 730 operates to combine, aggregate, or otherwise concatenate the quick paging block with the additional information. In one embodiment, a load control block is concatenated with the quick paging block to generate a QPCH packet that is a concatenation of the quick paging block and the load control block.

[0120] The output of the means for aggregating information 730 is coupled to a means for encoding the QPCH packet 740 that operates to encode the concatenated QPCH packet. The means for encoding the QPCH packet 740 encodes a quick paging block and generates an encoded quick paging packet. That is, the means for encoding the QPCH packet 740 jopintly encodes each quick paging bit with at least one additional quick paging bit corresponding to a distinct access terminal. The means for encoding the QPCH packet 740 couples the encoded QPCH packet to a means for TX processing 750, which may be for TX MIMO processing depending on the system. The means for TX processing 750 operates to generate at least one OFDM symbol having at least a portion of the encoded QPCH packet. The means for TX processing 750 produces at least one OFDM symbol from a stream of OFDM symbols, and thus time division multiplexes the encoded quick paging packet having the quick paging block with distinct information over a channel. The output of the means for TX processing 750 is coupled to a means for transmitting 760 that operates to process the at least one OFDM symbol to an RF frequency for transmission using the antenna 762.

[0121] As seen in Figure 7, means 702, 704, 712, 720, and 750 are optional and may be omitted based upon the application and system design.

[0122] Figure 8 is a simplified functional block diagram of an embodiment of a receiver 800 configured to process the quick paging block. The receiver 800 includes an antenna 852 configured to receive the OFDM symbol having the QPCH packet.

[0123] The antenna couples the OFDM symbol to a means for receiving the OFDM information 854 that is configured to receive a quick paging packet and process the received OFDM symbols to baseband OFDM symbols or samples. A means for synchronizing timing 810 operates to synchronize the received samples to align with the OFDM symbol timing.

[0124] The output of the means for receiving the OFDM information 854 is coupled to a means for RX MIMO Processing 860 that is configured to process the OFDM symbol to recover the underlying information modulated on the OFDM subcarriers. For the OFDM symbol having the QPCH packet, the means for RX MIMO Processing 860 demodulates the OFDM subcarriers to recover the encoded QPCH packet.

[0125] The means for RX MIMO Processing 860 couples the encoded QPCH packet to a means for decoding the QPCH packet 820 that is configured to decode the encoded QPCH packet in order to recover the QPCH packet including the quick paging block. The output of the means for decoding the QPCH packet 820 is optionally coupled to a means for decompressing the QPCH block 830 of the QPCH packet in order to determine which of the quick paging bits is asserted. The means for decompressing the QPCH block 830 can also operate as a means for determining a status of a quick paging bit associated with a particular access terminal based on the output of the decompressing process. The receiver can determine what action to take based on the state of the associated quick paging bit.

[0126] A quick paging channel format and quick paging channel packet, and process for generating the quick paging packet have been described herein. A jointly encoded quick paging packet allows redundant bits to be generated to assist in the accurate recovery of the quick paging bits at a wireless receiver. The improved ability to accurately recover the quick paging bits reduces the probability of missing a paging message directed to the receiver.

[0127] As used herein, the term coupled or connected is used to mean an indirect coupling as well as a direct coupling or connection. Where two or more blocks, modules, devices, or apparatus are coupled, there may be one or more intervening blocks between the two coupled blocks.

[0128] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), a Reduced Instruction Set Computer (RISC) processor, an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, for example, a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0129] For a firmware and/or software implementation, the techniques described herein may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. The firmware and/or software codes may be stored in a memory and executed by a processor. The memory may be implemented within the processor or external to the processor.

[0130] The steps of a method, process, or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. The various steps or acts in a method or process may be performed in the order shown, or may be performed in another order. Additionally, one or more process or method steps may be omitted or one or more process or method steps may be added to the methods and processes. An additional step, block, or action may be added in the beginning, end, or intervening existing elements of the methods and processes.

[0131] The above description of the disclosed embodiments is provided to enable any person of ordinary skill in the art to make or use the disclosure. Various modifications to these embodiments will be readily apparent to those of ordinary skill in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

1. A method of notifying an access terminal, the method comprising:

determining presence of a scheduled message for the access terminal;

setting a quick paging bit from a plurality of quick paging bits in a quick paging block, the quick paging bit corresponding to the access terminal;

encoding the quick paging block to generate an encoded quick paging packet;

generating at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block; and

transmitting the at least one OFDM symbol.

2. The method of claim 1, wherein the generating the at least one OFDM symbol comprises generating at least one OFDM symbol having an entire encoded quick paging block.

3. The method of claim 1, further comprising:

generating additional bits distinct from the quick paging block; and

appending the additional bits to the quick paging block prior to encoding the quick paging block.

4. The method of claim 1, further comprising:

compressing the quick paging block to generate a compressed quick paging block; and

wherein encoding the quick paging block comprises encoding the compressed quick paging block.

5. The method of claim 4, wherein compressing the quick paging block comprises:

determining a number of asserted quick paging bits from the plurality of quick paging bits; and

generating successive fields indicating positions of the asserted quick paging bits within the quick paging block if the number of asserted bits is less than a predetermined amount.

6. The method of claim 4, wherein compressing the quick paging block comprises:

determining a number of asserted quick paging bits from the plurality of quick paging bits; and

generating a predetermined value representative of the quick paging block if the number of asserted quick paging bits is greater than a predetermined amount.

7. The method of claim 1, wherein encoding the quick paging block comprises systematic encoding the quick paging block.

8. The method of claim 1, wherein encoding the quick paging block comprises generating a Cyclic Redundancy Code of a packet including the quick paging block.

9. The method of claim 1, wherein transmitting the at least one OFDM symbol comprises time division multiplexing the at least one OFDM symbol with other information over at least one channel.

10. The method of claim 1, wherein transmitting the at least one OFDM symbol comprises transmitting the at least one OFDM symbol during a superframe preamble.

11. A method of notifying an access terminal, the method comprising:

setting a quick paging bit corresponding to the access terminal in a quick paging block having a plurality of bits corresponding to a plurality of access terminals;

compressing the quick paging block to generate a compressed quick paging block; and

encoding the compressed quick paging block to generate an encoded quick paging block.

12. The method of claim 11, further comprising time division multiplexing the encoded quick paging block with other information over at least one channel of a wireless communication system.

13. The method of claim 11, further comprising:

generating an Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block; and

transmitting the OFDM symbol.

14. The method of claim 13, wherein generating the OFDM symbol comprises modulating at least a portion of the encoded quick paging block onto substantially all signal carrying subcarriers of the OFDM symbol.

15. The method of claim 13, wherein generating the OFDM symbol comprises Quadrature Phase Shift Keying (QPSK) modulating at least a portion of the encoded quick paging block onto at least a subset of subcarriers of the OFDM symbol.

16. A method of processing a quick paging message, the method comprising:

receiving a quick paging packet;

decoding the quick paging packet to generate a quick paging block;

decompressing the quick paging block; and

determining a status of a quick paging bit associated with an access terminal based on an output of the decompressing process.

17. The method of claim 16, wherein receiving the quick paging packet comprises receiving the quick paging packet including the quick paging block and a load control block.

18. The method of claim 16, wherein receiving the quick paging packet comprises receiving an Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the quick paging packet.

19. The method of claim 16, wherein determining the status of the quick paging bit comprises:

determining a position of an asserted bit in the quick paging block based on an output of the decompressing process; and

comparing the position to a position of the quick paging bit associated with the access terminal.

20. An apparatus for generating a quick paging message, the system comprising:

a scheduler configured to determine scheduled a paging message for an access terminal;

a quick paging block generator coupled to the scheduler and configured to assert a quick paging bit corresponding to the access terminal and configured to generate a quick paging block having at least the quick paging bit and a distinct quick paging bit corresponding to a distinct access terminal;

an encoder coupled to the quick paging block generator and configured to generate an encoded quick paging packet based on the quick paging block; and

a transmit processor coupled to the encoder and configured to generate at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging packet.

21. The apparatus of claim 20, further comprising:

a compression block coupled to the quick paging block generator and configured to compress the quick paging block and generate a compressed quick paging block; and

wherein the encoder is coupled to the compression block and is configured to generate the encoded quick paging packet based on the compressed quick paging block.

22. The apparatus of claim 20, further comprising:

a load control module configure to generate load control block having at least one bit distinct from a quick paging bit;

an aggregator coupled to the quick paging block generator and the load control block and configured to aggregate the quick paging block with the load control block; and

wherein the encoder is configured to encode an aggregated output of the aggregator.

23. The system of claim 20, further comprising a transmitter coupled to the transmit processor and configured to transmit the at least one OFDM symbol during a superframe preamble.

24. The system of claim 20, further comprising a transmitter coupled to the encoder and configured to time division multiplex the encoded quick paging packet over at least one channel with other information.

25. An apparatus for notifying an access terminal, the system comprising:

means for determining presence of a scheduled message for the access terminal;

means for setting a quick paging bit from a plurality of quick paging bits in a quick paging block, the quick paging bit corresponding to the access terminal;

means for encoding the quick paging block to generate an encoded quick paging packet;

means for generating at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block; and

means for transmitting the at least one OFDM symbol.

26. The apparatus of claim 25, wherein the means for generating the at least one OFDM symbol comprises means for generating at least one OFDM symbol having an entire encoded quick paging block.

27. The apparatus of claim 25, further comprising:

means for generating additional bits distinct from the quick paging block; and

means for appending the additional bits to the quick paging block prior to encoding the quick paging block.

28. The apparatus of claim 25, further comprising:

means for compressing the quick paging block to generate a compressed quick paging block; and

wherein the means for encoding the quick paging block comprises means for encoding the compressed quick paging block.

29. The method of claim 28, wherein the means for compressing the quick paging block comprises:

means for determining a number of asserted quick paging bits from the plurality of quick paging bits; and

generating successive fields indicating positions of the asserted quick paging bits within the quick paging block if the number of asserted bits is less than a predetermined amount.

30. The method of claim 28, wherein the means for compressing the quick paging block comprises:

means for determining a number of asserted quick paging bits from the plurality of quick paging bits; and

means for generating a predetermined value representative of the quick paging block if the number of asserted quick paging bits is greater than a predetermined amount.

31. An apparatus for notifying an access terminal, the system comprising:

means for setting a quick paging bit corresponding to the access terminal;

means for jointly encoding the quick paging bit with at least one additional quick paging bit corresponding to a distinct access terminal to generate an encoded quick paging block; and

means for time division multiplexing the encoded quick paging block with distinct information over a channel.

32. The apparatus of claim 31, further comprising means for time division multiplexing the encoded quick paging block with other information over at least one channel of a wireless communication system.

33. The apparatus of claim 31, further comprising:

means for generating at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block.

34. The apparatus of claim 33, wherein the means for generating the at least one OFDM symbol comprises modulating at least a portion of the encoded quick paging block onto substantially all signal carrying subcarriers of the at least one OFDM symbol.

35. The apparatus of claim 33, wherein generating the at least one OFDM symbol comprises Quadrature Phase Shift Keying (QPSK) modulating at least a portion of the encoded quick paging block onto at least a subset of subcarriers of the at least one OFDM symbol.

36. An apparatus for processing a quick paging message, the system comprising:

means for receiving a quick paging packet;

means for decoding the quick paging packet to generate a quick paging block;

means for decompressing the quick paging block; and

means for determining a status of a quick paging bit associated with an access terminal based on an output of the decompressing process.

37. The apparatus of claim 36, wherein the means for receiving the quick paging packet comprises means for receiving the quick paging packet including the quick paging block and a load control block.

38. The apparatus of claim 36, wherein the means for receiving the quick paging packet comprises means for receiving at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the quick paging packet.

39. The apparatus of claim 36, wherein the means for determining the status of the quick paging bit comprises:

means for determining a position of an asserted bit in the quick paging block based on an output of the decompressing process; and

means for comparing the position to a position of the quick paging bit associated with the access terminal.

40. A processor readable media including instructions that may be utilized by one or more processors, the instructions comprising:

instructions for determining presence of a scheduled message for the access terminal;

instructions for setting a quick paging bit from a plurality of quick paging bits in a quick paging block, the quick paging bit corresponding to the access terminal;

instructions for encoding the quick paging block to generate an encoded quick paging packet;

instructions for generating at least one Orthogonal Frequency Division Multiplex (OFDM) symbol having at least a portion of the encoded quick paging block; and

instructions for transmitting the at least one OFDM symbol.

41. The processor readable media of claim 41, the instructions further comprising:

instructions for compressing the quick paging block to generate a compressed quick paging block.

42. A processor readable media including instructions that may be utilized by one or more processors, the instructions comprising:

instructions for setting a quick paging bit corresponding to the access terminal in a quick paging block having a plurality of bits corresponding to a plurality of access terminals;

instructions for compressing the quick paging block to generate a compressed quick paging block; and

instructions for encoding the compressed quick paging block to generate an encoded quick paging block.

43. A processor readable media including instructions that may be utilized by one or more processors, the instructions comprising:

instructions for processing a quick paging packet;

instructions for decoding the quick paging packet to generate a quick paging block;

instructions for decompressing the quick paging block; and

instructions for determining a status of a quick paging bit associated with an access terminal based on an output of the decompressing process.

44. The processor readable media of claim 41, the instructions further comprising:

instructions for determining a position of an asserted bit in the quick paging block based on an output of the decompressing process; and

instructions for comparing the position to a position of the quick paging bit associated with the access terminal.