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PROCESS FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

The present invention relates to a process for manufacturing a semiconductor integrated circuit, and is particular to a process involving the formation of isolating regions for isolating elements of the device.

It is known to isolate elements in semiconductor integrated circuit devices by a method known as pn junction isolation, which uses diffusion layers, or by a method known as oxidation film isolation, which uses local oxidation films formed over the surface of the substrate. The widths of the isolation regions formed by such isolation methods, are relatively wide. Therefore, as the size of the elements becomes smaller, the isolation regions occupy proportionally larger areas. This makes it difficult to obtain large-scale integrated circuits (LSI circuits) in a very densely integrated form. The applicants have therefore proposed an isolation technique called U-groove isolation in which portions that act as isolation regions between active regions of elements are cut to form U-shaped grooves (moats or trenches, hereinafter referred to as U-grooves). A silicon dioxide film is formed within the U-grooves which are then filled with polycrystalline silicon. These form element-isolating regions.

This technique has been disclosed in, for

example, the journal "NIKKEI ELECTRONICS", March 29, 1982, No. 287, pp. 90-101.

Bipolar transistors are the main elements in the construction of a bipolar type of semiconductor integrated circuit device. However, bipolar transistors must be isolated from each other by U-grooves when they are very densely arranged on a semiconductor substrate.

To reduce the size of a bipolar transistor, however, an n^+-type semiconductor region that acts as a collector contact region must be isolated by an insulating material from a p^+-type base region.

The inventors have discovered that a problem arises when an attempt is made to satisfy these two requirements simultaneously.

When deep U-grooves isolating individual transistors and shallow U-grooves isolating each base region and collector region are used, the manufacturing process is complicated, and increased collector resistance makes the switching speed drop.

When U-grooves are used to isolate individual transistors, and when a field oxide film is used to isolate each base region and collector region, the breakdown voltage at the pn junction between the base region and the collector region drops due to "bird's beaks" formed in the field oxide film.

The object of the present invention is to

increase the degree of integration of bipolar semiconductor integrated circuit devices, without impairing their electrical characteristics.

According to the present invention, there is provided a process for manufacturing a semiconductor integrated circuit, comprising:

forming a semiconductor body having a substrate of a first conductivity type, a buried layer of second conductivity type, and an epitaxial layer of the second conductivity type;

forming a silicon oxide film on the body, the silicon oxide film having a first part and a second part, the first part having a greater thickness than the second;

forming grooves in the semiconductor body, those grooves extending through the oxide film the epitaxial and buried layers to the substrate, thereby to divide the epitaxial and buried layers into a plurality of isolated regions;

simultaneously forming further silicon oxide films on the surface of the semiconductor body, the further silicon oxide films including a first further film within the grooves and a second further film in the second part of the first oxide film and of greater thickness than the second part of the oxide film on a part of the surface of at least one isolated region, such that the surface of the epitaxial layer of the or each such isolated region is divided into a first and a second part by the

second further film;

forming isolation materials in the grooves; and

forming a semiconductor element in at least some of the isolated regions, the semiconductor element including a base region in the first part of the epitaxial layer and a collector region in the second part of the epitaxial layer.

In this way it becomes possible to provide a semiconductor integrated circuit device, in which semiconductor regions that act as collector contact regions and base regions are sufficiently isolated from each other, without increasing the number of processing steps.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figs. 1, 2, 4 to 6, and 8 to 16 are cross-sectional views showing various steps in the manufacture of a bipolar type semiconductor integrated circuit device according to the present invention;

Fig. 3 is a plan view of the bipolar type semiconductor integrated circuit device during the step corresponding to Fig. 4, the section of Fig. 4 being along the line A-A in Fig. 3; and

Fig. 7 is a plan view of the device during the step corresponding to Figs. 8 and 9, the section of Fig. 8 being along the line B-B in Fig. 7 and the section of Fig. 9 being along the line C-C.

Figs. 1 to 16 illustrate an embodiment of the

present invention being a bipolar type of semiconductor integrated circuit device. The figures illustrate the sequence of steps in the manufacture of the device.

According to this embodiment, it is necessary first to form a semiconductor body 24. Holes for the formation of buried layers are formed at suitable positions in a silicon oxide film formed over a semiconductor substrate 1 which consists of p-type monocrystalline silicon. Using the silicon oxide film

as a mask, n-type impurities are thermally diffused into the substrate 1 to form a local n^+-type buried layer 2. After the silicon oxide film is removed, an n^--type epitaxial layer 3 is grown onto the substrate 1 by a vapour growth method, and the resultant structure forms the semiconductor body 24.

A silicon oxide film (SiO_2 film) 4 and a silicon nitride film (Si_3N_4 film) 5 are formed on a main surface of the semiconductor body 24.

The silicon nitride film 5 is removed from portions where wiring will be formed, around the periphery of the chip. Using the silicon nitride film 5 as a mask, the main surface of the substrate 1 is cut by e.g. a conventional isoplanar technique, followed by thermal oxidation, to form a field oxide film 6 of a thickness of between 1μm to 1.2μm, as shown in Fig. 1. Since the field oxide film 6 is so thick, it is possible to reduce the electrostatic capacity of the wiring provided in the wiring regions.

The silicon nitride film 5 is removed, and another silicon nitride film 25 is formed over the whole surface of the semiconductor body 24.

The silicon nitride film 25 is etched to remove it from portions at which isolation regions will be formed, i.e., from the peripheries of bipolar transistors and from regions between the base region and the collector contact region of each transistor.

Using the silicon nitride film 25 as a mask, the surface of the semiconductor body 24 is locally oxidized by heating. Silicon oxide films 26a, 26b with a thickness between 300 mm and 350 mm are then formed over the portions at which the isolation regions will be formed, as shown in Fig. 2. The isolation region, base region, collector contact region, and the isolation region between the base region and the collector contact region are defined by the silicon nitride film 25.

The region between the base region and the collector contact region is covered with a photoresist film 27 and the exposed oxide films 26a are then removed by wet etching. The silicon oxide film 26b is left between the base region and the collector contact region, and is used as a mask for the etching of the semiconductor body 24 and for the implantation of ions. After the photoresist film 27 is removed, the openings of the grooves are tapered, as shown in Figs. 3 and 4, by etching with hydrazine. The silicon oxide film 26b is not etched by the hydrazine. If the surface of the semiconductor body 24 has been sufficiently tapered after the silicon oxide films 26a have been removed, etching with hydrazine is not necessary.

4 μm deep grooves 7 are formed by dry etching using the silicon nitride film 25 and silicon oxide

film 26b as masks so that the grooves 7 extend into the semiconductor body 24 as far as the substrate 1, as shown in Fig. 5. The etching reduces the thickness of the silicon oxide film 26b to about 200 mm.

Using the silicon nitride film 25 and silicon oxide film 26b as masks, boron ions are implanted into the bases of the U-grooves 7, and p^+-type channel-stopper layers 8 shown in Fig. 6 are then formed by heat treatment. The boron ions are not introduced into the surface of the semiconductor substrate 24 in the regions where the silicon oxide film 26b has been formed. The breakdown voltage at the pn junction between the base region and the collector region is increased by the introduction of the boron ions. If the silicon oxide film 26b is about 100 mm thick, it is capable of preventing the boron ions being introduced into the semiconductor body 24.

Using the silicon nitride film 25 as a mask, the surface of the semiconductor body 24 is thermally oxidized, which forms a silicon oxide film 9 of a thickness of about 600 mm in each U-groove 7. Since the nitride film 25 has been removed from the portion between the base region and the collector contact region, a relatively thick isolation oxide film 10 with a thickness between about 700 mm and 800 mm is formed at this portion. The thickness of the silicon oxide film increases since oxygen reaches the surface

of the semiconductor body 24 through the silicon oxide film 26b. The silicon oxide film 10 is thicker than the silicon oxide film 9 by the thickness of the silicon oxide film 26b.

The device in this state is shown in Figs. 7, 8 and 9, where Figs. 8 and 9 are sections taken along the lines B-B and C-C of Fig. 7, respectively. In Fig. 7, dot-dash lines 21a, 21b and 21c denote the positions of contact holes that will be formed in a subsequent step.

As shown in Fig. 9, the silicon oxide film 10 has end portions that continue from the silicon oxide film 9, at the same thickness, so that the base region and the collector contact region are reliably isolated from each other. No stress concentrations (which would generate crystal defects) occur at the boundaries between the U-grooves 7 and the silicon oxide film 10.

A silicon nitride film is deposited over the whole surface of the semiconductor body 24 by e.g. a CVD method, so that a silicon nitride film 11 is formed over the oxide film 9 within the U-grooves 7, as shown in Fig. 10.

Polycrystalline silicon is deposited thickly over the whole surface of the semiconductor substrate 24 by a CVD method, so that the U-grooves 7 are filled with polycrystalline silicon. The layer of polycrystalline

silicon on the surface of the substrate is removed by dry etching to flatten the surface, leaving polycrystalline silicon 12 within the U-grooves 7, as shown in Fig. 11.

Using the silicon nitride film 25 as a mask, the surface of the polycrystalline silicon 12 in each U-groove is thermally oxidized to form a silicon oxide film 13 with a thickness of 600 mm on top of the polycrystalline silicon 12. Then, as shown in Fig. 12, the silicon nitride film 25 is removed from the collector contact region. Using the silicon nitride film 25 as a mask, n-type impurities are implanted and are thermally diffused into the semiconductor body 24 to an n^+-type semiconductor region 14 that acts as a collector contact region.

The silicon nitride film 25 is removed using the silicon oxide film 13 as a mask, and p-type impurities are implanted into the whole main surface of the semiconductor body 24 to form a base region. A new silicon nitride film 15 is formed over the semiconductor body 24, and a p^+-type semiconductor region 16 that acts as a base region is formed by a heat treatment. Then, as shown in Fig. 13, the silicon nitride film 15 is removed from the portion that will be the emitter region.

The oxide film 4 is removed by etching from the surface of the portion that will be the emitter region,

and a thin layer of polycrystalline silicon is deposited over the whole surface of the semiconductor body 24 by a CVD method. N-type impurities such as arsenic ions are implanted into the polycrystalline silicon layer, and are then diffused from the polycrystalline silicon layer by a heat treatment to form an n^+-type semiconductor region 18 that acts as an emitter region. The majority of the polycrystalline silicon layer is thus removed by photolithography, the remaining polycrystalline silicon forming an electrode 19 on the emitter region 18. The resultant structure is shown in Fig. 14.

In this device, the emitter region 18 is formed by the diffusion of ions from the polycrystalline silicon layer. It is, however, also possible to implant ions and effect a heat treatment to form the emitter region prior to the deposition of the polycrystalline silicon. Alternatively, the emitter region can be formed by implanting and diffusing ions, and by making the ions diffuse from the polycrystalline silicon, before depositing the polycrystalline silicon.

A PSG film (phosphosilicate glass film) is formed over the semiconductor body 24 by a CVD method to form an intermediate insulation film 20. Using a photoresist film as a mask, contact holes 21a to 21c are formed through the intermediate insulation film 20, the silicon nitride film 15 and the silicon oxide film 4,

by etching, as shown in Fig. 15, to reach the base region, emitter region and collector region.

A wiring material such as aluminium is vapourized onto the whole surface of the semiconductor body 24, and aluminium electrodes 22a to 22c and aluminium wiring are formed by e.g. photolithography. A final passivation film 23, such as an SiO_2 film, is then formed over the device as shown in Fig. 16.

Fig. 16 shows only one bipolar transistor with an epitaxial layer 3 to its right instead of other transistors. This is also true for Figs. 12 to 15.

In this embodiment, the isolation oxide film 10 is formed between the collector contact region 14 and the base region 16, simultaneously with the formation of the silicon oxide film 9 in each U-groove isolation region. Therefore, no separate step is required for the formation of the isolation oxide film 10. Furthermore, when each collector contact region 14 and base region 16 are isolated from each other by a shallow U-groove, it is necessary to cut the U-grooves using two steps. In this embodiment, however, the U-grooves 7 may be formed by a single step, simplifying the manufacturing process.

The isolation oxide film 10 is formed simultaneously with the formation of the silicon oxide film 9, so that the isolation oxide film 10 is approximately uniform from the central portion to the edge

portions thereof, as shown in Fig. 9. On the other hand, when the silicon oxide film 9 and the isolation oxide film 10 are formed by separate steps, the boundaries between the edges of the oxide film 10 and the U-groove isolation regions 7 become so thin that there is a drop in the breakdown voltage at the junction between the base region and the collector region. According to the embodiment of the present invention described above, however, the breakdown voltage does not decrease but is kept sufficiently high.

It is easier to control the thickness of the oxide film 10 than the depth of the U-shape isolation regions, so that variations in the electrical characteristics of the transistors may be reduced. The method in which the collector contact region 14 is isolated by a U-groove isolation region from the base region 16 has the disadvantage that the collector resistance increases as the U-groove reaches the buried layer 3 through the epitaxial layer 2. When the U-groove is shallow, on the other hand, the breakdown voltage at the junction between the base region and the collector region drops. According to the embodiment of the present invention discussed above, however, the electrical characteristics of the transistors are greatly improved.

In this embodiment, the thick field oxide film

6 is formed over the regions where there are no transistors. A wiring layer, for instance, may be formed over the thick field oxide film 6, so that the regions covered by the field oxide film 6 may be used as wiring channels.

The emitter region 18 may be formed by implanting n-type impurities into the main surface of the substrate, without forming the polycrystalline silicon electrode 19, and the collector contact region can be formed after the base region and the emitter region have been formed.

The field oxide film 6 for the wiring region may be formed simultaneously with the formation of the silicon oxide film 9 in the U-groove, in the same way as the formation of the isolation oxide film 10.

An isolation oxide film (an insulating material providing isolation) is formed between the collector contact region and the base region simultaneously with the formation of an oxide film (insulating material) in the U-grooves used for isolation. Therefore, the isolation oxide film (the insulating material providing isolation) between the collector contact region and the thickness of the base region is nearly uniform from the central portion to the edge portions, so that the base region and the collector region are completely isolated from each other, and the thickness of the isolation oxide film (the insulating material

providing isolation) does not vary much, and consequently, the transistors exhibit an improved performance. Moreover, there is no need for there to be a separate step of forming an isolation oxide film between the collector contact region and the base region, and the process can thus be simplified.

The present invention has been described above in connection with a specific embodiment. However, the invention should not be limited to this embodiment alone, but can be modified in various ways.

For instance, the field oxide film provided over the wiring region in this embodiment need not be limited to one formed by an isoplanar technique. The field oxide film can be obtained by selective oxidation, without subjecting the surface of the semiconductor substrate to etching. A p^+-type buried layer can be formed just under the field insulation film, or the field insulation film need not be formed at all.

CLAIMS:

1. A process for manufacturing a semiconductor integrated circuit, comprising:

forming a semiconductor body having a substrate of a first conductivity type, a buried layer of second conductivity type, and an epitaxial layer of the second conductivity type;

forming a silicon oxide film on the body, the silicon oxide film having a first part and a second part, the first part having a greater thickness than the second;

forming grooves in the semiconductor body, those grooves extending through the oxide film the epitaxial and buried layers to the substrate, thereby to divide the epitaxial and buried layers into a plurality of isolated regions;

simultaneously forming further silicon oxide films on the surface of the semiconductor body, the further silicon oxide films including a first further film within the grooves and a second further film in the second part of the first oxide film and of greater thickness than the second part of the oxide film on a part of the surface of at least one isolated region, such that the surface of the epitaxial layer of the or each such isolated region is divided into a first and a second part by the second further film;

forming isolation materials in the grooves; and

forming a semiconductor element in at least some of

the isolated regions, the semiconductor element including a base region in the first part of the epitaxial layer and a collector region in the second part of the epitaxial layer.

2. A process according to claim 1, wherein the collector region in the epitaxial layer is a first collector region, and there is a second collector region in the buried layer, and wherein an emitter region is formed in the base region.

3. A process according to claim 1 or claim 2, wherein the grooves are formed by etching.

4. A process according to any one of the preceding claims, wherein the first and second further films are formed by selectively thermally oxidizing the semiconductor body.

5. A process according to any one of the preceding claims, wherein the isolated regions are formed by filling the grooves with polycrystalline silicon and by covering the surface of the polycrystalline silicon with a silicon oxide film.

6. A process of manufacturing a semiconductor integrated circuit device according to any one of the preceding claims further including

forming a first mask on one main surface of the semiconductor body, except for the regions at which the grooves will be formed and the regions where the second further film will be formed; and

forming a second mask on the regions where the

second further film will be formed;

wherein the grooves are formed using the first and second masks, and the first and second further films are formed using the first mask.

7. A process according to claim 6, wherein the first mask consists of a silicon nitride film, and the first and second parts of the silicon oxide films are formed by selectively and thermally oxidizing the semiconductor body.

8. A process according to claim 6 or claim 7, wherein the second mask consists of a silicon oxide film that is formed by selectively thermally oxidizing the semiconductor body using the first mask.

9. A process according to any one of claims 6 to 8, wherein, simultaneously with the formation of the second mask, a silicon oxide film is formed over the regions where the grooves will be formed, and the silicon oxide film is removed after the formation of the second mask.

10. A process according to any one of claims 6 to 9, wherein the first and second further silicon oxide films are formed after the formation of the grooves by thermally oxidizing the semiconductor substrate using the first mask whilst the second mask is still in place, the second further film being thicker than the first further film.

11. A process according to any one of claims 6 to 10 wherein, after the formation of the grooves, semiconductor regions of the first conductivity type are formed in the semiconductor body in the bottoms of at least some of the

grooves, the semiconductor region having an impurity concentration higher than that of the semiconductor substrate, and the impurities are introduced into the semiconductor body by ion implantation using the first and second masks, while said second mask is still in place.

12. A process for forming a semiconductor integrated circuit device substantially as any one herein described with reference to the accompanying drawings.

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