

Abstract

3D STACKED PACKAGE INTEGRATED CIRCUIT CHIP AND ITS FAILURE
LOCATION METHOD AND DEVICE

5 Embodiments of the present application disclose a 3D stacked package integrated circuit chip and its failure location method and apparatus. The failure location method comprises: determining a plurality of contrast detection layers located at different depths in a standard sample device; detecting the phase values corresponding to different detection frequencies of the exposed contrast detection layers in the failure state by a
10 thermal imager after each grinding of the contrast detection layers; determining the failure location curve of each contrast detection layer according to the correspondence between the detection frequencies and the phase values in the failure state; and performing failure location to the 3D stacked package integrated circuit chip under test according to the failure location curve of each contrast detection layer. The standard
15 sample device is a 3D stacked package integrated circuit chip under test. According to the corresponding relationship between the detection frequency and the phase value of each contrast detection layer in the failure state, the failure positioning curve of the contrast detection layer is determined; according to the failure positioning curve of each contrast detection layer, the failure positioning of the 3D stacked package integrated
20 circuit chip to be tested is performed; wherein the standard sample device is an intact 3D stacked package integrated circuit chip of the same type as the 3D stacked package integrated circuit chip to be tested. The technical solution provided by the embodiment of the application is able to identify or locate the failure in the 3D stacked package integrated circuit chip.

25 (FIG. 1)