PACKAGE ON PACKAGE USING A BUMP-LESS BUILD UP LAYER (BBUL) PACKAGE

FIELD OF THE INVENTION

Embodiments of the present invention generally relate to the field of integrated circuit package design and, more particularly, to package on package using a bump-less build up layer (BBUL) package.

BACKGROUND OF THE INVENTION

With shrinking electronic device sizes and increasing functionality, integrated circuit device packages will need to occupy less space. One way to conserve space is to combine packages on top of packages, however this can create to a prohibitively high z-height as traditionally the top package would need to be elevated to clear the bottom package die.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements, and in which:

FIG. 1 is a graphical illustration of a cross-sectional view of a bump-less build up layer package, in accordance with one example embodiment of the invention;

FIG. 2 is a graphical illustration of a cross-sectional view of another bump-less build up layer package, in accordance with one example embodiment of the invention;

FIG. 3 is a graphical illustration of a cross-sectional view of a package on package using a bump-less build up layer package, in accordance with one example embodiment of the invention; and

FIG. 4 is a graphical illustration of a cross-sectional view of another package on package using a bump-less build up layer package, in accordance with one example embodiment of the invention; and

FIG. 5 is a block diagram of an example electronic appliance suitable for implementing a package on package using a BBUL package, in accordance with one example embodiment of the invention.

DETAILED DESCRIPTION

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be

apparent, however, to one skilled in the art that embodiments of the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments.

Fig. 1 is a graphical illustration of a cross-sectional view of a bump-less build up layer (BBUL) package, in accordance with one example embodiment of the invention. As shown, integrated circuit package 100 includes one or more of microelectronic die 102, microelectronic die active surface 104, microelectronic die inactive surface 106, microelectronic die side 108, encapsulation material 110, first dielectric material layer 112, build-up layers 113, conductive traces 114, conductive contacts 116, through via connection 118, and interconnects 120 and 122.

Microelectronic die 102 is intended to represent any type of integrated circuit die. In one embodiment, microelectronic die 102 is a multi-core microprocessor. Microelectronic die 102 includes an active surface 104 which contains the electrical connections necessary to operate microelectronic die 102 and an inactive surface 106 parallel to active surface 104.

Microelectronic die 102 is held in place on at least one side 108 by encapsulation material 110. Encapsulation material 110 includes at least one surface substantially planar to active surface 104 and one surface substantially planar to inactive surface 106. In one embodiment, active surface 104 is placed on a holding plate while encapsulation material 110 is disposed around microelectronic die 102. In one embodiment, encapsulation material 110 may extend over inactive surface 106.

First dielectric material layer 112 is disposed on at least a portion of active surface 104 and encapsulation material 110. Build-up layers 113 are subsequently disposed on first dielectric material layer 112 using well known processing methods.

Conductive traces 114 are disposed on first dielectric material layer 112 and build-up layers 113 and are in electrical contact with active surface 104. Conductive contacts

116 couple with conductive traces 114 and allow integrated circuit package 100 to be electrically coupled, for example by a socket connection, to a circuit board. In one embodiment, conductive contacts 116 include solder bumps. In another embodiment, conductive contacts 116 include lands.

Through via connection 118 represents an electrically conductive connection through encapsulation material 110 substantially parallel to side 108. In one embodiment, through via connection 118 represents a plated through hole formed by drilling a hole through encapsulation material 110 that is then plated and filled. Interconnects 120 and 122 represent conductive traces to electrically couple through via connection 118 with microelectronic die active surface 104 or conductive contacts 116, respectively.

Fig. 2 is a graphical illustration of a cross-sectional view of another bump-less build up layer package, in accordance with one example embodiment of the invention. As shown, integrated circuit package 200 includes one or more of microelectronic die 202, microelectronic die active surface 204, microelectronic die inactive surface 206, microelectronic die side 208, encapsulation material 210, package core 212, first dielectric material layer 214, build-up layers 215, conductive traces 216, conductive contacts 218, through via connection 220, and interconnects 222 and 224.

Microelectronic die 202 is intended to represent any type of integrated circuit die. In one embodiment, microelectronic die 202 is a multi-core microprocessor. Microelectronic die 202 includes an active surface 204 which contains the electrical connections necessary to operate microelectronic die 202 and an inactive surface 206 parallel to active surface 204.

Microelectronic die 202 is held in place on at least one side 208 by package core 212. Package core 212 includes at least one surface substantially planar to active surface 204 and one surface substantially planar to inactive surface 206. In one embodiment, package core 212 represents a multilayer organic substrate. Microelectronic package core 212 may have an opening in which microelectronic die 202 is disposed. In one embodiment, encapsulation material 210 is disposed between package core 212 and microelectronic die 202 for improved fit or adhesion.

First dielectric material layer 214 is disposed on at least a portion of active surface 204 and encapsulation material 210. Build-up layers 215 are subsequently disposed on first dielectric material layer 214 using well known processing methods.

Conductive traces 216 are disposed on first dielectric material layer 214 and build-up layers 215 and are in electrical contact with active surface 204. Conductive contacts 218 couple with conductive traces 216 and allow integrated circuit package 200 to be electrically coupled, for example by a socket connection, to a circuit board. In one embodiment, conductive contacts 218 include solder bumps. In another embodiment, conductive contacts 218 include lands.

Through via connection 220 represents an electrically conductive connection through package core 212 substantially parallel to side 208. In one embodiment, through via connection 220 represents series of stacked microvias that are formed within package core 212 as part of a manufacturing process. Interconnects 222 and 224 represent conductive traces to electrically couple through via connection 220 with microelectronic die active surface 204 or conductive contacts 218, respectively.

Fig. 3 is a graphical illustration of a cross-sectional view of a package on package using a bump-less build up layer package, in accordance with one example embodiment of the invention. As shown, package on package assembly 300 includes integrated circuit package 100 coupled with a second package 304. While shown as including two packages, any number may be included. Electrical contacts 302 coupled with through via connections 118 electrically couple second package 304 with package 100. An underfill material, such as an epoxy, may be flowed between package 100 and second package 304. Heat spreader 306 may be included between package 100 and second package 304 on inactive surface 106 to assist with heat dissipation. In one embodiment, an integrated circuit device in second package 304 includes a memory device. In one embodiment, an integrated circuit device in second package 304 includes a chipset device. In one embodiment, second package 204 represents a multi-device chip scale package. In one embodiment, second package 204 represents another bump-less build up layer package. In one embodiment, second package 204 represents a traditional flip chip package.

Fig. 4 is a graphical illustration of a cross-sectional view of another package on package using a bump-less build up layer package, in accordance with one example embodiment of the invention. As shown, package on package assembly 400 includes integrated circuit package 200 coupled with a second package 404. While shown as including two packages, any number may be included. Electrical contacts 402 coupled with through via connections 220 electrically couple second package 404 with package 200. An underfill material, such as an epoxy, may be flowed between package 200 and

second package 404. Heat spreader 406 may be included between package 200 and second package 404 on inactive surface 206 to assist with heat dissipation. In one embodiment, an integrated circuit device in second package 404 includes a memory device. In one embodiment, an integrated circuit device in second package 404 includes a chipset device. In one embodiment, second package 404 represents a multi-device chip scale package. In one embodiment, second package 404 represents another bump-less build up layer package. In one embodiment, second package 404 represents a traditional flip chip package.

Fig. 5 is a block diagram of an example electronic appliance suitable for implementing an integrated circuit package, in accordance with one example embodiment of the invention. Electronic appliance 500 is intended to represent any of a wide variety of traditional and non-traditional electronic appliances, laptops, desktops, cell phones, wireless communication subscriber units, wireless communication telephony infrastructure elements, personal digital assistants, set-top boxes, or any electric appliance that would benefit from the teachings of the present invention. In accordance with the illustrated example embodiment, electronic appliance 500 may include one or more of processor(s) 502, memory controller 504, system memory 506, input/output controller 508, network controller 510, and input/output device(s) 512 coupled as shown in Fig. 5. Processor(s) 502, or other integrated circuit components of electronic appliance 500, may comprise a package on package using a BBUL package as described previously as an embodiment of the present invention.

Processor(s) 502 may represent any of a wide variety of control logic including, but not limited to one or more of a microprocessor, a programmable logic device (PLD), programmable logic array (PLA), application specific integrated circuit (ASIC), a microcontroller, and the like, although the present invention is not limited in this respect. In one embodiment, processors(s) 502 are Intel® compatible processors. Processor(s) 502 may have an instruction set containing a plurality of machine level instructions that may be invoked, for example by an application or operating system.

Memory controller 504 may represent any type of chipset or control logic that interfaces system memory 506 with the other components of electronic appliance 500. In one embodiment, the connection between processor(s) 502 and memory controller 504 may be a point-to-point serial link. In another embodiment, memory controller 504 may be referred to as a north bridge.

System memory 506 may represent any type of memory device(s) used to store data and instructions that may have been or will be used by processor(s) 502. Typically, though the invention is not limited in this respect, system memory 506 will consist of dynamic random access memory (DRAM). In one embodiment, system memory 506 may consist of Rambus DRAM (RDRAM). In another embodiment, system memory 506 may consist of double data rate synchronous DRAM (DDRSDRAM).

Input/output (I/O) controller 508 may represent any type of chipset or control logic that interfaces I/O device(s) 512 with the other components of electronic appliance 500. In one embodiment, I/O controller 508 may be referred to as a south bridge. In another embodiment, I/O controller 508 may comply with the Peripheral Component Interconnect (PCI) Express™ Base Specification, Revision 1.0a, PCI Special Interest Group, released April 15, 2003.

Network controller 510 may represent any type of device that allows electronic appliance 500 to communicate with other electronic appliances or devices. In one embodiment, network controller 510 may comply with a The Institute of Electrical and Electronics Engineers, Inc. (IEEE) 802.11b standard (approved September 16, 1999, supplement to ANSI/IEEE Std 802.11, 1999 Edition). In another embodiment, network controller 510 may be an Ethernet network interface card.

Input/output (I/O) device(s) 512 may represent any type of device, peripheral or component that provides input to or processes output from electronic appliance 500.

In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form.

Many of the methods are described in their most basic form but operations can be added to or deleted from any of the methods and information can be added or subtracted from any of the described messages without departing from the basic scope of the present invention. Any number of variations of the inventive concept is anticipated within the scope and spirit of the present invention. In this regard, the particular illustrated example embodiments are not provided to limit the invention but merely to illustrate it. Thus, the scope of the present invention is not to be determined by the specific examples provided above but only by the plain language of the following claims.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a microelectronic die having an active surface, an inactive surface parallel to said active surface, and at least one side;

an encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes a bottom surface substantially planar to said microelectronic die active surface and a top surface substantially planar to said microelectronic die inactive surface;

a through via connection in said encapsulation material extending from said top surface to said bottom surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material bottom surface;

a plurality of build-up layers disposed on said first dielectric material layer; and

a plurality of conductive traces disposed on said first dielectric material layer and said build-up layers and in electrical contact with said microelectronic die active surface.

2. The apparatus of claim 1, further comprising a second microelectronic die package on said top surface in electrical contact with said through via connection in said encapsulation material.

3. The apparatus of claim 2, further comprising a heat spreader between said second microelectronic die package and said inactive surface of said microelectronic die.

4. The apparatus of claim 2, wherein said through via connection comprises a plated through hole.

5. The apparatus of claim 2, further comprising said through via connection in electrical contact with said microelectronic die active surface.

6. The apparatus of claim 2, further comprising said through via connection in electrical contact with bumps formed on said build-up layers.

7. An electronic appliance comprising:

a network controller;

a system memory; and

a processor, wherein said processor comprises:

a microelectronic die having an active surface, an inactive surface parallel to said active surface, and at least one side;

an encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes a bottom surface substantially planar to said microelectronic die active surface and a top surface substantially planar to said microelectronic die inactive surface;

a through via connection in said encapsulation material extending from said top surface to said bottom surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material bottom surface;

a plurality of build-up layers disposed on said first dielectric material layer; and

a plurality of conductive traces disposed on said first dielectric material layer and said build-up layers and in electrical contact with said microelectronic die active surface.

8. The electronic appliance of claim 7, further comprising a second microelectronic die package on said top surface in electrical contact with said through via connection in said encapsulation material.

9. The electronic appliance of claim 8, wherein said second microelectronic die package comprises said system memory.

10. The electronic appliance of claim 8, wherein said second microelectronic die package comprises a chipset device.

11. The electronic appliance of claim 8, wherein said second microelectronic die package comprises a bumpless build-up layer package.

12. The electronic appliance of claim 8, wherein said second microelectronic die package comprises a chip scale package.

13. An apparatus comprising:

a microelectronic die having an active surface, an inactive surface parallel to said active surface, and at least one side;

a substrate core adjacent said at least one microelectronic die side, wherein said substrate core includes a bottom surface substantially planar to said microelectronic die active surface and a top surface substantially planar to said microelectronic die inactive surface;

a through via connection in said substrate core extending from said top surface to said bottom surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said substrate core bottom surface;

a plurality of build-up layers disposed on said first dielectric material layer; and

a plurality of conductive traces disposed on said first dielectric material layer and said build-up layers and in electrical contact with said microelectronic die active surface.

14. The apparatus of claim 13, further comprising a second microelectronic die package on said top surface in electrical contact with said through via connection in said substrate core.

15. The apparatus of claim 14, further comprising a heat spreader between said second microelectronic die package and said inactive surface of said microelectronic die.

16. The apparatus of claim 14, wherein said through via connection comprises stacked microvias.

17. The apparatus of claim 14, further comprising said through via connection in electrical contact with said microelectronic die active surface.

18. The apparatus of claim 14, further comprising said through via connection in electrical contact with bumps formed on said build-up layers.

19. An electronic appliance comprising:

a network controller;

a system memory; and

a processor, wherein the processor comprises:

a microelectronic die having an active surface, an inactive surface parallel to said active surface, and at least one side;

a substrate core adjacent said at least one microelectronic die side, wherein said substrate core includes a bottom surface substantially planar to said microelectronic die active surface and a top surface substantially planar to said microelectronic die inactive surface;

a through via connection in said substrate core extending from said top surface to said bottom surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said substrate core bottom surface;

a plurality of build-up layers disposed on said first dielectric material layer; and

a plurality of conductive traces disposed on said first dielectric material layer and said build-up layers and in electrical contact with said microelectronic die active surface.

20. The electronic appliance of claim 19, further comprising a second microelectronic die package on said top surface in electrical contact with said through via connection in said substrate core.

21. The electronic appliance of claim 20, wherein said second microelectronic die package comprises said system memory.

22. The electronic appliance of claim 20, wherein said second microelectronic die package comprises a chipset device.

23. The electronic appliance of claim 20, wherein said second microelectronic die package comprises a bumpless build-up layer package.

24. The electronic appliance of claim 20, wherein said second microelectronic die package comprises a chip scale package.