

# PATENT SPECIFICATION

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## DRAWINGS ATTACHED

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## (54) IMPROVEMENTS IN OR RELATING TO PHASE COMPARISON RADIO NAVIGATION SYSTEMS

(71) We, DECCA LIMITED, a British Company, of Decca House, 9, Albert Embankment, London, S.E.1, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to receivers for phase comparison radio navigation systems.

In the Decca (Registered Trade Mark) Navigator system, a chain of transmitting stations comprises a master station which normally radiates radio frequency signals of a frequency  $6f$  and three slave stations, known as the red, green and purple slaves which normally radiate signals of frequencies  $8f$ ,  $9f$  and  $5f$  respectively,  $f$  being the fundamental frequency of the system. All the radiated signals are in a fixed phase relation. Periodically the radiations from the stations are interrupted and one station radiates on all four frequencies in a fixed phase relation, this being done by all the stations in sequence. Different chains operate with slightly different fundamental frequencies  $f$ .

According to this invention, a receiver for a phase comparison radio navigation system in which phase locked signals of different but harmonically related frequencies are normally radiated from fixed stations and in which periodically for a short duration each station in turn radiates signals of all the frequencies in fixed phase relation, the normal radiations from the other stations being interrupted, comprises receiving channels for each of the radiated signals, a number of oscillators corresponding to the number of different received frequencies, means for locking the oscillators in phase respectively with the received signals of different frequencies during the normal transmission periods, the oscillators having frequencies either equal to the received frequencies or being in the same ratio as the received frequencies, phase discriminators

coupled to the oscillators to provide at least two sets of sine and cosine signals, each set being representative of the phase relation between a different pair of oscillators, a separate rotary indicator for each set of sine and cosine signals, the indicators being driven by the discriminators, a frequency divider dividing the output of one of the oscillators down to the fundamental frequency (i.e. the highest frequency of which all the oscillator frequencies are integral multiplies), means for producing from the multiple signal transmissions from the various stations signals of said fundamental frequency, and a digital phase indicator including a digital counter and clock source for indicating the phase relation between the divided down oscillator output and the successive signals of the same frequency derived from the multiple frequency transmissions from the various stations in turn.

For operation with any one of a number of different chains, a frequency synthesiser may be provided for producing a heterodyne signal of frequency  $\Delta$  such that  $\Delta = f + F$  where  $f$  is the fundamental frequency of any selected chain and  $F$  is the fixed fundamental frequency of the oscillators in the receiver. Each received signal, which is a harmonic of  $f$ , may be converted to the corresponding harmonic of  $F$  by mixing with the corresponding harmonic of  $\Delta$  and taking the lower side-band.

The lane identification display is conveniently a decimal digit display, e.g. using cold cathode number tubes.

Each of said rotary indicators preferably comprises a meter with a rotary pointer movable over a circular scale and phase angle integrating means comprising a mechanical cycle counter indicating the number of complete cycles of rotation of said pointer. Such a rotary indicator with a pointer movable over a scale provides the optimum form of a display when the display is used for steering a

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vessel along a lattice line of the navigation system as deviations from the required track are immediately indicated visually in magnitude and direction by the deflection of the pointer. This type of display moreover enables, by mechanical integration, the lane and zone counts to be indicated continuously. The digital display of lane information provided by the digital counter forms a particularly convenient way of indicating the lane identification information which is derived from the periodic multipulse transmissions so that an observer can unambiguously obtain lane identification (which is only intermittently available) which can be used for setting the mechanical integrators.

The invention furthermore includes within its scope a receiver for a phase comparison radio navigation system of the kind in which radio frequency signals are radiated from two or more pairs of spaced transmitters, said transmitters including a common master transmitter normally radiating a signal of frequency  $6f$  and at least two slave stations normally radiating signals of different frequencies  $nf$  where  $n$  is 5, 8 or 9,  $f$  being the common fundamental frequency and wherein for short duration periods each transmitter in turn radiates signals of  $5f$ ,  $6f$ ,  $8f$  and  $9f$  simultaneously, the radiations from the other transmitters being interrupted during these periods, said receiver comprising:—

(a) a frequency selective amplifier for each of the four frequencies,

(b) four oscillators having frequencies either equal to the respective received frequencies or being in the same ratio as the respective received frequencies, together with means locking the phases of the oscillator outputs to the respective received signals during the normal transmission periods;

(c) pulse generating means for deriving from the output of the oscillator locked to the  $6f$  signals a series of short duration pulses synchronised with the oscillator output, each pulse having a duration short compared with a cycle of the oscillator output;

(d) three frequency multipliers coupled respectively to the outputs of the three oscillators locked to the  $5f$ ,  $8f$  and  $9f$  signals and operative to provide three outputs respectively of frequencies equal to the respective least common multiple of the frequency of the associated oscillator and the frequency of that locked to the  $6f$  signals;

(e) means for generating, from each of the frequency multiplied signals, a pair of phase quadrature signals in fixed phase relation with the frequency multiplied signals from which they are generated;

(f) gating means controlled by the short duration pulses from said pulse generating means arranged to gate the three pairs of phase quadrature signals to provide three pairs of phase-controlled d.c. outputs;

(g) three rotary indicator means, each having a rotor taking up an angular position dependant on the relative magnitudes and polarities of d.c. signals applied to orthogonal coils together with means applying the three pairs of phase-controlled d.c. outputs respectively to the three sets of orthogonal coils, whereby the rotor rotations are proportional to the phase angles between the received signals from the master station and the respective slave stations during the normal transmissions;

(h) cycle counting means coupled to the rotors of the three rotary indicator means to indicate integrated cycles of measured phase change;

(i) a frequency divider dividing the output of the oscillator locked to the  $6f$  received signals down to the fundamental frequency (i.e. the highest frequency of which all the oscillator frequencies are integral multiples);

(k) means for producing from the multiple signal transmissions from the various stations signals of said fundamental frequency; and

(l) a digital phase indicator including a digital counter and a clock source for indicating the phase relation between the divided down oscillator output and the successive signals of the same frequency derived from the multiple frequency transmissions from the various stations in turn.

The aforesaid digital counter and clock source conveniently comprises digital counting means providing a readout which is the complement of a count of clock pulses during a time period started by a signal at the oscillator fundamental frequency derived from a received multipulse signal from one of the slave stations and stopped by a stop count pulse signal at the same frequency derived from the oscillator locked to the normal master signal, said count being compensated by a count started by a signal at the oscillator fundamental frequency derived from the master multipulse signal and stopped by the stop count pulse.

The following is a description of one embodiment of the invention, reference being made to the accompanying drawings in which:—

Figure 1 is a perspective view of a receiver and display unit for a phase comparison radio navigation system;

Figure 2 is a schematic diagram of a radio frequency/intermediate frequency unit forming part of the receiver of Figure 1 and including also certain controls;

Figure 3 is a schematic diagram of a locked oscillator unit of the receiver of Figure 1 showing also certain display indicators;

Figure 4 is a schematic diagram of a heterodyne and locked oscillator unit of the receiver of Figure 1, showing also certain further controls;

Figure 5 is a schematic diagram of a lane

identification and timer unit of the receiver of Figure 1 together with a further display unit; and

5 Figure 6 is a diagram showing how Figures 2, 3 4 and 5 fit together to form the complete receiver display system.

10 The receiver and display unit shown in the drawings is for use with fixed transmitting stations of the Decca (Registered Trade Mark) system. Each chain of transmitters comprises a master station and usually three slave stations, known as the red, green and purple slaves. The master station normally radiates continuous signals of a frequency  $6f$  where  $f$  is a fundamental frequency of the order of 14 kHz. The red, green and purple slaves normally radiate on frequencies  $8f$ ,  $9f$  and  $5f$ . All the radiated signals are locked in phase. Periodically the transmissions from all the stations are interrupted and a short duration signal of all the frequencies  $5f$ ,  $6f$ ,  $8f$  and  $9f$  in fixed phase relation is radiated from one station. This signal is referred to as the multipulse signal. The multipulse signal is radiated in sequence from the master station and the red, green and purple slaves. Each multipulse transmission is preceded by a break of 0.1 seconds in the normal master ( $6f$ ) transmission.

30 The normal transmissions are utilized in a mobile receiver by separately comparing the phase of each of the received slave signals ( $8f$ ,  $9f$  and  $5f$ ) with the received master  $6f$  signals. The comparisons are effectively at the lowest common multiple frequencies. The phase angle is indicated to provide fine positional information with respect to three sets of hyperbolic position lines. This final positional information corresponds to the phase angle within a cycle but is ambiguous in that each hyperbolic pattern covers many complete cycles. The various different cycles of the pattern are referred to as lanes. The multipulse signals are used for lane identification. 45 In this receiver the effective comparison frequency employed is the fundamental frequency. A phase measurement at this frequency gives a coarser indication which serves to identify a lane within a zone, a zone being 24 lanes for the red pattern, 18 lanes for the green pattern and 30 lanes for the purple pattern.

50 The receiver can be utilized with any of a number of different chains. The different chains have fundamental frequencies which differ by small amounts. This is achieved, as will be more fully explained later by superheterodyne operation to convert the received signals of  $5f$ ,  $6f$ ,  $8f$  and  $9f$  to  $5F$ ,  $6F$ ,  $8F$  and  $9F$  by mixing with the appropriate harmonics of a heterodyne frequency  $\Delta$  where  $\Delta = f + F$ , using the lower side bands of the mixer outputs. Thus the normal phase comparison is effected in the circuitry at the frequencies 65 24F for red, 18F for green and 30F for purple

whilst the lane identification has a comparison frequency of  $1F$ , although the effective frequencies are  $24f$ ,  $18f$  and  $30f$  for the normal patterns and  $1f$  for lane identification.

Referring now to Figure 1, the receiver and display unit illustrated is particularly for marine use and comprises a base 10 with a trunnion mounted display unit 11 containing all the circuitry which, with the exception of a cold-cathode number tube display, is all solid-state utilizing printed circuit boards. The power supplies are provided by a power supply unit (not shown) fitting onto the bottom of the assembly of Figure 1, this power supply unit being interchangeable so that an appropriate unit may be fitted according as to whether the external supply is A.C. or D.C. and to its voltage and frequency.

In the upper part of the unit 11 are the red, green and purple fractional lane indicators 12, 13 and 14 (known as decometers), each comprising a pointer rotatable over a dial. Associated with each of the fractional lane indicators are integrating lane counters in the form of rotating discs. It will be seen that each fractional lane indicator has a lane indicator 15 and a zone indicator 16. The lane indication from the multiple signals is shown on a three digit cold cathode number tube display 17.

The panel of the upper unit also includes a "lock lamp" 18 to be described later, a lane identification zero push button 19 and a dimmer control 20 for the display 17.

In the lower part of the assembly, a hinged cover 21 is provided for covering certain controls, primarily for setting up, these controls being a pair of multiposition switches 22, 23 for chain selection, zero setting controls 24, 25 and 26 for the three decometers and a function switch 27.

Referring now to Figures 2 to 5, the main units, each formed by a single circuit board and indicated by dashed line boxes, are an R.F./I.F. unit 30 (shown in Figure 2), a heterodyne and reference oscillator unit 32 (shown in Figure 4), a locked oscillator unit 33 (shown in Figure 3) and a lane identification and timer 34 (shown in Figure 5) with which is associated a smaller board 35 (also shown in Figure 5) for the display 17. Figures 2 to 5 fit together as shown in Figure 6.

An aerial 40 (Figure 2) is connected via a buffer/limiter 41 and gate 42 to amplifiers 43, 44, 45 and 46 tuned respectively to  $5f$ ,  $8f$ ,  $9f$  and  $6f$  but of sufficient bandwidth to amplify signals from any selected chain. The outputs from these amplifiers are fed respectively to mixers 47, 48, 49 and 50 where they are mixed with the appropriate harmonics of the  $\Delta$  signals from the unit 32. For this purpose, the  $\Delta$  signals on a lead 51 from unit 32 are fed to multipliers 52, 53, 54 and 55 to provide the appropriate harmonics. Associated with the multipliers 52, 53 and 54 res-

pectively are the zero setting controls 26, 24 and 25 which, although shown within the box 30 of Figure 2, are located on the lower panel as shown in Figure 1. The required sidebands of 5F, 8F, 9F and 6F from the mixers 47, 48, 49 and 50 are selected by band pass filters 56, 57, 58 and 59 and the filter outputs are amplified by amplifiers 60, 61, 62 and 63 and are passed to phase discriminators 64, 65, 66 and 67 where the received signals are respectively compared in phase with signals of the same frequencies from oscillators 68, 69, 70 and 71 in the unit 33 (Figure 3). The phase discriminators 64, 65, 66 and 67 are of the sampling type, the outputs of the oscillators 68, 69, 70, 71 being fed to pulse producing circuits 72, 73, 74, 75 respectively to provide the short duration sampling pulses for applying to the phase discriminators. The phase discriminators are sine output discriminators, there being zero outputs when the oscillator outputs are in phase with the received signals; the discriminator outputs are thus D.C. voltages and they are applied to integrator/reactors 76, 77, 78 and 79 (Figure 3) to control the respective oscillator frequencies. In two positions, "LOCK 1" and "LOCK 2" of the function switch 27 (Figure 2), fast lock switching is applied via lead 28 to the integrator/reactors 76, 77, 78 and 79. These integrator/reactors serve to control the frequencies of the respective oscillators so as to maintain a phase lock between each oscillator output and the respective input from the amplifiers 60, 61, 62 and 63. A further description of the oscillator control loop is given in the specification of co-pending British Patent Application No. 50542/69 (Serial No. 1,258,117).

The pulse outputs from the pulse producers 72, 73 and 74 (at frequencies 5F, 8F and 9F respectively) are fed to frequency multipliers 80, 81 and 82 to give signals at frequencies 30F, 24F and 18F respectively. Considering the 30F signal from the multiplier 80, this signal is fed directly to a sine output phase discriminator 83 and is also fed via a quadrature phase shifter 84 to a cosine phase discriminator 85. These are sampling type phase discriminators, the sampling pulses being at 6F from the oscillator 71 via the pulse shaper 75 and an amplifier 87. The sine and cosine outputs from the phase discriminators 83, 85 are applied via d.c. amplifiers 88, 89 to the purple decometer 14. Similarly the red decometer 12 is driven by phase discriminators 90, 91 and d.c. amplifiers 92, 93 to indicate the phase relation between the 8F and 6F signals and the green decometer 13 is driven by phase discriminators 94, 95 and d.c. amplifiers 96, 97 to indicate the phase relation between the 9F and 6F signals. It will be noted that, by using locked oscillators to drive the decometers, the locked oscillators

perform effectively as very narrow band filters, providing continuous noise-free drive to the decometers and bridging the interruptions in received signals during the short signalling breaks and during the multipulse transmissions.

Each of the decometers 12, 13 and 14 has a rotor carrying a pointer which traverses a circular scale. The angular position of the rotor is determined by the relative magnitudes and polarities of d.c. signals applied to orthogonal coils of the decometer. These d.c. signals are obtained from the d.c. amplifiers 88, 89 for the purple decometer and the corresponding amplifiers for the other decometers and hence correspond to the sine and cosine of the phase angle between the master and respective slave signals as received at the receiver. The angular positions of the rotors thus correspond to the phase angles. The changes of phase angle are mechanically integrated and complete cycles of phase change are indicated by the associated lane indicator 15 which is driven through a reduction gear from the decometer rotor. The zone indicator 16 for each decometer is likewise driven through further reduction gearing from the lane indicator.

The decometers may be adjusted manually by means of manual control knobs 180. Operation of these controls enables the lane and zone indicators to be reset but the rotor of each phase angle indicator will take up a position corresponding to the measured phase angle. These knobs 180 therefore enable the lane and zone indicators 15, 16 to be reset without affecting the accuracy of the positional information from the phase angle measurement within a cycle.

The 6F pulse output from the pulse shaper 75 is used not only as the sampling pulse for the phase discriminators driving the three decometers 12, 13 and 14 and in the phase lock control loop for the 6F oscillator 71 but is fed also to a frequency divider 98 to give 1F pulses for purposes to be described later and is also fed via a quadrature phase shifter 99 to a cosine phase discriminator 100 (Figure 2). In this discriminator 100, the 6F signals from amplifier 63 are sampled. This discriminator 100 thus gives its maximum output so long as the normal 6F signals from the master station are being received and the 6F oscillator 71 in the receiver is locked in phase to the 6F signals from amplifier 63.

The output from the discriminator 100 is fed via a lead 101 to an amplifier 110 in the heterodyne and reference oscillators 32 (Figure 4). The output from the amplifier 110 is fed to the lock lamp 18 which will thus "blink" if the oscillator 71 is not properly phase locked. If the oscillator 71 is locked, the lamp 18 will remain continuously lit except during the multipulses and the breaks in the master transmissions immediately before the multi-

pulses. The amplifier 110 also provides the input to a "break detector" 111 to detect the restoration of the 0.1 second after the break and so give an output signal which indicates the start of each multipulse.

The heterodyne and reference oscillator 32 contains a frequency synthesiser providing the heterodyne frequency  $\Delta$  and also a reference oscillator for referencing the receiver.

The frequency synthesiser comprises a 436,907 kHz crystal oscillator 120 feeding a divider train 121 and a matrix 122 for combining the divider train outputs, the matrix 122 being controlled by the aforementioned chain selector switches 22, 23. The synthesised frequency output from the matrix is used to control the frequency of a heterodyne oscillator 123 having a phase lock control loop consisting of a sawtooth output discriminator 124 giving a d.c. output voltage applied to a reactor 125 controlling the oscillator frequency. The  $\Delta$  frequency output from the oscillator 123 is used for frequency changing in the aforementioned mixers 47, 48, 49 and 50. The reference oscillator for referencing the receiver is an 8F oscillator 130. This oscillator is phase locked to the 1F pulses from the aforementioned divider 98 (Figure 3), these pulses being applied via a lead 102 to a linear phase discriminator 131 (Figure 4) having 1F sampling pulses from a divide-by-eight divider 132 fed from the output of oscillator 130 and the d.c. output voltage of discriminator 131 being applied to a reactor 133 to control the frequency of oscillator 130. The 1F output from the divider 132 is converted into 1f pulse signals by means of a mixer 134, receiving  $\Delta$  frequency signals from oscillator 123, and a pulse shaper 135. The 1f pulses from the shaper 135 can be applied to the receiver input channels 43, 44, 45 and 46 (Figure 2) via a gate 136. This gate 136 and the aforementioned gate 42 are controlled by the function switch 27; normally only the received signals are applied to the receiver input channels but, when the function switch 27 is in the "Reference" position, these signals are disconnected from the receiver channels by closing gate 42 and the 1f pulses are applied by opening gate 136. These pulses form a series of harmonics of the frequency 1f in a fixed multiple phase relation and the decimeters 12, 13 and 14 are set to zero using the zero setting controls 24, 25 and 26 which provide electrical reference adjustment for the decimeters. During referencing, the 6F oscillator 71 is not locked to received signals but the stability of this oscillator is such as to maintain the frequency of the reference oscillator 130 very closely during the referencing operation.

The lane identification is obtained by measuring the phase lag of an effective 1f signal from each slave station compared with

a 1f signal from the master station. These 1f signals from the slaves are provided by the multipulse transmissions and are used after frequency changing to 1F. The master oscillator 71 provides the master 1F reference.

The multipulse signals for lane identification purposes are obtained in the receiver by combining the outputs at 5F, 8F, 9F and 6F from the amplifiers 60, 61, 62 and 63 in a multipulse circuit 140 (Figure 5). The phase relationship of the radiated 5f, 8f, 9f and 6f signals in each multipulse transmission is such that they combine to give a peak pulse at a frequency 1f. Thus the 5F, 8F, 9F and 6F signals from the amplifiers 60, 61, 62 and 63 give a peak pulse at a frequency 1F and this is used to set a bistable 141 which is reset by the 1F output from the frequency divider 98 (Figure 3) on lead 139. The bistable 141 (Figure 5) controls a gate 142. The multipulse signal has a duration of a fraction of a second but contains many cycles at 1F. The gate 142 is cocked by a short duration lane identification read time pulse, referred to as the second L.I pulse obtained on the lead 151 from switching logic 147 to be described later. The gate 142 is cocked only for the duration of this second L.I pulse and serves only to pass pulses during one time period starting on a 1F multipulse signal and ended by the next 1F pulse from the divider 98. The gate 142 gates pulses from a 300F oscillator 143 into a store 144 via an OR gate 145. The multipulse circuit 140, from the received multipulse 1F signals, thus effectively provides one pulse synchronised with the effective 1F from the multipulse. This pulse opens the gate 142 and the next 1F signal from the divider 98 closes the gate. The multipulse signal will therefore produce a stored count in store 144 proportional to the multipulse-to-master delay, i.e. proportional to the complement of the Master:Multipulse zone pattern phase angle in 1/300th zone units. The total capacity of the store 144 corresponds to one complete cycle at 1F, i.e. a count of 300 at 300F. The required lane identification is obtained by determining the residual capacity in the store 144, this being done by filling the store until it overflows and determining the quantity required in 1/300th zone units for purple but in 1/24th zone units for red and 1/180th zone units for green. To do this, the store 144 is filled from the 300F oscillator 143 via a divider 146 which divides by a factor of 10 or 8 or 6 under the control of lane identification switching logic 147, to be described later, the division factor being 10 for purple, 8 for red and 6 for green. The divider output is fed to the store 144 via the OR gate 145. Simultaneously, the 300F signals from the oscillator 143 are fed via a 10 to 1 divider 148 and a gate 149 into a display register 150. The gate 149 is a two input AND gate having, as a second input a pulse

signal derived from a pulse generator 152 which is started by a pulse, known as the fourth LI pulse from the logic unit 147 on lead 153 and terminated by a stop pulse from the register 144 when the latter is full. The fourth LI pulse is a timing pulse slightly delayed after the second LI pulse. Thus, considering the red lane identification, the divider 146 is set to divide by 8 and so the ratio of the number of pulses fed into the display register 150 to the number fed into the store 144 is 8 to 10. Similarly for the green lane identification, the ratio is 6 to 10. Thus, although the pulses fed into the store 144 are in units of 1/300th of a zone, those fed into the display register are in units of 1/240th of a zone for red, 1/180th of a zone for green and 1/300th of a zone for purple; in other words they now correspond to one tenth of a lane for each of the patterns.

The display register 150 has to be filled only during the time taken for the store register 144 to be filled after the initial count of the complement of the master to multipulse period. To do this the display register has to be reset for the start of the required period and the gate 149 closed when the store register 144 is completely full. This closing of the gate 149 is effected by an output signal from register 144 when this store register is full. The display register is reset for each multipulse by a first LI pulse from the switching logic 147. In the Decca (Registered Trade Mark) Navigator system, to avoid any possibility of confusion between readings on different patterns, the 24 lanes in a red zone are numbered from 0 to 23 and thus a red lane identification (to a tenth of a lane) is expressed as a number between 0 to 23.9. The 18 lanes in a green zone are numbered from 30 to 47 and so the green lane identification is expressed as a number between 30 and 47.9. The 30 lanes in a purple zone are numbered from 50 to 79 and so the purple lane identification is expressed as a number between 50 and 79.9. For these reasons, the display register 150 is set to zero at the beginning of the red lane identification count into that register, to 30 at the beginning of the green count into that register and to 50 at the beginning of the purple count into that register. The switching logic 147, in resetting the display register, therefore has appropriately to set the most significant decimal digit of the display register which is a binary coded decimal counter.

The lane identification switching logic 147 provides output gating signals referred to as the first LI pulse, on four leads 160, 161, 162 and 163 indicating the start of the master, red, green and purple multipulse transmissions respectively, these signals being used for setting the divider 146 to divide by the appropriate factor and to reset the display register 150 before the start of each count into that

register. For this purpose, the switching logic 147 makes use of the "break" detector 111, and time division of 26.6 Hz and 13.3 Hz signals from the divider train 121 to provide a cycle of approximately 20 second period during which an output appears successively on the leads 160, 161, 162 and 163 at 2.5 second intervals. The master multipulse is the first of each sequence of four pulses and is identified thereby in the switching logic. The first LI pulse for each multipulse which is used for setting the store register 144 via lead 158 is timed to occur in the latter half of the multipulse period and is timed to occur about 0.3 to 0.4 of a second after the break in the master transmission. The second, third and fourth LI pulses follow the first LI pulse in each multipulse with small sequential delays appropriate for their respective logical operations.

The master multipulse LI signal on lead 160 is applied, by means of an OR gate 164, to the divider 146 and display register 150 in the same way as the red multipulse signal and is utilized for zeroing the lane identification outputs. In the receiver described, the frequency divider 98 dividing the 6F oscillator output down to 1F is not "notched", that is to say, the 1F output is not locked to any specific one of the six cycles of the 6F signal. There is therefore a sixfold possible ambiguity in the phase relation of the 1F output from divider 98 with respect to the 1F multipulse from the master station fed to the multipulse circuit 144. A correction is therefore put in the store register 144 to bring the lane identification reading on display register 150 to zero on the master multipulse transmission and this same correction is used for each of the other multipulse transmissions thereby correcting for the absence of notching on the divider 98 and also correcting for any other phase errors which might arise between the multipulse take-off and the master oscillator (6F oscillator 71) locking circuit. This correction is effected using a "phase" store 170 and a bistable 171. The bistable 171 can be set by depressing the lane identification zero push button 19 and it then provides a signal to a gate 172, which gate, when opened admits 30F pulses from divider 148 into the phase store 170. The bistable 171 is reset the next time the store register 144 is completely filled. The gate 172 is a four input AND gate and has an input on lead 156 from logic unit 147 so that the gate 172 is open only during master multipulse transmissions and not during slave multipulse transmissions. The fourth input to gate 172 is a third LI pulse on lead 157 from logic unit 147 so that the gate is only opened for the required appropriate time duration during the master multipulse transmission. The number of 30F pulses fed into the phase store 170 via the gate 172 is thus the same as the number fed into the display

register 150. The reason for the four inputs to gate 172 is to ensure that the phase error reading is injected into store 170 at the third LI pulse only when the button 19 is pressed and only on a master multipulse transmission. The pulses from gate 172 are also fed via lead 173 into gate 145 and thus into the store register 144. When this register is full, it spills over and bistable 171 is reset. Thus the phase store 170 has the required correction and register 144 is in the zero state. Gate 181 ensures that the bistable 171 is reset only between the third and fourth LI pulses. This prevents bistable 171 being reset too early if the zero button 19 is pressed for example, immediately after the previous master lane identification.

The number thus put in the phase store 170 is then applied as an initial input to the store register 144 each time the latter is reset by the first LI pulse. Functionally, it is required that the phase store 170 should contain the phase reading on the master multipulse transmissions and thus the button 19 should be depressed before a master multipulse transmission. In practice however, the button can be depressed at any time and the next master multipulse reading on the display register 150 is 00.0 or 23.9. The required correction is thus set into the phase store 170. The count remains in the store 170 and is used for correction of each subsequent count in the store register 144.

The output on the display register 150 is visually indicated on the three tubes of the number tube display 17 (Figure 1). In Figure 5, these three tubes are shown at 174, 175 and 176, having associated binary-coded-decimal to decimal converters 177, 178 and 179 respectively. The master red, green and purple indications are displayed in sequence in that order, at 2.5 second intervals with a longer interval before the cycle repeats in its 20 second period. Because the numerical values of the green readings must be between 30 and 47.9 and the purple readings between 50 and 79.9, the various readings can readily be distinguished. However, to avoid any possible confusion between the master reading (which is 00.0 or 23.9 after the correction has been set in) and the read reading, the display is made to blink during the master indication, a suitable control signal being obtained from the switching logic 147. The displayed lane identification information is used to set in the lane readings on the indicators 15 of the decometers 12, 13, 14 using the manual control knob 180 on the respective decometers.

The receiver described with reference to and illustrated in the accompanying drawings is also described in the specifications of co-pending Applications Nos. 54971/69 (Serial No. 1308148), 54972/69 (Serial No.

1308149) and 54973/69 (Serial No. 65 1308150).

In the specification of No. 54971/69 Serial No. 1308148, there is described and claimed:—

A receiver for a phase comparison radio navigation system of the kind in which fixed stations normally radiate signals, one from each station, on different harmonics of a common radiation fundamental frequency and in which, for lane identification, each station periodically radiates signals of two or more frequencies from which a signal of the fundamental frequency may be derived at the receiver, said receiver having an oscillator locked in phase to signals of the one frequency normally radiated from one station, and a divider for dividing down the output from the oscillator to the fundamental frequency, wherein there are provided means for determining the phase relation between the fundamental frequency signal derived from the multiple frequency transmissions from said one station and the fundamental frequency signal from the divider and means for automatically applying this phase determination as a correction to determinations of the phase relation between the divider output and the fundamental frequency signals derived from the multiple frequency transmissions from each of the other stations.

In the specification of No. 54972/69 (Serial No. 1308149), there is described and claimed:—

A receiver for a phase comparison radio navigation system of the kind in which radio frequency signals of three or more different but harmonically related frequencies received from different spaced transmitting stations are compared in phase in pairs at their least common multiple frequencies to provide positional information with respect to fine patterns and in which coarser positional information to identify the lanes of the fine patterns is obtained by making phase comparisons at the fundamental frequency for each pair of stations, characterized in that the fundamental frequency comparisons are affected digitally using a counter to count pulses from a clock source during a time interval representative of the phase difference between the signals to be compared, the clock pulse source including an adjustable frequency divider controlled in accordance with the sequential comparison of signals from different pairs of stations to display counts related to the phase difference, the respective counts, by adjustment of the divider, being proportional to the respective least common multiple frequencies used for the fine pattern of each pair.

In the specification of No. 54973/69 (Serial No. 1308150), there is described and claimed:—

A receiver for a phase comparison radio navigation system of the kind in which sig-

nals of different multiples of a fundamental frequency  $f$  are radiated in fixed phase relation from spaced transmitting stations, the transmitting stations normally radiating one signal at a time, but in which periodically the normal transmissions are interrupted and each station, one at a time in sequence, radiates all the frequencies to form a multipulse for lane identification, the multipulse being in a fixed cyclic time sequence from the various stations, and in which the receiver is of the heterodyne type for receiving signals from chains operating on different fundamental frequencies, wherein the receiver has a frequency synthesiser including a stable oscillator and divider chain for providing a plurality of selectable different frequencies for heterodyning the received signals whereby phase comparison means operating at fixed frequencies may be used irrespective of the actual radiated frequencies of the transmitting stations being used.

#### WHAT WE CLAIM IS:—

1. A receiver for a phase comparison radio navigation system of the kind in which phase locked signals of different but harmonically related frequencies are normally radiated from fixed stations and in which periodically for a short duration each station in turn radiates signals of all the frequencies in fixed phase relation, the normal radiations from the other stations being interrupted, which receiver comprises receiving channels for each of the radiated signals, a number of oscillators corresponding to the number of different received frequencies, means for locking the oscillators in phase respectively with the received signals of different frequencies during the normal transmission periods, the oscillators having frequencies either equal to the respective received frequencies or being in the same ratio as the respective received frequencies, phase discriminators coupled to the oscillators to provide at least two sets of sine and cosine signals, each set being representative of the phase relation between a different pair of oscillators, a separate rotary indicator for each set of sine and cosine signals, the indicators being driven by the discriminators, a frequency divider dividing the output of one of the oscillators down to the fundamental frequency (i.e. the highest frequency of which all the oscillator frequencies are integral multiples), means for producing from the multiple signal transmissions from the various stations signals of said fundamental frequency, and a digital phase indicator including a digital counter and a clock source for indicating the phase relation between the divided down oscillator output and the successive signals of the same frequency derived from the multiple frequency transmissions from the various stations in turn.

2. A receiver as claimed in claim 1 and

for use with any one of a number of different chains of transmitting stations using different fundamental frequencies  $f$ , wherein there is provided a frequency synthesiser for producing a heterodyne signal of frequency  $\Delta$  such that  $\Delta = f + F$  where  $f$  is the fundamental frequency of any selected chain and  $F$  is the fixed fundamental frequency of the oscillators in the receiver, and wherein frequency converting means comprising a mixer and filter as provided for each received signal to convert the received signal which is a harmonic of  $f$ , to the corresponding harmonic of  $F$  by mixing with the corresponding harmonic of  $\Delta$  and taking the lower side band.

3. A receiver as claimed in either of the preceding claims wherein said digital phase indicator comprises a decimal digit display.

4. A receiver as claimed in any of the preceding claims wherein each of said rotary indicators comprises a meter with a rotary pointer movable over a circular scale and phase angle integrating means comprising a mechanical cycle counter indicating the number of complete cycles of rotation of said pointer.

5. A receiver for a phase comparison radio navigation system of the kind in which radio frequency signals are radiated from two or more pairs of spaced transmitters, said transmitters including a common master transmitter normally radiating a signal of frequency  $6f$  and at least two slave stations normally radiating signals of different frequencies  $nf$  where  $n$  is 5, 8 or 9,  $f$  being the common fundamental frequency and wherein for short duration periods, each transmitter in turn radiates signals of  $5f$ ,  $6f$ ,  $8f$  and  $9f$  simultaneously, the radiations from the other transmitters being interrupted during these periods, said receiver comprising:—

(a) a frequency selective amplifier for each of the four frequencies,

(b) four oscillators having frequencies either equal to the respective received frequencies or being in the same ratio as the respective received frequencies, together with means locking the phases of the oscillator outputs to the respective received signals during the normal transmission periods;

(c) pulse generating means for deriving from the output of the oscillator locked to the  $6f$  signals a series of short duration pulses synchronised with the oscillator output, each pulse having a duration short compared with a cycle of the oscillator output;

(d) three frequency multipliers coupled respectively to the outputs of the three oscillators locked to the  $5f$ ,  $8f$  and  $9f$  signals and operative to provide three outputs respectively of frequencies equal to the respective least common multiple of the frequency of the associated oscillator and the frequency of that locked to the  $6f$  signals,

(e) means for generating, from each of the

nals of different multiples of a fundamental frequency  $f$  are radiated in fixed phase relation from spaced transmitting stations, the transmitting stations normally radiating one signal at a time, but in which periodically the normal transmissions are interrupted and each station, one at a time in sequence, radiates all the frequencies to form a multipulse for lane identification, the multipulse being in a fixed cyclic time sequence from the various stations, and in which the receiver is of the heterodyne type for receiving signals from chains operating on different fundamental frequencies, wherein the receiver has a frequency synthesiser including a stable oscillator and divider chain for providing a plurality of selectable different frequencies for heterodyning the received signals whereby phase comparison means operating at fixed frequencies may be used irrespective of the actual radiated frequencies of the transmitting stations being used.

#### WHAT WE CLAIM IS:—

1. A receiver for a phase comparison radio navigation system of the kind in which phase locked signals of different but harmonically related frequencies are normally radiated from fixed stations and in which periodically for a short duration each station in turn radiates signals of all the frequencies in fixed phase relation, the normal radiations from the other stations being interrupted, which receiver comprises receiving channels for each of the radiated signals, a number of oscillators corresponding to the number of different received frequencies, means for locking the oscillators in phase respectively with the received signals of different frequencies during the normal transmission periods, the oscillators having frequencies either equal to the respective received frequencies or being in the same ratio as the respective received frequencies, phase discriminators coupled to the oscillators to provide at least two sets of sine and cosine signals, each set being representative of the phase relation between a different pair of oscillators, a separate rotary indicator for each set of sine and cosine signals, the indicators being driven by the discriminators, a frequency divider dividing the output of one of the oscillators down to the fundamental frequency (i.e. the highest frequency of which all the oscillator frequencies are integral multiples), means for producing from the multiple signal transmissions from the various stations signals of said fundamental frequency, and a digital phase indicator including a digital counter and a clock source for indicating the phase relation between the divided down oscillator output and the successive signals of the same frequency derived from the multiple frequency transmissions from the various stations in turn.

2. A receiver as claimed in claim 1 and

for use with any one of a number of different chains of transmitting stations using different fundamental frequencies  $f$ , wherein there is provided a frequency synthesiser for producing a heterodyne signal of frequency  $\Delta$  such that  $\Delta = f + F$  where  $f$  is the fundamental frequency of any selected chain and  $F$  is the fixed fundamental frequency of the oscillators in the receiver, and wherein frequency converting means comprising a mixer and filter as provided for each received signal to convert the received signal which is a harmonic of  $f$ , to the corresponding harmonic of  $F$  by mixing with the corresponding harmonic of  $\Delta$  and taking the lower side band.

3. A receiver as claimed in either of the preceding claims wherein said digital phase indicator comprises a decimal digit display.

4. A receiver as claimed in any of the preceding claims wherein each of said rotary indicators comprises a meter with a rotary pointer movable over a circular scale and phase angle integrating means comprising a mechanical cycle counter indicating the number of complete cycles of rotation of said pointer.

5. A receiver for a phase comparison radio navigation system of the kind in which radio frequency signals are radiated from two or more pairs of spaced transmitters, said transmitters including a common master transmitter normally radiating a signal of frequency  $6f$  and at least two slave stations normally radiating signals of different frequencies  $nf$  where  $n$  is 5, 8 or 9,  $f$  being the common fundamental frequency and wherein for short duration periods, each transmitter in turn radiates signals of  $5f$ ,  $6f$ ,  $8f$  and  $9f$  simultaneously, the radiations from the other transmitters being interrupted during these periods, said receiver comprising:—

(a) a frequency selective amplifier for each of the four frequencies,

(b) four oscillators having frequencies either equal to the respective received frequencies or being in the same ratio as the respective received frequencies, together with means locking the phases of the oscillator outputs to the respective received signals during the normal transmission periods;

(c) pulse generating means for deriving from the output of the oscillator locked to the  $6f$  signals a series of short duration pulses synchronised with the oscillator output, each pulse having a duration short compared with a cycle of the oscillator output;

(d) three frequency multipliers coupled respectively to the outputs of the three oscillators locked to the  $5f$ ,  $8f$  and  $9f$  signals and operative to provide three outputs respectively of frequencies equal to the respective least common multiple of the frequency of the associated oscillator and the frequency of that locked to the  $6f$  signals,

(e) means for generating, from each of the



frequency multiplied signals, a pair of phase quadrature signals in fixed phase relation with the frequency multiplied signals from which they are generated;

5 (f) gating means controlled by the short duration pulses from said pulse generating means arranged to gate the three pairs of phase quadrature signals to provide three pairs of phase-controlled d.c. outputs;

10 (g) three rotary indicator means, each having a rotor taking up an angular position dependant on the relative magnitudes and polarities of d.c. signals applied to orthogonal coils, together with means applying the three pairs of phase-controlled d.c. outputs respectively to the three sets of orthogonal coils, whereby the rotor rotations are proportional to the phase angles between the received signals from the master station and the respective

20 slave stations during the normal transmissions; (h) cycle counting means coupled to the rotors of the three rotary indicator means to indicate integrated cycles of measured phase change;

25 (j) a frequency divider dividing the output of the oscillator locked to the 6f received signals down to the fundamental frequency (i.e. the highest frequency of which all the oscillator frequencies are integral multiples);

30 (k) means for producing from the multiple signal transmissions from the various stations signals of said fundamental frequency; and

l) a digital phase indicator including a

digital counter and a clock source for indicating the phase relation between the divided 35 down oscillator output and the successive signals of the same frequency derived from the multiple frequency transmissions from the various stations in turn.

6. A receiver as claimed in claim 5 wherein 40 said digital counter and clock source comprises digital counting means providing a readout which is the complement of a count of clock pulses during a time period started by a signal at the oscillator fundamental frequency 45 derived from a received multipulse signal from one of the slave stations and stopped by a stop count pulse signal at the same frequency derived from the oscillator locked to the normal master signal, said count 50 being compensated by a count started by a signal at the oscillator fundamental frequency derived from the master multipulse signal and stopped by the stop count pulse.

7. A receiver for a phase comparison radio 55 navigation system having rotary phase angle indicators with mechanical integrating means and digital counting means substantially as hereinbefore described with reference to the 60 accompanying drawings.

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