"A DATA PROCESSING METHOD, A DEVICE FOR CARRYING OUT SUCH DATA PROCESSING METHOD, A DATA CARRIER PRODUCED BY EXECUTING SUCH DATA PROCESSING METHOD, A DECODER FOR USE WITH SUCH DATA PROCESSING METHOD, AND A DEVICE INCLUDING SUCH A DECODER"

The present invention relates to a data processing method which has a high error-correcting capability for both burst errors and random errors. An earlier proposal for a data transmission method encompassing capability for correcting burst errors has used a so-called "cross-interleave feature". In this cross-interleave, a PCM (pulse code modulated) word of each of a plurality of parallel channels arranged in a first predetermined arrangement is fed to a first error correcting coder to generate therefrom a first check word series; this first check word series and the PCM data series of the plural channels are converted to a second predetermined arrangement; and one word contained in each of the PCM data series of the plural channels in the second predetermined arrangement is fed to a second error correcting coder thereby to generate a second check word series, whereby a double interleave (re-arrangement) is carried out per word unit. The interleave serves to reduce the number of erroneous words contained in a common error correcting block when the check word contained in the common error correcting block and the PCM data are transmitted after being dispersed and they are returned to the original arrangement thereof at the receiving side. In other words, when a burst error is generated during transmission, the burst error can be dispersed. If the above-mentioned interleave is performed twice, the first and second check words each form an error correcting block. For example, even if an error cannot be corrected by the first check words, the error can be corrected by the second check words, and vice versa. Therefore, the error correcting capability is improved. Even when in the aforementioned data processing method a word contains only one erroneous bit, the whole word is considered erroneous. Therefore, when received

data including relatively large numbers of random errors have to be dealt with, the above-mentioned cross-interleave does not always have a sufficient error correcting ability.

It is an object of the present invention to provide an error correcting data transmission method having both burst error and random error correcting capability.

According to the invention there is provided data processing method comprising the steps of:

receiving a data stream by receiving each time one data word of a data word series on each of a first plurality of parallel channels arranged in a first predetermined arrangement;

applying one word on each of said first plurality of parallel channels to a first error correcting coder to generate on the basis of a first generator matrix a first check word series;

applying mutually different delay time values to the words of said first check word series and the words of said data word series, after application to said first error correcting coder, to convert them to a second predetermined arrangement;

applying one word on each of said first plurality of channels and said first check word series in said second predetermined arrangement to a second error correcting coder to generate a second check word series on the basis of a second generator matrix;

applying each time one data word on each of a plurality of output channels equal to said first plurality and respective words of the first check word series and the second check word series on a second plurality of output channels; wherein the generation of each of the first and second check word series of k check words is based upon the following parity detection matrix H wherein in said first and second error correcting coders each word is formed of $\underline{m}$ bits and a check word series formed in an encoder completes an error correctable block to a total of $\underline{n}$ words, wherein $\underline{n} \leqslant 2^{m-1}$:

$$H=\begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ \alpha^{1} & \alpha^{2} & \alpha^{3} & \cdots & \alpha^{n-1} & \alpha^{n} \\ \alpha^{2} & \alpha^{4} & \alpha^{6} & \cdots & \alpha^{2(n-1)} & \alpha^{2n} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \alpha^{k-1} & \alpha^{(k-1)2} & \alpha^{(k-1)3} & \cdots & \alpha^{(k-1)(n-1)} & \alpha^{(k-1)n} \end{bmatrix}$$

or

$$H=\begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ 1 & \alpha^{1} & \alpha^{2} & \cdots & \alpha^{n-2} & \alpha^{n-1} \\ 1 & \alpha^{2} & \alpha^{4} & \cdots & \alpha^{2(n-2)} & \alpha^{2(n-1)} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 1 & \alpha^{k-1} & \alpha^{(k-1)2} & \cdots & \alpha^{(k-1)(n-2)} & \alpha^{(k-1)(n-1)} \end{bmatrix}$$

where α is a root which satisfies $F(x) = 0$ when $F(x)$ is an irreducible and primitive polynomial of degree m over a field GF(2). Obviously, for the second error correcting coder the value of n is larger than for the first error correcting coder.

It has been found that the processing method in accordance with the present invention (a kind of so-called "adjacent codes" or "b-adjacent code") has a high error correcting capability and may correct up to two word errors in one block. Also, 3 word errors or 4 word errors can be corrected when the position of an error can be determined, if combined with the above-mentioned multi-interleave. Further, when the error detecting code is used to correct only a one-word error, a decoder used therefore can be much simplified in construction.

The invention also relates to a device for carrying out the data processing method as mentioned hereabove, said device comprising:
first means for receiving an audio signal and generating therefrom a sequence of odd and even digitized samples;
second means for distributing each even digitized sample

into two even order words and distributing each odd digitized sample into two odd order words, and third means for presenting said odd and even order words to said first plurality of parallel channels. Thus a simple encoding device is advantageously provided.

The invention also relates to a data carrier produced by carrying out the method as indicated hereabove, the data carrier containing a sequence of blocks each block comprising a sequence of:

a third plurality, equal to half said first plurality, of words derived from even words of said data word series;

a fourth plurality of words derived from said first check word series;

a further third plurality of words derived from odd words of said data word series; and

a further fourth plurality of words derived from said second check word series. In this way a carrier for error-correcting data storage has been provided, for example for storing very-high quality audio signals.

The invention also relates to a decoder for use with a data processing method as mentioned hereabove, which decoder comprises:

a) input means for each time receiving on a plurality of receiving channels equal to said first plurality of output channels a data word series and in parallel therewith on a plurality of receiving channels equal to said second plurality of output channels a first check word series and a second check word series ;

b) a first decoder means for under control of said second check word series reproducing each time a first plurality of data words and a first check word series by means of a first syndrome generated therein;

c) delaying means for realigning said data words and first check word series by mutually different delay times thereamong;

d) a second decoder means for under control of said first check word series reproducing each time a first plurality of data words by means of a second syndrome generated therein; and

e) output means for each time providing as an output on a plurality of channels equal to said first plurality of output channels, a series of data words representing a data stream. In this way an advantageous and straightforwardly operating decoder has been provided.

The invention also relates to a device including a decoder as described hereabove, which device furthermore comprises: fourth means for receiving a serial data stream and for generating therefrom parallel data for the respective channels of said input means;
parallel to serial reconverting means for serializing the data words provided on said output channels, and digital to analog converting means for therefrom generating a continuous audio signal. Such device may represent, for example, a hifi record player of superior quality than the type hitherto in general use.

The present invention further relates to a data encoding/decoding method comprising the following method steps:

a) receiving a data stream by receiving each time one data word of a data word series on each of a first plurality of parallel channels according to a first predetermined arrangement,
b) applying one word on each of said first plurality of parallel channels to a first error correcting coder to generate on the basis of a first generator matrix a first check word series,
c) applying mutually different delay time values to the words of said first check word series and the words of said data word series, after application to said first error correcting coder to convert them to a second predetermined arrangement,
d) applying one word on each of said first plurality of channels and said first check word series in said second predetermined arrangement to a second error correcting coder to generate a second check word series on the basis of a second generator matrix,
e) outputting each time one data word on each of a plurality of

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output channels equal to said first plurality and the respective check words of said first check word series and said second check word series each on one of a second plurality of output channels, wherein the generation of each of the first and second check word series of $\underline{k}$ check words is based on the following parity check matrix H and in the first and the second error correcting coders each word consists of m bits and the series of check words generated in an encoder completes an error correctable block to a total of n words, wherein $n \leq 2^{m-1}$, and

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ \alpha^1 & \alpha^2 & \alpha^3 & \cdots & \alpha^{n-1} & \alpha^n \\ \alpha^2 & \alpha^4 & \alpha^6 & \cdots & \alpha^{2(n-1)} & \alpha^{2n} \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ \alpha^{k-1} & \alpha^{(k-1)2} & \alpha^{(k-1)3} & & \alpha^{(k-1)(n-1)} & \alpha^{(k-1)n} \end{bmatrix}$$

or

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ 1 & \alpha^1 & \alpha^2 & \cdots & \alpha^{n-2} & \alpha^{n-1} \\ 1 & \alpha^2 & \alpha^4 & \cdots & \alpha^{2(n-2)} & \alpha^{2(n-1)} \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 1 & \alpha^{(k-1)} & \alpha^{(k-1)2} & & \alpha^{(k-1)(n-2)} & \alpha^{(k-1)(n-1)} \end{bmatrix}$$

wherein α is a root of $F(x) = 0$, $F(x)$ being an irreducible and primitive polynomial of degree m over a Galois Field GF(2).

f) effecting a wordwise parallel to serial conversion for the onward transmission or storage of the data words and check words,

g) receiving or reproducing the data words and check words,

h) effecting a wordwise serial to parallel conversion to a number of parallel channels equal to the sum of said first and second pluralities, for reconstruction of the said second predetermined arrangement,

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i) effecting a first error detecting decoding process to the second predetermined arrangement according to a first parity detection matrix which is defined by a number of data words equal to said first plurality and a number of check words equal to the number of said first series,

j) delaying the reproduced data words and check words by mutually different delay times to reconstruct the said first predetermined arrangement,

k) effecting a second error detecting decoding process to the first predetermined arrangement according to a second parity detection matrix, which is defined by a number of data words equal to said first plurality, and

l) outputting of the reproduced data words.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Fig. 1 is a block diagram showing an example of an error correcting encoder to which the present invention is applied;

Fig. 2 is a block diagram showing an arrangement upon transmission;

Fig. 3 is a block diagram showing an example of an error correcting decoder;

Figs. 4 and 5 are respectively diagrams used to explain the operation of the error correcting decoder;

Fig. 6 is a block diagram of a second encoder;

Fig. 7 is a block diagram of a second decoder;

Fig. 8 is a block diagram of a third encoder;

Fig. 9 is a block diagram of a third decoder;

Fig. 10 is a block diagram of a fourth encoder;

Fig. 11 is a block diagram of a fourth decoder.

In the following, first an error code suitable for use in this invention will be described.

For explaining the error correcting code use is made of a vector representation or cyclic group representation. In the first place, an irreducible and primitive m'th order polynomial F(x) is considered over a Galois field GF(2). The theory of Galois fields is standard and will not be reconsidered here. The field GF(2) consists only of the elements "0" and "1". Suppose there exists a root α, which satisfies F(x) = 0. Now, an extension field $GF(2^m)$ which consists of 2^m different elements can be constructed by means of the quantities α^0, α^1, α^2 ... α^{m-1}, each being a different power of the root α (the set of these quantities is called the "base" of the field $GF(2^m)$. Note that the field $GF(2^m)$ also contains the zero element. The extension field $GF(2^m)$ is a polynomial ring with an m'th order irreducible polynominal F(x) over the field GF(2) as a modulo. Each element of $GF(2^m)$ can be expressed as a linear combination of $\alpha^0 = 1$, $\alpha = \{x\}$, $\alpha^2 = \{x^2\}$, --- $\alpha^{m-1} = \{x^{m-1}\}$. The general form of this expression is:

$$a_0 + a_1\{x\} + a_2\{x^2\} + \text{---} + a_{m-1}\{x^{m-1}\}$$
$$= a_0 + a_1\alpha + a_2\alpha^2 + \text{---} a_{m-1}\alpha^{m-1}$$

or

$$(a_{m-1}, a_{m-2}, \ldots a_2, a_1, a_0)$$

where a_{m-1}, a_{m-2}, ... a_1, a_0 are elements of GF(2). As an example, $GF(2^8)$ is considered; wherein the primitive and irreducible polynomial F(x) is, for example, $F(x) = x^8 + x^4 + x^3 + x^2 + 1$. All eight-bit data words may be expressed as follows:

$$a_7x^7 + a_6x^6 + a_5x^5 + a_4x^4 + a_3x^3 + a_2x^2 + a_1x + a_0 \text{ or}$$

$$(a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0).$$

Therefore, by way of example, a_7 is assigned to the MSB (most significant bit) side and a_0 is assigned to the LSB (least significant bit) side, respectively.

Since a_j belongs to GF(2), its element is 0 or 1.

Further, from the polynomial F(x) the following matrix T of (m x m) may be derived:

$$T=\begin{bmatrix} 0 & 0 & \cdots & 0 & a_0 \\ 1 & 0 & \cdots & 0 & a_1 \\ 0 & 1 & \cdots & 0 & a_2 \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & & 1 & a_{m-1} \end{bmatrix}$$

Alternatively, the elements of $GF(2^m)$ may be expressed by using a cyclic group, by considering that the remainder of $GF(2^m)$ except zero element, forms a multiplicative group with the order 2^{m-1}. If the elements of $GF(2^m)$ are expressed by using such cyclic group, the following is obtained.

$$0,\ 1\ (\equiv \alpha^{2m-1}),\ \alpha,\ \alpha^2,\ \alpha^3,\ \ldots\ldots \alpha^{2m-2}$$

In the present invention, when m bits form 1 word and n words form 1 block, k check words are generated based upon the following parity check matrix H.

$$H=\begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ \alpha^1 & \alpha^2 & \alpha^3 & \cdots & \alpha^{n-1} & \alpha^n \\ \alpha^2 & \alpha^4 & \alpha^6 & \cdots & \alpha^{2(n-1)} & \alpha^{2n} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \alpha^{k-1} & \alpha^{(k-1)2} & \alpha^{(k-1)3} & \cdots & \alpha^{(k-1)(n-1)} & \alpha^{(k-1)n} \end{bmatrix}$$

The parity check matrix H can be equally expressed by using the matrix T as follows:

$$H=\begin{bmatrix} I & I & I & \cdots & I & I \\ T^1 & T^2 & T^3 & \cdots & T^{n-1} & T^n \\ T^2 & T^4 & T^6 & \cdots & T^{2(n-1)} & T^{2n} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ T^{k-1} & T^{(k-1)2} & T^{(k-1)3} & \cdots & T^{(k-1)(n-1)} & T^{(k-1)n} \end{bmatrix}$$

where I is a unit matrix of (m x m) elements.

As described above, the expressions using the root α are fundamentally the same as that using a generating matrix. In this case, it is possible that all elements of the first column of each matrix are selected as 1 or I and the last column of each matrix can be omitted.

The error correcting code will be described in detail for an example wherein four (k=4) check words are used. In this case, if 1 block of received data is taken as a column vector $V = (W_1, W_2, W_3, \ldots W_n)$, 4 syndromes, S_1, S_2, S_3 and S_4 are generated at the receiving side in accordance with:

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \end{bmatrix} = H.V^T$$

$$\begin{cases} S_1 = \sum_{i=1}^{n} W_i \\ S_2 = \sum_{i=1}^{n} T^i W_i \\ S_3 = \sum_{i=1}^{n} T^{2i} W_i \\ S_4 = \sum_{i=1}^{n} T^{3i} W_i \end{cases}$$

Each block contains 4 check words ($p = W_{n-3}$, $q = W_{n-2}$, $r = W_{n-1}$, $s = W_n$). These check words are generated at the transmitting side according to:

$$\begin{cases} p + q + r + s = \sum W_i \\ T^{n-3}p + T^{n-2}q + T^{n-1}r + T^n s = \sum T^i W_i \\ T^{2n-6}p + T^{2n-4}q + T^{2n-2}r + T^{2n}s = \sum T^{2i} W_i \\ T^{3n-9}p + T^{3n-6}q + T^{3n-n}r + T^{3n}s = \sum T^{3i} W_i \end{cases}$$

$$\begin{cases} p + q + r + s = \sum W_i & = a \\ p + Tq + T^2 r + T^3 s = \sum T^{i-n+3} W_i & = b \\ p + T^2 q + T^4 r + T^6 s = \sum T^{2(i-n+3)} W_i & = c \\ p + T^3 q + T^6 r + T^9 s = \sum T^{3(i-n+3)} W_i & = d \end{cases}$$

where $\sum$ is $\sum_{i=1}^{n-4}$.

The check words can be obtained by solving these simultaneous equations. The calculation is defined in $GF(2^m)$ and the result is as follows:

$$p = \frac{T^6 a + (T^3+T^4+T^5)b + (T+T^2+T^3)c + d}{(1+T)(1+T^2)(1+T^3)}$$

$$q = \frac{T^5 a + (T^2+T^3+T^5)b + (1+T^2+T^3)c + d}{T^2(1+T^4)}$$

$$r = \frac{T^4 a + (T+T^3+T^4)b + (1+T+T^3)c + d}{T^3(1+T^4)}$$

$$s = \frac{T^3 a + (T+T^2+T^3)b + (1+T+T^2)c + d}{T^3(1+T)(1+T^2)(1+T^3)}$$

$$p = \left[T^6 \sum W_i + (1+T+T^2)\cdot\left\{\sum T^{i-n+6} W_i + \sum T^{2(i-n+3)+1} W_i\right\} + \sum T^{3(i-n+3)} W_i\right] \cdot (1+T)^{-1} \cdot (1+T^2)^{-1} \cdot (1+T^3)^{-1};$$

$$q = \left[T^5 \sum W_i + (1+T+T^3)\sum T^{i-n+5} W_i + (1+T^2+T^3) \cdot \sum T^{2(i-n+3)} W_i + \sum T^{3(i-n+3)} W_i\right] \cdot T^{-2} \cdot (1+T^4)^{-1};$$

$$r = \left[T^4 \sum W_i + (1+T^2+T^3)\sum T^{i-n+4} \cdot W_i + (1+T+T^3) \cdot \sum T^{2(i-n+3)} W_i + \sum T^{3(i-n+3)} W_i\right] T^{-3} \cdot (1+T^4)^{-1};$$

$$s = \left[T^3 \sum W_i + (1+T+T^2)\left\{\sum T^{i-n+4} W_i + \sum T^{2(i-n+3)} W_i\right\} + \sum T^{3(i-n+3)} W_i\right] \cdot T^{-3} \cdot (1+T)^{-1} \cdot (1+T^2)^{-1} \cdot (1+T^3)^{-1} .$$

Next, an error correction will be described when the data including the check words generated as above are transmitted and then received. In this case, it is assumed that a pointer representing an error position is not used.

(1) If there is no error, $S_1 = S_2 = S_3 = S_4 = 0$.

(2) If there is one word error (an error pattern is taken as ei), $S_1 = ei$, $S_2 = T^i ei$, $S_3 = T^{2i} ei$ and $S_4 = T^{3i} ei$.

Thus, the following equations are established.

$$\begin{cases} T^i S_1 = S_2 \\ T^i S_2 = S_3 \\ T^i S_3 = S_4 \end{cases}$$

At this time, the syndrome S_1 is the error pattern ei itself.

(3) In the case of 2 word errors (ei and ej):

$$\begin{cases} S_1 = ei + ej \\ S_2 = T^i ei + T^j ej \\ S_3 = T^{2i} ei + T^{2j} ej \\ S_4 = T^{3i} ei + T^{3j} ej \end{cases}$$

The above equations can be modified as follows:

$$\begin{cases} T^j S_1 + S_2 = (T^i + T^j)\, ei \\ T^j S_2 + S_3 = T^i (T^i + T^j)\, ei \\ T^j S_3 + S_4 = T^{2i} (T^i + T^j)\, ei \end{cases}$$

Accordingly, if the following equations are established, 2 word errors are discriminated.

$$\begin{cases} T^i (T^j S_1 + S_2) = T^j S_2 + S_3 \\ T^i (T^j S_2 + S_3) = T^j S_3 + S_4 \end{cases}$$

The error patterns at this time are expressed as follows:

$$ei = \frac{S_1 + T^{-j} S_2}{1 + T^{i-j}}, \quad ej = \frac{S_1 + T^{-i} S_2}{1 + T^{j-i}}$$

(4) In the case of 3 word errors (ei, ej and ek):

$$\begin{cases} S_1 = ei + ej + ek \\ S_2 = T^i ei + T^j ej + T^k ek \\ S_3 = T^{2i} ei + T^{2j} ej + T^{2k} ek \\ S_4 = T^{3i} ei + T^{3j} ej + T^{3k} ek \end{cases}$$

The above equations can be modified as follows:

$$\begin{cases} T^k S_1 + S_2 = (T^i + T^k) ei + (T^j + T^k)\, ej \\ T^k S_2 + S_3 = T^i (T^i + T^k) ei + T^j (T^j + T^k)\, ej \\ T^k S_3 + S_4 = T^{2i} (T^i + T^k) ei + T^{2j} (T^j + T^k)\, ej \end{cases}$$

Accordingly, if the following equation is established, 3 word errors can be discriminated since the conditions $S_1 \neq 0$, $S_2 \neq 0$, $S_3 \neq 0$ are satisfied.

$$T^j(T^kS_1+S_2)+(T^kS_2+S_3) = T^j(T^kS_2 + S_3) + (T^kS_3 + S_4)$$

The respective error patterns at this time are expressed as follows:

$$\begin{cases} ei = \dfrac{S_1 + (T^{-j} + T^{-k}).S_2 + T^{-j-k}S_3}{(1+T^{i-j})(1+T^{i-k})} \\ ej = \dfrac{S_1 + (T^{-k} + T^{-i})\,S_2 + T^{-k-i}S_3}{(1+T^{j-i})\,(1+T^{j-k})} \\ ek = \dfrac{S_1 + (T^{-i} + T^{-j})S_2 + T^{-i-j}S_3}{(1+T^{k-i})\,(1+T^{k-j})} \end{cases}$$

As described above, all 3-word errors can be corrected without using the pointer.

If the pointer is used and error positions (i, j, k, 1) are known thereby, 4 word errors can also be corrected.

Further, if the number k of the check words is increased, the error correcting ability can be improved even further.

Now, an example of the present invention will be described with reference to the accompanying drawings in which the invention is applied to the recording and reproducing of an audio PCM signal.

Fig. 1 shows, as a whole, an error correcting encoder provided in the recording system whose input side is supplied with an audio PCM signal. The audio PCM signal is provided in such a manner that left and right stereo signals are respectively sampled at a sampling frequency f_s (for example, 44.1 kHz) and each sampled value is converted into a sixteen-bit number expressed in two's complement notation. Accordingly, the left audio channel provides a string of 16-bits PCM data (L0, L1, L2 ...) and

the right audio channel provides a further string of 16-bits PCM data (R0, R1, R2 ...). The PCM data of the left and right audio channels are each multiplexed-by-word by a device not shown, cyclically over a respective plurality of six encoding channels. Therefore, totally 12 channels of PCM data series are input to the error correcting encoder. At a given or predetermined instant, e.g. 12 numbers such as L_{6n}, R_{6n}, L_{6n+1}, R_{6n+1}, L_{6n+2}, R_{6n+2}, L_{6n+3}, R_{6n+3}, L_{6n+4}, R_{6n+4}, L_{6n+5}, R_{6n+5} are input. In the example each 16-bit number is divided into eight more significant bits and eight less significant bits. These eight-bit groups will be called "words" hereinafter. Consequently, the twelve numbers are processed according to twenty-four parallel channels. Now, one 16-bit number of the PCM data series is indicated as W_i, its upper 8 bits are expressed as $Wi_{i,A}$ and its lower bits are expressed as $W_{i,B}$ respectively. For example, the number L_{6n} is divided into two words $W_{12n,A}$ and $W_{12n,B}$. Note also the earlier use of n as a dimension of the matrixes H.

The PCM data series of 24 channels are firstly fed to an even and odd interleaver 1. If n = 0, 1, 2, ---, the words L_{6n} (i.e. $W_{12n,A}$ and $W_{12n,B}$), R_{6n} (i.e. $W_{12n+1,A}$ and $W_{12n+1,B}$), L_{6n+2} (i.e. $W_{12n+4,A}$ and $W_{12n+4,B}$), R_{6n+2} (i.e. $W_{12n+5,A}$ and $W_{12n+5,B}$), L_{6n+4} (i.e. $W_{12n+8,A}$ and $W_{12n+8,B}$) and R_{6n+4} (i.e. $W_{12n+9,A}$ and $W_{12n+9,B}$) constitute the even order words, while the other words likewise are odd order words. The PCM data series consisting of even order words are respectively delayed through respective delay circuits or delay lines 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 6A, 6B, 7A and 7B of the even and odd interleaver 1 by a one word interval. Further, in the even and odd interleaver 1 such a conversion is carried out that 12 data series consisting of even order words occupy 1st to 12th transmission channels and 12 data series consisting of odd order words occupy 13th to 24th transmission channels, respectively.

The even and odd interleaver 1 serves to avoid the situation wherein more than two adjacent numbers of any (left or right) audio channel would be erroneous and the errors would then be incorrectable. This can be understood as follows. Three adjacent numbers L_{i-1}, L_i, L_{i+1} will be considered by way of example. Where the number L_i is erroneous and non-correctable, the number L_{i-1} or L_{i+1}, or both, should be correct. In this way, the erroneous number L_i may be restored by replacing it by the directly preceding number L_{i-1} or by the directly following number L_{i+1} or by the average value of L_{i-1} and L_{i+1}. In many instances this provides an acceptable approximation of the "true" value of L_i. The delay lines 2A, 2B ... 7A, 7B of the even and odd interleaver 1 are provided for adjacent words to be contained in different error correcting blocks. Further, the reason why the transmission channels for each of the data series consisting of the even order words and the data series consisting of odd order words are gathered is that when the data series are interleaved, the distance between the recording positions of the adjacent even and odd order words are selected as far apart as possible.

At the output of the even and odd interleaver 1, the PCM data series of 24 channels appear in a first predetermined arrangement. The words that have been delayed by a one word interval have been indicated by an index that is twelve points lower at the output of interleaver 1. From the respective PCM data series, each time four first check words Q_{12n}, Q_{12n+1}, Q_{12n+2}, Q_{12n+3} are derived from an error correcting block of data words. This error correcting block therefore comprises the words:

$(W_{12n-12,A}; W_{12n-12,B}; W_{12n+1-12,A}; W_{12n+1-12,B};$
$W_{12n+4-12,A}; W_{12n+4-12,B}; W_{12n+5-12,A}; W_{12n+5-12,B};$
$W_{12n+8-12,A}; W_{12n+8-12,B}; W_{12n+9-12,A}; W_{12n+9-12,B};$
$W_{12n+2,A}; W_{12n+2,B}; W_{12n+3,A}; W_{12n+3,B}; W_{12n+6,A};$
$W_{12n+6,B}; W_{12n+7,A}; W_{12n+7,B}; W_{12n+10,A}; W_{12n+10,B};$

$W_{12n+11,A}$; $W_{12n+11,B}$; Q_{12n}; Q_{12n+1}, Q_{12n+2}, Q_{12n+3}).

In the first coder 8 therefore, twenty-four data words of 8 bits each are encoded to yield four check words. Consequently, the fixed parameter values of the code used here are n = 28, m = 8, k = 4.

24 PCM data series and 4 check word series are fed to a second interleaver 9. In this interleaver 9, the positions of the channels are changed such that the check word series are located between the PCM data series consisting of the even order words and the PCM data series consisting of the odd order words, and thereafter the delay process for this interleaving is performed. This delay process is such that 27 transmission channels except the first transmission channel are delayed by delay lines with delay amounts of 1D, 2D, 3D, 4D, --- 26D and 27D (where D is a unit delay amount), respectively.

At the output of the interleaver 9 28 data series in a second predetermined arrangement appear. From the respective data series, the data words are derived one by one. Then, the words are fed to a coder 10 which then produces second check words P_{12n}, P_{12n+1}, P_{12n+2} and P_{12n+3}. An error correcting block including the second check words and consisting of 32 words is listed hereafter. Note that a delay by jD in a coding channel will decrease the value of the index of W by an amount of 12.j.D:

$W_{12n-12,A}$; $W_{12n-12(D+1),B}$;

$W_{12n+1-12(2D+1),A}$; $W_{12n+1-12(3D+1),B}$;

$W_{12n+4-12(4D+1),A}$; $W_{12n+4-12(5D+1),B}$;

$W_{12n+5-12(6D+1),A}$; ...

.

.

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$W_{12n+9-12(10D+1),A}$; $W_{12n+9-12(11D+1),B}$;

$Q_{12n-12(12D)}$; $Q_{12n+1-12(13D)}$; $Q_{12n+2-12(14D)}$; $Q_{12n+3-12(15D)}$

$W_{12n+2-12(16D)}$; ...

.

.

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$W_{12n+11-12(26D)}$; $W_{12n+11-12(27D)}$;

P_{12n}; P_{12n+1}; P_{12n+2}; P_{12n+3}.

An interleaver 11 is provided which includes delay lines providing 1 word delay period for the even order channels of 32 data series including the first and second check words, and also inverters 12, 13, 14 and 15 are provided for the second check word series. The interleaver 11 serves to avoid such a defect that a burst error interval which during transmission would cross the boundary between adjacent blocks would also be apt to influence so many words in an error correcting block that the correction thereof would be rendered impossible. The inverters 12, 13, 14 and 15 serve to avoid such an erroneous operation that all the data in one block are made "0" by a drop-out during transmission and/or recording and this is discriminated correct in the reproducing system, for example, as an interval of silence in the audio representation. Such silence interval would therefore yield a second check word series different from zero. The finally produced code words are listed in the last column of the figure inclusive of there respective delays now incurred.

The finally produced block of 24 PCM data words and 8 check words is serialized by a parallel to serial converter not shown. A synchronizing signal of 16 bits is added at the beginning thereof to form one block which for convenience will be referred to as a transmission block as shown in Fig. 2 and then the block thus made is transmitted and/or recorded. In Fig. 2, for the sake of brevity, a word derived from the i'th channel is shown as u_i.

Practical examples of the signal processing system, may be magnetic recording and reproducing apparatus, rotary disc apparatus and so on.

The above coder 8 relates to the above-mentioned error correcting code wherein the values of the fixed code parameters are m = 8, n = 28 and k = 4. For the encoder 10 the corresponding fixed code parameters have the values m = 8, n = 32 and k = 4. Thus the complete block of Fig. 2 comprises 32 x 8 + 16 = 272 bits.

At the decoding station, first the synchronization header is removed by a device not shown. The remaining reproduced 32 code words of each transmission block , are applied to the input of an error correcting decoder shown in Fig. 3. Due to the reproducing process there is a possibility that the reproduced data contain an error. If there is no error, 32 words fed to the input of the decoder are identical to the 32 words that had appeared at the output of the error correcting encoder. At the error correcting decoder, the de-interleave process complementing the interleave process at the encoder is performed to return the order of the data to the original order and then the error correcting process is carried out.

At first, as shown in Fig. 3, a de-interleaver 16 is provided in which delay lines, each having a delay period of 1 word, are provided for the odd order transmission channels and inverters 17, 18, 19 and 20 are provided for the second check word series. The outputs from the de-interleaver 16 and inverters 17 to 20 are fed to a first decoder 21. At this decoder 21, syndromes S_{11}, S_{12}, S_{13} and S_{14} are generated from a parity detection matrix H_{c1} and input 32 words V^T as shown in Fig. 4, and the above-mentioned error correction is performed based upon the syndromes. In Fig. 4, α is an element of $GF(2^8)$, being a root of the primitive and irreducible polynomial of degree m, $F(x) = x^8+x^4+x^3+x^2+1$. From the decoder 21, 24 PCM data series and 4 check word series are derived. At every word of the data series, a pointer (at least 1 bit) is added which shows whether or not there is an error. The pointer bit or bits are transported in similar

way as the further bits of data words and check words.

The output data series from the decoder 21 are fed to a de-interleaver 22 which serves to cancel the effects of delay process performed by the interleaver 9 in the error correcting encoder and in which delay lines with different delay periods of 27D, 26D, 25D, --- 2D and 1D are provided for the 1st to 27th transmission channels. The output from the de-interleaver 22 is fed to a second decoder 23 in which syndromes S_{21}, S_{22}, S_{23} and S_{24} are generated from a parity detection matrix H_{c2} and input 28 words V^T as shown in Fig. 5 and the above-mentioned error correction is carried out based upon the syndromes. In the decoder 23, the pointer relating to a word whose error is corrected is erased, but the pointer relating to a word whose error cannot be corrected by the decoder 23 is not erased.

The data series appearing at the output of the decoder 23 are fed to an even and odd de-interleaver 24, in which the PCM data series consisting of the even order words and the PCM data series consisting of the odd order words are re-arranged such that they are positioned at the alternative transmission channels and delay lines of 1 word delay amount that are provided for the PCM data series consisting of the odd order words. At the output of the even and odd de-interleaver 24, the PCM data series which have the arrangement and predetermined order transmission channels entirely the same as those fed to the input of the error correcting encoder are obtained. Though not shown in Fig. 3, a correcting circuit is provided at the next stage of the even and odd de-interleaver 24 to carry out a correction, for example, mean value interpolation so that the error, which is not corrected by the decoders 21 and 23 is made inconspicuous.

In the error correcting decoder shown in Fig. 3, the error correction using the first check words P_{12}, P_{12n+1}, P_{12n+2} and P_{12n+3} and the error correction using the second check words Q_{12n}, Q_{12n+1}, Q_{12n+2} and Q_{12n+3}

are respectively carried out one time. If the above error corrections are respectively carried out more than twice, the error correcting capability is increased and fewer errors remain uncorrected.

In the embodiment described the delay intervals in interleaver 9 differ by each time an amount D in successive channels, but it is possible to employ an irregular variation in delay amount other than the above regular sequence. Further, similar to the second check words Pi which are calculated by using not only the PCM data but also the first check words Q_i, also the first check words Q_i may be codetermined by the second check words P_i. This may be effected by feeding back the second check words to an input of the coder producing the first check words.

The error correction code described hereabove may correct, for example, up to two word errors without using the pointer showing the error position, and a burst error is dispersed by the cross-interleave, so that both the random errors and burst errors can be effectively corrected.

Furthermore, as the number of correctable error words increases, the decoding algorithm becomes more complicated. When only 1 word error is correctable, a very simple construction of the decoder is enough. Accordingly, it becomes clear that error correcting decoders having respective correcting abilities from low error correcting ability to high error correcting ability or may be constructed.

The apparatus and method as shown and explained herebefore may be modified in several ways that may offer specific advantages:

a) In Fig. 1 the parity words Q(12n), Q(12n+1), Q(12n+2), Q(12n+3) may be inverted in the same way as parity words P(12n) through P(12n+3); however, the encoder 10 would still receive the non-inverted parity words Q(12n) through Q(12n+3). In corresponding manner,

the decoder of Fig. 3 would receive the inverted parity words $\overline{Q_{12n-12(12D)}}$ ... through $\overline{Q_{12n+3-12(15D+1)}}$. These would be re-inverted again before entering decoder (21).

b) In Fig. 4 the second row may be changed from $(\alpha^{32}, \alpha^{31}, \ldots \alpha^{3}, \alpha^{2}, \alpha^{1})$ into $(\alpha^{31}, \alpha^{30}, \ldots, \alpha^{2}, \alpha^{1}, 1)$. In Fig. 5, in corresponding manner, the second row may be changed from $(\alpha^{28}, \alpha^{27}, \ldots \alpha^{3}, \alpha^{2}, \alpha^{1})$ into $(\alpha^{27}, \alpha^{26}, \ldots \alpha^{2}, \alpha^{1}, 1)$. Furthermore in both Figs. 4, 5 the matrix in α may have front side and back side reversed. In that way, the second through fourth rows would start with low powers of α and end with high powers of α.

c) The apparatus and method may advantageously be used in a high-fidelity system. The encoding is executed first. The data may be stored on an audio disc, audio tape, or the like. Alternatively, or in combination therewith, the data may be transmitted via a communication channel, or broadcasted. At a receiving end, the decoding method and apparatus are operated, and possible errors are corrected. Finally, high-fidelity amplification and reproduction are effected.

Figs. 6, 7 show a block diagram of a second encoder and second decoder, respectively. The main difference between Fig. 1 and Fig. 6 lies in interleaver 30, which now has respective delays over two word intervals as indicated by the numerals "2". Furthermore, the cyclic transposition of the coding channels is different. At the input side, each time two channels are rearranged together, while after 8 channels a next cycle is started. Thus three cycles of 8 channels are present. At the output side, after 6 channels a new cycle is started. Thus, four cycles of 6 channels each are present. A second difference occurs relative to encoder 32, which is situated in the middle between the two groups of code channels. In this way the number of crossings is diminished: element 34 now comprises delay elements only. For example D = 6 word intervals. Delay element 38 has

delay introduced in the odd channels as in contradistinction to Fig. 1. Finally, all check words are inverted. Fig. 7 again follows directly from the arrangement of Fig. 6.

Figs. 8, 9 show a block diagram of a third encoder and third decoder, respectively. Fig. 8 is identical to Fig. 6, except for the interleaver 40. Here, the first six channels are delayed by two word intervals, and also the third group of six channels is delayed by two word intervals. The other coding channels are not delayed in interleaver 40. Furthermore, the transposition of the coding channels is different. At the input side, each time two channels are rearranged together, while the next cycle is only started after twelve coding channels. Thus two cycles of twelve channels are present.

At the output side, after four channels a new cycle is started. Thus, six cycles of four channels are present. Again the arrangement of Fig. 9 follows directly from the arrangement of Fig. 8.

Figs. 10 , 11 show a block diagram of a fourth encoder and fourth decoder, respectively. Fig. 10 is identical to Fig. 8, except for the interleaver 42. Here, the coding channels are distributed over three groups. The coding channels of the first group are not delayed in the interleaver 42. The channels of the second group comprise a delay element over one word interval. The coding channels of the third group comprise a delay element over two word intervals. No rearrangement of the channels is executed. Again the arrangement of Fig. 11 follows directly from the arrangement of Fig. 10.

In this way changing between Figs. 7, 9, 11 or 6, 8, 10 requires only the modification of a part of the arrangement. In this respect, Figs. 6/7 show an arrangement that is most suitable for use with two audio channels (stereophonic use), Figs. 8/9 show an arrangement that is most suitable for use with three audio channels and Figs. 10/11 show an arrangement that is most suitable

for use with four audio channels (quadrophonic use). In each of these cases, the interpolation of irrecovered audio signals between correct audio signals offers an advantageous remedy.

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CLAIMS:

1. A data processing method comprising the steps of:

a) receiving a data stream by receiving each time one data word of a data word series on each of a first plurality of parallel channels arranged in a first predetermined arrangement;

b) applying one word on each of said first plurality of parallel channels to a first error correcting coder to generate on the basis of a first generator matrix a first check word series;

c) applying mutually different delay time values to the words of said first check word series and the words of said data word series, after application to said first error correcting coder, to convert them to a second predetermined arrangement;

d) applying one word on each of said first plurality of channels and said first check word series in said second predetermined arrangement to a second error correcting coder to generate a second check word series on the basis of a second generator matrix;

e) applying each time one data word on each of a plurality of output channels equal to said first plurality and respective words of the first check word series and the second check word series on a second plurality of output channels;

f) wherein the generation of each of the first and second check word series of k check words is based on the following parity detection matrix H wherein in said first and second error correcting coders each word is formed of $\underline{m}$ bits and a check word series formed in an encoder completes an error correctable block to a total of $\underline{n}$ words, wherein $\underline{n} \leqslant 2^{m-1}$:

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ \alpha^1 & \alpha^2 & \alpha^3 & \cdots & \alpha^{n-1} & \alpha^n \\ \alpha^2 & \alpha^4 & \alpha^6 & \cdots & \alpha^{2(n-1)} & \alpha^{2n} \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ \alpha^{k-1} & \alpha^{(k-1)2} & \alpha^{(k-1)3} & & \alpha^{(k-1)(n-1)} & \alpha^{(k-1)n} \end{bmatrix}$$

or

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ 1 & \alpha^1 & \alpha^2 & \cdots & \alpha^{n-2} & \alpha^{n-1} \\ 1 & \alpha^2 & \alpha^4 & \cdots & \alpha^{2(n-2)} & \alpha^{2(n-1)} \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 1 & \alpha^{k-1} & \alpha^{(k-1)2} & & \alpha^{(k-1)(n-2)} & \alpha^{(k-1)(n-1)} \end{bmatrix}$$

where α is a root which satisfies $F(x) = 0$ when $F(x)$ is an irreducible and primitive polynomial of degree m over a field GF(2).

2. A method as claimed in Claim 1, wherein said second check word series is inverted before being applied to the output channels.

3. A method as claimed in Claim 1, wherein, after application thereof to said second error correcting coder but before being applied to the output channels, said first check word series is inverted.

4. A method as claimed in Claim 1, wherein in step c) a first group of the words of said data word series have delay times in a first set of delay time values, said first check word series have delay times in a second set of delay time values, and a further group of words, equal in number to said first group of the words of said data word series have delay times in a third set of delay time values, each member of said third set having a larger delay time value than each member of said second set, each member of said second set having a larger delay time value than each member of said first set.

5. A method in Claim 1, wherein data in the data stream is formed into a sequence of odd and even samples, the odd samples being distributed into two pairs of odd order words and the even samples being distributed into two pairs of even order words and after reception but before application thereof to said first

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error correcting coder a relative delay of one word interval is imposed between respective even order words of said data word series and odd order words of said data word series.

6. A method as claimed in Claim 1, wherein a relative delay of one word interval is imposed between the words on respective even channels thereof and respective odd channels thereof before being applied to the first and second pluralities of output channels.

7. A method as claimed in Claim 4 wherein after reception but before application thereof to said first error correcting coder a relative delay of mutually equal value of at least one word interval is imposed to the words forming part of said first group with respect to said further group.

8. A device for carrying out the data processing method as claimed in any one of Claims 1 to 6, comprising:

first means for receiving an audio signal and generating therefrom a sequence of odd and even digitized samples;

second means for distributing each even digitized sample into two even order words and distributing each odd digitized sample into two odd order words, and

third means for presenting said odd and even order words to said first plurality of parallel channels.

9. A device as claimed in Claim 8, wherein said first means is adapted for operating on the left and right mono-aural signals of a stereo audio signal to generate the sequence of odd and even digitized samples respectively.

10. A data carrier produced by carrying out the method as claimed in any one of Claims 1 to 7 and containing a sequence of blocks each block comprising a sequence of:

a third plurality, equal to half said first plurality, of words derived from even words of said data word series;

a fourth plurality of words derived from said first check word series;

a further third plurality of words derived from odd words of said data word series, and

a further fourth plurality of words derived from said second check word series.

11. A data carrier as claimed in Claim 10, wherein each block furthermore comprises a synchronization header.

12. A decoder for use with a data processing method according to any of Claims 1 to 7, said decoder comprising

a) input means for each time receiving on a plurality of receiving channels equal to said first plurality of output channels a data word series and in parallel therewith on a plurality of receiving channels equal to said second plurality of output channels a first check word series and a second check word series;

b) a first decoder means for under control of said second check word series reproducing each time a first plurality of data words and a first check word series by means of a first syndrome generated therein;

c) delaying means for realigning said data words and first check word series by mutually different delay times thereamong;

d) a second decoder means for under control of said first check word series reproducing each time a first plurality of data words by means of a second syndrome generated therein; and

e) output means for each time providing as an output on each of a plurality of channels equal in number to said first plurality of output channels a data word of a series of data words; a sequence of the data words representing a data stream.

13. A decoder as claimed in Claim 12, for use with a method according to Claims 2 or 3, wherein said input means comprise reinverting means responsive to inverted check words received.

14. A decoder as claimed in Claim 12, for use with a method according to Claim 6, wherein said input means comprise second delaying means for compensating for the relative delay incurred between even data channels and odd data channels.

15. A decoder as claimed in Claim 12, for use with a method according to Claim 5, wherein said output means comprise third delaying means for compensating the relative delay incurred between even order words and odd order words.

16. A device including a decoder as claimed in any one of the Claims 12 to 15, said device furthermore comprising: fourth means for receiving a serial data stream and for generating therefrom parallel data for the respective channels of said input means; parallel to serial reconverting means for serializing the data words provided on said output channels, and digital to analog converting means for therefrom generating a continuous audio signal.

17. A data encoding/decoding method comprising the following method steps:

a) receiving a data stream by receiving each time one data word of a data word series on each of a first plurality of parallel channels according to a first predetermined arrangement,

b) applying one word on each of said first plurality of parallel channels to a first error correcting coder to generate on the basis of a first generator matrix a first check word series,

c) applying mutually different delay time values to the words of said first check word series and the words of said data word series, after application to said first error correcting coder to convert them to a second predetermined arrangement,

d) applying one word on each of said first plurality of channels and said first check word series in said second predetermined arrangement to a second error correcting coder to generate a second check word series on the basis of a second generator matrix,

e) outputting each time one data word on each of a plurality of output channels equal to said first plurality and the respective check words of said first check word series and said second check word series each on one of a second plurality of output channels, wherein the generation of each of the first and second check word series of $\underline{k}$ check words is based on the following parity check matrix H and in the first and the second error correcting coders each word consists of m bits and the series of check words generated in an encoder completes an error correctable block to a total of n words, wherein $n \leq 2^{m-1}$, and

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ \alpha^1 & \alpha^2 & \alpha^3 & \cdots & \alpha^{n-1} & \alpha^n \\ \alpha^2 & \alpha^4 & \alpha^6 & \cdots & \alpha^{2(n-1)} & \alpha^{2n} \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ \alpha^{k-1} & \alpha^{(k-1)2} & \alpha^{(k-1)3} & & \alpha^{(k-1)(n-1)} & \alpha^{(k-1)n} \end{bmatrix}$$

or

$$H = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & 1 \\ 1 & \alpha^1 & \alpha^2 & \cdots & \alpha^{n-2} & \alpha^{n-1} \\ 1 & \alpha^2 & \alpha^4 & \cdots & \alpha^{2(n-2)} & \alpha^{2(n-1)} \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 1 & \alpha^{(k-1)} & \alpha^{(k-1)2} & & \alpha^{(k-1)(n-2)} & \alpha^{(k-1)(n-1)} \end{bmatrix}$$

wherein α is a root of $F(x) = 0$, $F(x)$ being an irreducible and primitive polynomial of degree m over a Galois Field GF(2),

f) effecting a wordwise parallel to serial conversion for the onward transmission or storage of the data words and check words,

g) receiving or reproducing the data words and check words,

h) effecting a wordwise serial to parallel conversion to a number of parallel channels equal to the sum of said first and second pluralities, for reconstruction of the said second predetermined arrangement,

i) effecting a first error detecting decoding process to the second predetermined arrangement according to a first parity detection matrix which is defined by a number of data words equal to said first plurality and a number of check words equal to the number of said first series,

j) delaying the reproduced data words and check words by mutually different delay times to reconstruct the said first predetermined arrangement,

k) effecting a second error detecting decoding process to the first predetermined arrangement according to a second parity detection matrix, which is defined by a number of data words equal to said first plurality, and

l) outputting of the reproduced data words.

18. A method as claimed in Claim 17, wherein in step j) a first group of the first plurality of data words is given delays in a first set of delay time values, the first check word series is given delays in a second set of delay time values, and a second group of data words equal in number to the first group is given delays in a third set of delay time values, and wherein each element of the third set has a delay time value that is larger than the delay time value of each element of the second set and each element of the second set has a delay time value that is larger than the delay time value of each element of the first set.

19. A method as claimed in Claim 17 or 18, wherein in the first predetermined arrangement mutually equal relative delays over a predetermined number of word intervals are introduced between even-numbered data words and odd-numbered data words in the data stream and after the reproduction by means of the second parity check matrix mutually equal, relative delays over a predetermined number of word intervals are introduced between the odd-numbered data words and the even numbered data words to re-align the data words.

20. A method as claimed in Claim 17, wherein at the reception or reproduction of the data words and check words mutually equal relative delays over a predetermined number of word intervals are introduced between the words entered into the even channels and those introduced into the odd channels.

21. An encoder for use in encoding data words in accordance with a processing method as claimed in Claim 17, the encoder comprising:

a) input means for receiving a serial data stream and for recurrently multiplexing the words of said data stream over said first plurality of parallel channels;

b) a first encoder means for recurrently generating a first check word series associated with a plurality of data words;

equal to said first plurality by means of implementing said first generator matrix;

c) delay means fed by said first encoder means for producing said second predetermined arrangement;

d) a second encoder means for recurrently generating a second check word series associated with a plurality of data words equal to said first plurality and a plurality of check words equal to the number in said first check word series by means of implementing said second generator matrix; and

e) output means for outputting in parallel a second plurality of data words and check words.

22. An apparatus comprising an encoder as claimed in Claim 21, further comprising a parallel to serial reconverting means fed by said output means.

23. A decoder for use with a data processing method as claimed in Claim 17, wherein the decoder comprises:

a) input means for recurrently receiving a series of data words in a number of input channels equal to said first plurality and in parallel therewith in a number of input channels equal to said second plurality, a first check word series and a second check word series,

b) a first decoder for the reproduction of each time a first plurality of data words and a first check word series by means of a plurality of first syndromes generated therein by a parity detection matrix,

c) delay means for realigning the data words and the first check word series by means of mutually different delay times,

d) a second decoder for the reproduction of each time a first plurality of data words by means of a plurality of second syndromes generated therein by a parity detection matrix, and ,

e) output means for outputting each time a data word of a data word series in a number of output channels equal to said first plurality, wherein a data word series represents a data stream.

24. A decoder as claimed in Claim 23, wherein said input means comprise second delaying means for compensating relative

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delays incurred between even data channels and odd data channels.

25. A decoder as claimed in Claim 23, wherein the output means comprise third delaying means for compensating the relative delays incurred between even and odd data words of the data word series.

26. An apparatus comprising a decoder as claimed in Claim 23, wherein the apparatus further comprises means for accommodating a drivable audio disc, pick-up means for interrogating said audio disc, serial to parallel converting means having an input connected to said pick-up means for receiving therefrom a serial data stream and a plurality of outputs each connected to a respective channel of said input means, and parallel to serial reconverting means having a plurality of parallel inputs each connected to a respective data word channel of said output means, and furthermore digital to analog conversion means for converting a serial data stream to a continuous audio signal.

27. An apparatus comprising a decoder as claimed in Claim 23, wherein said apparatus further comprises means for accommodating a drivable storage disc, pick-up means for interrogating said storage disc, serial to parallel converting means having an input connected to said pick-up means for therefrom receiving a serial data stream and a plurality of outputs each connected to a respective channel of said input means, and parallel to serial reconverting means having a plurality of parallel inputs each connected to a respective data word channel of said output means.

28. A data carrier for use with a decoder as claimed in Claim 24, or with an apparatus as claimed in Claim 26 or 27, wherein the data carrier comprises a sequence of blocks, each block comprising a sequence of a third plurality, equal to one half said first plurality, of words derived from even data words of said data word series, a fourth plurality of words derived from said first check word series, and a further third plurality of words derived from odd data words of said data word series and a further fourth plurality of words derived from said second check word series.

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29. A data carrier as claimed in Claim 28, wherein each said block furthermore comprises a synchronization header.

30. A data processing method substantially as hereinbefore described with reference to Figures 1 to 5 of the accompanying drawings.

31. A method as claimed in Claim 30 modified substantially as hereinbefore described with reference to Figures 6 and 7, Figures 8 and 9, or Figures 10 and 11 of the accompanying drawings.

32. A device as claimed in Claim 8, substantially as hereinbefore described with reference to Figures 1, 6, 8 or 10 of the accompanying drawings.

33. A decoder as claimed in Claim 12, substantially as hereinbefore described with reference to Figure 3, 7, 9 or 11 of the accompanying drawings.

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