

## Abstract

## Device for testing a plurality of integrated circuits on a semiconductor wafer

The invention relates to a device for testing "high-power" integrated circuits (1001) on a semiconductor wafer (1000) during performance and failure testing, using testers (3004) that are not designed to perform the tests on this type of integrated circuit. It comprises probes (3002a) for establishing a temporary electrical connection with the connectors (2000) of the integrated circuits (1001) to be tested, a buffer circuit (4001a) for sharing a power supply resource (SC1) of a tester (3004) with the power supply inputs (VCC) of the integrated circuits (1001) to be tested, and a group (4002) of multiplexer circuits (4002a-d) each having, a first input connected to a shared high-voltage resource (HVC1) of the tester (3004), a second input connected to a distinct data input/output electronic resource (DC1-4) in communication with the tester (3004), and an output in communication with a test input/output (SPT) of an integrated circuit (1001a-d) to be tested.

Figure 3