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CO., LTD. [CN/CN]; 中国重庆市沙坪坝区西永大道25号C栋, Chongqing 401331 (CN)。

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(72) 发明人: 霍炎(**HUO, Yan**); 中国重庆市沙坪坝区西永大道25号C栋, Chongqing 401331 (CN)。涂旭峰(**TU, Xufeng**); 中国重庆市沙坪坝区西永大道25号C栋, Chongqing 401331 (CN)。

(74) 代理人: 北京博思佳知识产权代理有限公司 (**BEIJING BESTIPR INTELLECTUAL PROPERTY LAW CORPORATION**); 中国北京市海淀区上地三街9号嘉华大厦B座409, Beijing 100085 (CN)。

(71) 申请人: 矽磐微电子(重庆)有限公司 (**SIPLP MICROELECTRONICS (CHONGQING)**)

(81) 指定国(除另有指明, 要求每一种可提供的国家保护): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB,

(54) **Title:** SEMICONDUCTOR PACKAGING METHOD AND SEMICONDUCTOR PACKAGING STRUCTURE

(54) 发明名称: 半导体封装方法及半导体封装结构

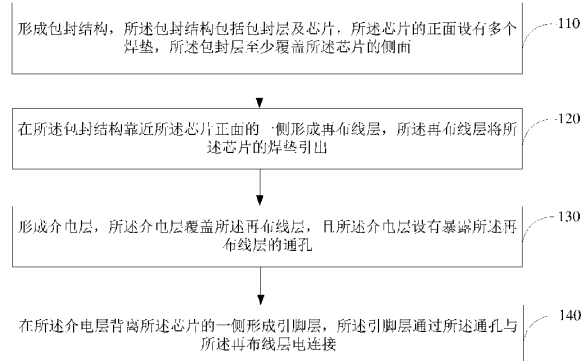


图 1

- 110 Form an encapsulating structure, which comprises an encapsulating layer and a chip, with a front surface of the chip being provided with multiple pads, and the encapsulating layer covering at least a side surface of the chip
- 120 Form, on the side of the encapsulating structure that is close to the front surface of the chip, a rewiring layer that leads out the pads of the chip
- 130 Form a dielectric layer which covers the rewiring layer and in which through holes are provided for exposing the rewiring layer
- 140 Form, on the side of the dielectric layer that faces away from the chip, a pin layer that is electrically connected to the rewiring layer via the through hole

(57) **Abstract:** Provided are a semiconductor packaging method and a semiconductor packaging structure. The semiconductor packaging method comprises: forming an encapsulating structure, which comprises an encapsulating layer and a chip, with a front surface of the chip being provided with multiple pads, and the encapsulating layer covering at least a side surface of the chip; forming, on the side of the encapsulating structure that is close to the front surface of the chip, a rewiring layer that leads out the pads of the chip; forming a dielectric layer which covers the rewiring layer and in which through holes are provided for exposing the rewiring layer;

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GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW。

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and forming, on the side of the dielectric layer that faces away from the chip, a pin layer that is electrically connected to the rewiring layer via the through hole.

(57) 摘要: 本申请提供一种半导体封装方法及半导体封装结构。所述半导体封装方法包括: 形成包封结构, 所述包封结构包括包封层及芯片, 所述芯片的正面设有多个焊垫, 所述包封层至少覆盖所述芯片的侧面; 在所述包封结构靠近所述芯片正面的一侧形成再布线层, 所述再布线层将所述芯片的焊垫引出; 形成介电层, 所述介电层覆盖所述再布线层, 且所述介电层上设有暴露所述再布线层的通孔; 在所述介电层背离所述芯片的一侧形成引脚层, 所述引脚层通过所述通孔与所述再布线层电连接。