

Description

BACKGROUND OF THE INVENTION

This invention relates to the field of electrical capacitors and more particularly to electrically variable piezoelectric capacitors manufacturable on thick or thin film hybrid microelectronic circuit substrates.

Hybrid microelectronic circuits are typically manufactured using either a thick film or a thin film process. In the thick film process, conductors, resistors, dielectrics, and insulators are silk screened onto a thin ceramic substrate, dried, and fired. Solder paste is then screened on at appropriate locations and discrete parts are attached to the substrate by heating the substrate and reflowing the solder. In the thin film process conductors are formed by applying a conductive material to the substrate surface and then etching the surface at predetermined locations using a photolithographic process. When a particular circuit, such as a voltage controlled oscillator, requires an electrically variable capacitor, a varactor diode is normally used because of its small size and ease of attachment to a hybrid microelectronic circuit substrate.

Varactor diodes have disadvantages, however, the most significant is their nonlinear voltage-capacitance response. It is a well known principle that nonlinear devices generate harmonic frequencies. In radio circuits, where the spectral purity of the transmitted signal is extremely important, any nonlinear device can generate unwanted harmonics which can be unintentionally amplified and transmitted. Thus, when varactor diodes are used in radio circuits, extreme care must be taken to insure that any harmonic frequencies that they generate are not radiated.

Another disadvantage of varactor diodes and other nonlinear capacitors is that they are two terminal devices. Therefore, the capacitance control voltage and the signal voltage cannot be separate and isolated voltages, but must be applied across the same two terminals. Therefore, the signal voltage must be combined with the control voltage.

Electrically variable capacitors have also been manufactured from piezoelectric elements. A typical prior art piezoelectric variable capacitor, such as that disclosed in US-A 3,949,246 includes two bimorph piezoelectric elements. Each element includes two piezoelectric layers of different polarizations bonded together with a conductive control plate in between the layers. One surface of each element has a conductive control plate while the other surface has a centrally located capacitor plate with a lead extending to the edge of the element. Each capacitor plate is surrounded by a narrow

insulating area which in turn is surrounded by another control plate. The two elements are then bonded together at their capacitor plate surfaces. A control voltage, appropriately applied to the various control plates, causes the elements to flex at their centers thereby moving the two capacitor plates further apart and varying the capacitance accordingly.

Although electrically variable piezoelectric capacitors are more linear than varactor diodes, the prior art piezoelectric capacitor is not well suited for either attachment to a hybrid microelectronic circuit substrate or for manufacturing using existing hybrid microelectronic circuit manufacturing technology.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an improved electrically variable piezoelectric capacitor.

A more specific object of the present invention is to provide an electrically variable piezoelectric capacitor that can be manufactured on hybrid microelectronic circuit substrates using existing hybrid microelectronic circuit manufacturing technology.

Briefly, in one embodiment of the invention, a method of constructing an electrically variable piezoelectric hybrid microelectronic circuit capacitor, comprising the steps of:

forming a first capacitor plate on a surface of a substrate;

forming a ridge on said surface of said substrate substantially about said first capacitor plate with the upper surface of said ridge above said first capacitor plate;

forming a second capacitor plate on a first surface of a piezoelectric wafer;

forming a first control plate on a second surface of said piezoelectric wafer; and

attaching said piezoelectric wafer to said ridge whereby said second capacitor plate is located substantially opposite said first capacitor plate.

In another embodiment an electronically variable piezoelectric hybrid microelectronic circuit capacitor, comprising in combination:

a substrate;

a first capacitor plate formed on a surface of said substrate;

a ridge on said surface of said substrate substantially about said first capacitor plate, said ridge having an upper surface extending above said first capacitor plate;

a piezoelectric wafer connected to said upper surface of said ridge;

a second capacitor plate formed on a first surface of said piezoelectric wafer; and

a first control plate formed on a second surface of said piezoelectric wafer.

In still another embodiment, an electrically variable piezoelectric hybrid microelectronic circuit capacitor includes a ceramic substrate with a first capacitor plate and a substantially circular supporting ridge formed on one surface of the ceramic substrate. The ridge, which is formed by a hybrid microelectronic circuit manufacturing process, has an upper surface positioned a predetermined distance above the first capacitor plate. A substantially dome shaped piezoelectric wafer, which has a convex surface adjacent the first capacitor plate and an opposing concave surface, is connected at its perimeter to the upper surface of the ridge. A second capacitor plate and a control plate are respectively formed on the convex and concave surfaces of the piezoelectric wafer. The capacitance between the first and second capacitor plates depends on the control voltage applied between the control plate and the second capacitor plate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a top view of the preferred three terminal monomorphic embodiment of the present invention wherein the capacitance control voltage V_c and the output capacitance C_o are illustrated schematically.

FIG. 2 is a sectional view of the preferred three terminal monomorphic embodiment as seen along line 2-2 of FIG. 1.

FIG. 3 is a bottom view of the preferred piezoelectric element as used in the four terminal embodiment: of FIGS. 4-5 and 8-9.

FIG. 4 is a top view of the preferred four terminal monomorphic embodiment of the present invention wherein the capacitance control voltage V_c and the output capacitance C_o are illustrated schematically.

FIG. 5 is a sectional view of the preferred four terminal monomorphic embodiment as seen along line 5-5 of FIG. 4.

FIG. 6 is a top view of the preferred three terminal bimorphic embodiment of the present invention wherein the capacitance control voltage V_c and the output capacitance C_o are illustrated schematically.

FIG. 7 is sectional view of the preferred three terminal bimorphic embodiment as seen along line 7-7 of FIG. 6.

FIG. 8 is a top view of the preferred four terminal bimorphic embodiment of the present invention wherein the capacitance control voltage V_c and the output capacitance C_o are illustrated schematically.

FIG. 9 is a sectional view of the preferred four terminal bimorphic embodiment as seen along line

9-9 of FIG. 8.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 1 and 2 illustrate the preferred three terminal monomorphic embodiment of the present invention. A hybrid microelectronic circuit substrate 10 is preferably made from a ceramic material, such as alumina, although any well known material compatible with hybrid microelectronic circuit manufacturing processes is suitable. A first capacitor plate 12, having an attached terminal 14, is formed on one surface of substrate 10 by a well known hybrid microelectronic circuit manufacturing process for forming conductive layers. Such well known processes include silk screening for thick film circuits and sputtering, vacuum deposition, or electroplating for thin film circuits. The preferred thickness for first capacitor plate 12 and terminal 14 is 25 to 50 μm (microns).

A ridge 16, having an attached terminal 18, is also formed on the surface of substrate 10 by a well known hybrid microelectronic circuit manufacturing process. In addition to the aforementioned processes for forming conductive layers, ridge 16 can also be formed by tooling substrate 10. For example, ridge 16 can be formed by a tool die when the alumina substrate 10 is "green". After firing, ridge 16 and terminal 18 would then be permanently formed on the surface of substrate 10. Ridge 16 and terminal 18 can also be comprised of a preformed glass ring epoxy bonded to the surface of substrate 10. If ridge 16 is tooled or preformed glass, a conductive surface can then be applied to its upper surface by one of the aforementioned processes for forming conductive layers. This conductive surface on ridge 16 and terminal 18 is preferably applied simultaneously with first capacitor plate 12. Regardless of the process used to form ridge 16, its upper surface is always a predetermined distance above the upper surface of capacitor plate 12 and terminal 14. This distance provides for separation between the two capacitor plates and is preferably less than 25 microns, although wider capacitor plate separations are acceptable.

A well known monomorphic piezoelectric wafer 20 has a second capacitor plate 22 formed on its lower surface and a control plate 24 formed on its upper surface. Capacitor plate 22 and control plate 24 are preferably electroplated on piezoelectric wafer 20, although any hybrid microelectronic circuit process for forming conductive layers is suitable. Piezoelectric wafer 20 is bonded to ridge 16 at capacitor plate 22, preferably by soldering, however other well known methods of providing a conductive bond, such as conductive epoxy, are suit-

able. Prior to bonding, a force 26 is applied substantially in the center of piezoelectric wafer 20 causing the wafer to arch downward slightly. Although the amount of the force will depend on the particular piezoelectric wafer used, it should be sufficient to produce about a 13 μm (micron) deflection at the center of wafer 20. After bonding wafer 20 to ridge 16, force 26 is removed and wafer 20 will maintain a slight arched or domed shape, curving in the direction of first capacitor plate 12. Fixing a slight but permanent arch into wafer 20 is necessary to predispose wafer 20 to flex downwards towards first capacitor plate 12 when a control voltage is applied between control plate 24 and second capacitor plate 22. Without this predisposition to move downward, monomorphous piezoelectric wafer 20 would have an equal probability of flexing away from first capacitor plate 22 when the control voltage V_c is applied.

Capacitance control terminal 28 is formed on the surface of substrate 10, preferably at the same time, to the same thickness, and by the same process that first capacitor plate 12 and terminal 18 are formed. Flywire 30 interconnects control plate 24 with control terminal 28. Flywire 30 is preferably connected to control plate 24 and terminal 28 by soldering, although other well known methods such as compression bonding or conductive epoxy are suitable.

In operation, a control voltage V_c is applied between terminals 28 and 18 and the variable capacitance C_v appears across terminals 14 and 18. Although terminal 18 is shown symbolically at ground potential it can conceivably be any voltage. When the control voltage is increased, the piezoelectric wafer 20 attempts to expand, however, its expansion is confined by ridge 16, therefore, the wafer bulges in its predisposed direction towards first capacitor plate 12. As piezoelectric wafer 20 arches towards first capacitor plate 12, the distance between capacitor plates 12 and 22 decreases, thereby increasing the capacitance across terminals 14 and 18.

The three terminal monomorphous piezoelectric capacitor of Figs. 1 and 2 can be converted into a four terminal capacitor by constructing the bottom surface of piezoelectric wafer 20 as illustrated in Fig. 3. A second capacitor plate 38 is smaller than capacitor plate 22 of Figure 1, it is also centrally located and has a lead 40 extending to the edge of wafer 20. Capacitor plate 38 and lead 40 are surrounded by an insulating area 42 which in turn is surrounded by a second control plate 44.

Fig. 4 and 5 illustrate the preferred four terminal monomorphous embodiment of the present invention. This embodiment uses the piezoelectric wafer as illustrated in Figure 3. As before, a first capacitor plate 52, having an attached terminal 54,

is formed on the surface of substrate 10 by a well known hybrid microelectronic circuit manufacturing process. First capacitor plate 52 is smaller than capacitor plate 12 of Figs. 1 and 2 because of the reduced surface area of the opposing capacitor plate 38 on the lower surface of wafer 20. Ridge 16 with attached terminal 18 and terminal 28 are formed on the surface of substrate 10 as previously described. Also, control plate 24 is connected to terminal 28 through flywire 30 as previously described.

To connect second capacitor plate 38 to the substrate, a terminal 56 is formed on the surface of substrate 10, preferably simultaneous with and using the same process as that used to form ridge 16. Terminal 56 is formed to the same thickness as ridge 16. To attach wafer 20 to substrate 10, control plate 44 is bonded to ridge 16 and lead 40 is bonded to terminal 56 preferably by soldering, although other conductive bonding techniques well known in the art such as conductive epoxy are suitable. As before, force 26 is applied substantially at the center of wafer 20 before bonding the wafer to ridge 16 and terminal 56. Upper control plate 24 is connected to terminal 28 through flywire 30 as previously described and the control voltage V_c is applied across terminals 28 and 18. In the four terminal embodiment, however, the capacitance is taken across terminals 54 and 56. It will be noted that in this embodiment that there is no common electrical connection between capacitance terminals 54 and 56 and control terminals 28 and 18.

Figs. 6 and 7 illustrate the preferred three terminal bimorphous embodiment of the present invention. As previously described, a first capacitor plate 12 with an attached terminal 14, and a ridge 16 with an attached terminal 18 are formed on the surface of substrate 10. In this embodiment, a well known bimorphous piezoelectric wafer 60 has a control plate 66 formed on the upper surface of a first piezoelectric layer 64. A second piezoelectric layer 62 is then bonded to the first layer over control plate 66. Control plate 66 has a tab 68 extending outside the perimeter of wafer 60. A control plate 24 is formed on the upper surface of piezoelectric wafer 60 and a second capacitor plate 22 is formed on its lower surface as previously described for wafer 20. Capacitor plate 22 is bonded to ridge 16, also as previously described. A terminal 70 is also formed on the surface of substrate 10 preferably simultaneous with capacitor plate 12 and a flywire 72 is connected between tab 68 and terminal 70, preferably by soldering. As previously described, flywire 80 is attached to control plate 24, however, in this embodiment the other end of the flywire is attached to terminal 18.

In operation, by applying the appropriate polar-

ity of control voltage V_c between terminals 70 and 18 piezoelectric wafer 60 can be made to flex towards first capacitor plate 12, thereby increasing the capacitance between terminals 14 and 18. By reversing the polarity of control V_c voltage applied between terminals 70 and 18, piezoelectric wafer 60 can be made to flex away from first capacitor plate 12, thereby decreasing the capacitance between terminals 14 and 18.

Figs. 8 and 9 illustrate the preferred four terminal bimorphic embodiment of the present invention. First capacitor plate 52 with attached terminal 54, ridge 16 with attached terminal 18, and terminals 56 and 70 are formed on the surface of substrate 10 as previously described. In this embodiment, bimorph piezoelectric element 60 has a first capacitor plate 38 with an attached lead 40, insulating area 42, and control plate 44 formed on its lower surface as depicted in Fig. 3. As previously described, control plate 44 is attached to ridge 16 and terminal 40 is attached to terminal 56. Flywire 72 is connected between tab 68 and terminal 70 while flywire 30 is connected between upper control plate 24 and terminal 18. In this embodiment, the variable capacitance C_v appears across terminals 54 and 56 while the control voltage is applied across terminal 70 and 18. As before, with the appropriate polarity of control voltage V_c , piezoelectric element 60 flexes towards substrate 10, decreasing the distance between capacitor plates 38 and 52 and thereby increasing the capacitance. If the opposite polarity is applied between terminals 70 and 18, piezoelectric element 60 flexes away from substrate 10, increasing the distance between capacitor plates 38 and 52, and thereby decreasing the capacitance.

In all embodiments of the invention, it is preferred that lower capacitor plate 12 or 52 be coated with a dielectric material. This dielectric material is preferably a low temperature glass for thick film processes, or about 1 μm (micron) of sputtered or evaporated SiO_2 for thin film processes. A sprayed on polyimide film is also suitable as are most dielectric materials well known in the hybrid microelectronic circuit processing art. In the alternative, either the upper capacitor plate 22 or 38, or both upper and lower plates can be coated with the dielectric material. If a thick dielectric material is used, the distance between the upper surface of ridge 16 and the upper surface of the lower capacitor plate 12 or 52 should be adjusted accordingly. To improve the Q of the capacitor, it is preferred that both the lower capacitor plate 12 or 52 and the upper capacitor plate 22 or 38 be formed from a highly conductive material, such as copper, silver, or gold.

In all embodiments, the diameter of the plates and the spacing between the plates depend upon

the desired capacitance and these dimensions are chosen according to well known formulas. In a typical design according to Figs. 1 and 2, with a wafer 20 and upper capacitor plate 22 diameter of 23 millimeters, a lower capacitor plate 12 diameter of 13 millimeters, a ridge 16 inside diameter of 18 millimeters, and a capacitor plate separation of 75 μm (microns), a piezoelectric capacitor manufactured with thin film hybrid microelectronic circuit technology has a capacitance range of 14 to 28 pico-Farads.

Claims

1. A method of constructing an electrically variable piezoelectric hybrid microelectronic circuit capacitor, comprising the steps of:
 - forming a first capacitor plate (12; 52) on a surface of a substrate (10);
 - forming a ridge (16) on said surface of said substrate substantially about said first capacitor plate with the upper surface of said ridge above said first capacitor plate;
 - forming a second capacitor plate (22; 38) on a first surface of a piezoelectric wafer (20; 60);
 - forming a first control plate (24) on a second surface of said piezoelectric wafer; and
 - attaching said piezoelectric wafer (20; 60) to said ridge (16) whereby said second capacitor plate (22 or 38) is located substantially opposite said first capacitor plate (12; 52).
2. The method of claim 1, wherein said step of attaching said piezoelectric wafer (20; 60) to said ridge (16) includes the steps of:
 - placing said piezoelectric wafer (20) on said ridge (16);
 - applying a force substantially at the center of said piezoelectric wafer (20), thereby causing said piezoelectric wafer (20; 60) to arch; and
 - bonding said piezoelectric wafer (20; 60) to said ridge (16) whereby said piezoelectric wafer maintains an arched shape when said force is removed.
3. The method of claim 2, further comprising the step of applying a dielectric material over the surface of one of said capacitor plates.
4. The method of claim 2, further comprising the step of forming a second control plate (44) on said first surface of said piezoelectric wafer (20; 60).
5. The method of claim 1, wherein said piezoelectric wafer is formed by the steps of:

ity of control voltage V_c between terminals 70 and 18 piezoelectric wafer 60 can be made to flex towards first capacitor plate 12, thereby increasing the capacitance between terminals 14 and 18. By reversing the polarity of control V_c voltage applied between terminals 70 and 18, piezoelectric wafer 60 can be made to flex away from first capacitor plate 12, thereby decreasing the capacitance between terminals 14 and 18.

Figs. 8 and 9 illustrate the preferred four terminal bimorphic embodiment of the present invention. First capacitor plate 52 with attached terminal 54, ridge 16 with attached terminal 18, and terminals 56 and 70 are formed on the surface of substrate 10 as previously described. In this embodiment, bimorph piezoelectric element 60 has a first capacitor plate 38 with an attached lead 40, insulating area 42, and control plate 44 formed on its lower surface as depicted in Fig. 3. As previously described, control plate 44 is attached to ridge 16 and terminal 40 is attached to terminal 56. Flywire 72 is connected between tab 68 and terminal 70 while flywire 30 is connected between upper control plate 24 and terminal 18. In this embodiment, the variable capacitance C_v appears across terminals 54 and 56 while the control voltage is applied across terminal 70 and 18. As before, with the appropriate polarity of control voltage V_c , piezoelectric element 60 flexes towards substrate 10, decreasing the distance between capacitor plates 38 and 52 and thereby increasing the capacitance. If the opposite polarity is applied between terminals 70 and 18, piezoelectric element 60 flexes away from substrate 10, increasing the distance between capacitor plates 38 and 52, and thereby decreasing the capacitance.

In all embodiments of the invention, it is preferred that lower capacitor plate 12 or 52 be coated with a dielectric material. This dielectric material is preferably a low temperature glass for thick film processes, or about 1 μm (micron) of sputtered or evaporated SiO_2 for thin film processes. A sprayed on polyimide film is also suitable as are most dielectric materials well known in the hybrid microelectronic circuit processing art. In the alternative, either the upper capacitor plate 22 or 38, or both upper and lower plates can be coated with the dielectric material. If a thick dielectric material is used, the distance between the upper surface of ridge 16 and the upper surface of the lower capacitor plate 12 or 52 should be adjusted accordingly. To improve the Q of the capacitor, it is preferred that both the lower capacitor plate 12 or 52 and the upper capacitor plate 22 or 38 be formed from a highly conductive material, such as copper, silver, or gold.

In all embodiments, the diameter of the plates and the spacing between the plates depend upon

the desired capacitance and these dimensions are chosen according to well known formulas. In a typical design according to Figs. 1 and 2, with a wafer 20 and upper capacitor plate 22 diameter of 23 millimeters, a lower capacitor plate 12 diameter of 13 millimeters, a ridge 16 inside diameter of 18 millimeters, and a capacitor plate separation of 75 μm (microns), a piezoelectric capacitor manufactured with thin film hybrid microelectronic circuit technology has a capacitance range of 14 to 28 pico-Farads.

Claims

1. A method of constructing an electrically variable piezoelectric hybrid microelectronic circuit capacitor, comprising the steps of:
 - forming a first capacitor plate (12; 52) on a surface of a substrate (10);
 - forming a ridge (16) on said surface of said substrate substantially about said first capacitor plate with the upper surface of said ridge above said first capacitor plate;
 - forming a second capacitor plate (22; 38) on a first surface of a piezoelectric wafer (20; 60);
 - forming a first control plate (24) on a second surface of said piezoelectric wafer; and
 - attaching said piezoelectric wafer (20; 60) to said ridge (16) whereby said second capacitor plate (22 or 38) is located substantially opposite said first capacitor plate (12; 52).
2. The method of claim 1, wherein said step of attaching said piezoelectric wafer (20; 60) to said ridge (16) includes the steps of:
 - placing said piezoelectric wafer (20) on said ridge (16);
 - applying a force substantially at the center of said piezoelectric wafer (20), thereby causing said piezoelectric wafer (20; 60) to arch; and
 - bonding said piezoelectric wafer (20; 60) to said ridge (16) whereby said piezoelectric wafer maintains an arched shape when said force is removed.
3. The method of claim 2, further comprising the step of applying a dielectric material over the surface of one of said capacitor plates.
4. The method of claim 2, further comprising the step of forming a second control plate (44) on said first surface of said piezoelectric wafer (20; 60).
5. The method of claim 1, wherein said piezoelectric wafer is formed by the steps of:



- forming a second control plate (66) on a surface of a first piezoelectric layer (64); and bonding a second piezoelectric layer (62) to said surface of said first piezoelectric layer (64), whereby said piezoelectric wafer is bimorphous.
6. The method of claim 5, further comprising the step of forming a third control plate (44) on said first surface of said piezoelectric wafer (60).
7. An electronically variable piezoelectric hybrid microelectronic circuit capacitor, comprising in combination:
- a substrate (12);
 - a first capacitor plate (12; 52) formed on a surface of said substrate (10);
 - a ridge (16) on said surface of said substrate (10) substantially about said first capacitor plate (12), said ridge (16) having an upper surface extending above said first capacitor plate;
 - a piezoelectric wafer (20; 60) connected to said upper surface of said ridge (16);
 - a second capacitor plate (22; 38) formed on a first surface of said piezoelectric wafer (20; 60); and
 - a first control plate (24) formed on a second surface of said piezoelectric wafer (20).
8. The piezoelectric hybrid microelectronic circuit capacitor of claim 7 wherein said piezoelectric wafer (20; 60) is dome shaped.
9. The piezoelectric hybrid microelectronic circuit capacitor of claim 7, further comprising a dielectric material covering the surface of one of said capacitor plates (12; 52, 22; 38).
10. The piezoelectric hybrid microelectronic circuit capacitor of claim 8, further comprising a second control plate (44) connected to said first surface of said piezoelectric wafer.
11. The piezoelectric hybrid microelectronic circuit capacitor of claim 7, wherein said piezoelectric wafer (60) includes two piezoelectric layers (62, 64) and a second control plate (66) between said layers.
12. The piezoelectric hybrid microelectronic circuit capacitor of claim 11, further comprising a third control plate (44) connected to said first surface of said piezoelectric wafer.

Patentansprüche

1. Ein Verfahren zum Herstellen eines elektrisch veränderbaren piezoelektrischen Kondensators für hybride Mikroelektronikschaltkreise, das die Schritte umfaßt:

Bilden einer ersten Kondensatorplatte (12; 52) auf einer Oberfläche eines Substrates (10);

Bilden eines Steges (16) auf der benannten Oberfläche des benannten Substrates im wesentlichen um die benannte erste Kondensatorplatte herum, wobei die obere Oberfläche des benannten Steges oberhalb der benannten ersten Kondensatorplatte ist;

Bilden einer zweiten Kondensatorplatte (22; 38) auf einer ersten Oberfläche eines piezoelektrischen Wafers (20; 60; 24);

Bilden einer ersten Steuerungsplatte (24) auf einer zweiten Oberfläche des benannten piezoelektrischen Wafers; und

Anbringen des benannten piezoelektrischen Wafers (20; 60) an dem benannten Steg (16), wobei die benannte zweite Kondensatorplatte (22 oder 38) im wesentlichen gegenüber der benannten ersten Kondensatorplatte (12; 52) angeordnet wird.

2. Das Verfahren des Anspruchs 1, bei dem der benannte Schritt des Anbringens des benannten piezoelektrischen Wafers (20; 60) an dem benannten Steg (16) die Schritte einschließt:

Anordnen des benannten piezoelektrischen Wafers (20) an dem benannten Steg (16);

Aufbringen einer Kraft im wesentlichen bei der Mitte des benannten piezoelektrischen Wafers (20), wodurch bewirkt wird, daß sich der benannte piezoelektrische Wafer (20; 60) wölbt; und

Bonden des benannten piezoelektrischen Wafers (20; 60) an den benannten Steg (16), wodurch der benannte piezoelektrische Wafer eine gewölbte Form aufrechterhält, wenn die benannte Kraft entfernt wird.

3. Das Verfahren des Anspruchs 2, das ferner den Schritt des Aufbringens eines dielektrischen Materials über die Oberfläche einer der benannten Kondensatorplatten umfaßt.

4. Das Verfahren des Anspruchs 2, das ferner den Schritt des Bildens einer zweiten Steuerungsplatte (44) auf der benannten ersten



Oberfläche des benannten piezoelektrischen Wafers (20; 60) umfaßt.

5. Das Verfahren des Anspruches 1, bei dem der benannte piezoelektrische Wafer durch die Schritte gebildet wird:

Bilden einer zweiten Steuerungsplatte (66) auf einer Oberfläche einer ersten piezoelektrischen Schicht (64); und

Bonden einer zweiten piezoelektrischen Schicht (62) an der benannten Oberfläche der benannten ersten piezoelektrischen Schicht (64), wodurch der benannte piezoelektrische Wafer zweielementig wird.

6. Das Verfahren des Anspruches 5, das ferner den Schritt des Bildens einer dritten Steuerungsplatte (44) auf der benannten ersten Oberfläche des benannten piezoelektrischen Wafers (60) umfaßt.

7. Elektronisch veränderbar, piezoelektrischer Kondensator für hybride Mikroelektronikschaltkreise, umfassend in Kombination:

ein Substrat (12);

eine erste Kondensatorplatte (12; 52), die auf einer Oberfläche des benannten Substrats (10) geformt ist;

einen Steg (16) auf der benannten Oberfläche des benannten Substrats (10) im wesentlichen um die benannte erste Kondensatorplatte (12) herum, wobei der benannte Steg (16) eine sich oberhalb der benannten ersten Kondensatorplatte erstreckende Oberfläche aufweist;

ein mit der benannten oberen Oberfläche des benannten Steges verbundener piezoelektrischer Wafer (20; 60);

eine zweite Kondensatorplatte (22; 38), die auf einer ersten Oberfläche des benannten piezoelektrischen Wafers (20; 60) geformt ist; und

eine erste Steuerungsplatte (24), die auf einer zweiten Oberfläche des benannten piezoelektrischen Wafers (20) geformt ist.

8. Der piezoelektrische Kondensator für hybride Mikroelektronikschaltkreise des Anspruch 7, wobei der benannte piezoelektrische Wafer (20; 60) kalottenförmig ist.

9. Der piezoelektrische Kondensator für hybride Mikroelektronische Schaltkreise des Anspru-

ches 7, ferner umfassend ein dielektrisches Material, das die Oberfläche von einer der benannten Kondensatorplatten (12; 52; 22; 38) überdeckt.

10. Der piezoelektrische Kondensator für hybride Mikroelektronikschaltkreise des Anspruches 8, ferner umfassend eine zweite Steuerungsplatte (44), die mit der benannten ersten Oberfläche des benannten piezoelektrischen Wafers verbunden ist.

11. Der piezoelektrische Kondensator für hybride Mikroelektronikschaltkreise des Anspruches 7, wobei der benannte piezoelektrische Wafer (60) zwei piezoelektrische Schichten (62, 64) und eine zweite Steuerungsplatte (66) zwischen den benannten Schichten einschließt.

12. Der piezoelektrische Kondensator für hybride Mikroelektronikschaltkreise des Anspruches 11, ferner umfassend eine dritte Steuerungsplatte (44), die mit der benannten ersten Oberfläche des benannten piezoelektrischen Wafers verbunden ist.

Revendications

1. Procédé de réalisation d'un condensateur piézo-électrique variable électriquement dans un circuit micro-électronique hybride, consistant essentiellement :

à former une première plaque de condensateur (12, 52) sur une surface d'un substrat (10),

à former un rebord (16) sur ladite surface dudit substrat, pratiquement autour de la première plaque de condensateur, avec la surface supérieure dudit rebord au-dessus de ladite première plaque de condensateur,

à former une seconde plaque de condensateur (22, 38) sur une première surface d'une plaquette piézo-électrique (20, 60),

à former une première plaque de commande (24) sur une seconde surface de ladite plaquette piézo-électrique, et

à fixer ladite plaquette piézo-électrique (20, 60) sur ledit rebord (16) de manière que ladite seconde plaque de condensateur (22, 38) soit située pratiquement à l'opposé de ladite première plaque de condensateur (12, 52).

2. Procédé selon la revendication 1, dans lequel ladite opération de fixation de ladite plaquette piézo-électrique (20, 60) sur ledit rebord (16) consiste :

à placer ladite plaquette piézo-électrique



- (20) sur ledit rebord (16),
à appliquer une force, pratiquement au centre de ladite plaquette piézo-électrique (20), provoquant ainsi une courbure de ladite plaquette piézo-électrique (20, 60), et
à fixer ladite plaquette piézo-électrique (20, 60) sur ledit rebord (16) de manière que ladite plaquette piézo-électrique maintienne une forme incurvée quand ladite force est supprimée.
3. Procédé selon la revendication 2, consistant en outre à appliquer une matière diélectrique sur la surface de l'une desdites plaques de condensateur.
4. Procédé selon la revendication 2, consistant en outre à former une seconde plaque de commande (44) sur ladite première surface de ladite plaquette piézo-électrique (20, 60).
5. Procédé selon la revendication 1, dans lequel ladite plaquette piézo-électrique est formée :
en formant une seconde plaque de commande (66) sur une surface d'une première couche piézo-électrique (64), et
en fixant une seconde couche piézo-électrique (62) sur ladite surface de ladite première couche piézo-électrique (64) de manière que ladite plaquette piézo-électrique soit bimorphe.
6. Procédé selon la revendication 5, consistant en outre à former une troisième plaque de commande (44) sur ladite première surface sur ladite plaquette piézo-électrique (60).
7. Condensateur piézo-électrique variable électriquement, dans un circuit micro-électronique hybride, comportant :
un substrat (12),
une première plaque de condensateur (12, 52) formée sur une surface dudit substrat (10),
un rebord (16) sur ladite surface dudit substrat (10) pratiquement autour de ladite première plaque de condensateur (12), ledit rebord (16) comportant une surface supérieure qui s'étend au-dessus de ladite première plaque de condensateur,
une plaquette piézo-électrique (20, 60), connectée à ladite surface supérieure dudit rebord (16),
une seconde plaque de condensateur (22, 38) formée sur une première surface de ladite plaquette piézo-électrique (20, 60), et
une première plaque de commande (24) formée sur une seconde surface de ladite plaquette piézo-électrique (20).

8. Condensateur piézo-électrique dans un circuit micro-électronique hybride selon la revendication 7, dans lequel ladite plaquette piézo-électrique (20, 60) a la forme d'un dôme.
9. Condensateur piézo-électrique dans un circuit micro-électronique hybride selon la revendication 7, comportant en outre une matière diélectrique qui couvre la surface de l'une desdites plaques de condensateur (12, 52, 22, 38).
10. Condensateur piézo-électrique dans un circuit micro-électronique hybride selon la revendication 8, comportant en outre une seconde plaque de commande (44) connectée à ladite première surface de ladite plaquette piézo-électrique.
11. Condensateur piézo-électrique dans un circuit micro-électronique hybride selon la revendication 7, dans lequel ladite plaquette piézo-électrique (60) comporte deux couches piézo-électriques (62, 64) et une seconde plaque de commande (66) entre lesdites couches.
12. Condensateur piézo-électrique dans un circuit micro-électronique hybride selon la revendication 11, comportant en outre une troisième plaque de commande (44) connectée à ladite première surface de ladite plaquette piézo-électrique.

