



(51) International Patent Classification:

H05K 3/06 (2006.01) *H01L 21/02* (2006.01)
H05K 1/02 (2006.01)

(21) International Application Number:

PCT/US2013/000185

(22) International Filing Date:

9 August 2013 (09.08.2013)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

61/743,596 7 September 2012 (07.09.2012) US

(71) Applicant (for all designated States except US): **R&D CIRCUITS, INC.** [US/US]; 3601 South Clinton Road, South Plainfield, NJ 07080-1322 (US).

(74) Agent: **KLAR, Richard, B.**; 145 Willis Ave., Suite 6, Mineola, NY 11501 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: METHOD AND STRUCTURE FOR FORMING CONTACT PADS ON A PRINTED CIRCUIT BOARD USING ZERO UNDER- CUT TECHNOLOGY

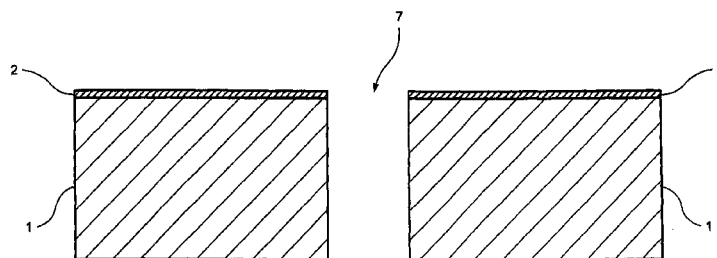


FIG. 1

(57) Abstract: A method and an apparatus for forming a contact pad on a printed circuit board over a filled plate via or blind in which an additional metallic or a non metallic coating is applied to a final surface finished plate which encapsulates the side walls of the wear resistant surface plate, and also covers the side walls of the metal layer plated onto the filled via and the wrap around plated metal which was plated in the via and onto the surface of the base metal to the extents of the pad geometry. This prevents subsequent undermining through the etching process and ensuring the integrity and reliability of the vias' electrical connection when an underlying base metal such as but not limited to copper and the surface plated metal are formed when plating metal in the via and consequently onto the surface.

