SEMICONDUCTOR PROCESSING APPARATUS

FIELD OF THE INVENTION

The present invention relates to a semiconductor wafer processing apparatus and more specifically relates to a semiconductor processing apparatus with a liner structure.

BACKGROUND OF THE INVENTION

The plasma etching technology has been widely applied to the etching process of semiconductor fabrication, such as gate etching, dielectric etching and metal etching etc. A typical semiconductor processing chamber comprises a chamber, a plasma generating and controlling device, a process gas delivery device, a chuck for securing a silicon wafer and process assemblies (for controlling and defining the area where gas flows and plasma exists, and preventing etching products adsorbing and depositing on the inner wall of the chamber, which is not easy to be disassembled for cleaning) etc.

Under low pressure, the reaction gas is excited by a radio frequency power and is ionized to generate plasma. The plasma is composed of electrons and charged ions. When the gas in the reaction chamber is impacted by the electrons, not only the gas is changed into ions, but also it can absorb energy and form a large number of active groups. There are chemical reactions occurred between the active reaction groups and the surface of the material to be etched and subsequently volatile reaction products are produced. The reaction products get away from the surface of the material to be etched and are pumped out of the chamber by a vacuum system.

The plasma generated after the process gas entering into the reaction chamber is activated is used to etch the material on the wafer surface. However, the non-uniform distribution of gas inside the reaction chamber will result in great variations in etch rate and uniformity on the wafer surface in the chamber. In particular, while the size of the present wafer increases from 100 mm to 300 mm, the volume of the reaction chamber has to be enlarged accordingly and therefore, it is more difficult to provide a more uniform distribution of gas in the chamber. Therefore, the reason for the great variations

in etch rate and uniformity from the center to the periphery of the wafer is the non-uniform distribution of gas. A large number of production and research data show that during a semiconductor fabrication, it is very difficult to realize the uniform distribution of the process gas on the surface of the semiconductor silicon wafer, while the uniform and stable distribution of the gas flow on the surface of the silicon wafer is a key factor to achieve a stable gas plasma.

Another problem of the plasma etching in the semiconductor fabrication is that if many wafers are processed in the chamber, a film builds up on the wall of the processing chamber over the period of time. This kind of film build-up can result in any one of the following two problems. First, the film may flake off the wall and the particles infiltrate into the processing chamber. Because the sizes of the components of the integrated circuit devices are becoming smaller and smaller, the degree to which the particles can be tolerated during an etching process decreases rapidly. Therefore, it is more critical to solve the problem of the particles occurring on the wall during the etching process. Second, the film may alter the RF grounding path and thereby affect the wafer quality. Because the occurrence of any one of the two situations above is not desirable, the wet cleaning treatment for the processing chamber has to be done, i.e. the wall of the processing chamber is physically scrubbed to remove the film build-up.

In the commercial semiconductors fabrication, the wet cleaning treatment for the processing chamber is not preferred because it is done in the mode of off production line and thereby the throughput is decreased. In the efforts to avoid the need for the wet cleaning, some processing chambers adopt a liner structure to protect the wall of the chamber. The use of the liner enables the replacement and cleaning to be done easily with the minimal downtime when the film build-up occurs on the wall, and thereby the continuous and effective production in the processing chamber can be ensured.

Fig. 1 shows a schematic diagram of a structure of the semiconductor processing chamber liner as disclosed in the Chinese Patent Application No. CN1152414C. The processing chamber liner includes a plasma confinement shield 116c with a plurality of apertures 128. An outer sidewall 116b extends upwardly from the plasma confinement shield 116c. An outer flange 116a extends outwards from the

outer sidewall 116b so that the outer flange extends beyond the chamber and into a region under atmospheric pressure. Besides, the processing chamber liner further includes an inner sidewall 116d extending upwardly from the plasma confinement shield.

Though the liner disclosed in the patent as mentioned above can effectively protect the inner wall of the processing chamber and reduce the film build-up, and thereby reduce the particle contamination, it has at least the following defects. That is, the scope protected with this liner structure is too small to protect an adjustment support below a quartz window and an exhaust chamber below the confinement shield effectively and avoid the production of particles to the largest extent. Thereby the wafer contamination is caused. In addition, the uniformity of a flow field in the reaction chamber provided by such structure, especially the uniformity of the flow field on the silicon wafer surface is limited to some extent, and thereby the further improvement of uniformity of the flow field on the silicon wafer surface is limited.

The US Patent 6,821,378 discloses a baffle with asymmetrical screens as shown in Fig. 2 to slow down the flow speed of the process gas in the side-pumped etching chamber and accordingly the uniformity of the process gas flow across the wafer surface can be improved. The baffle is designed for the side-pumped etching chamber and its screen adopts round holes, square holes, slot holes etc. When the slot holes are used, the porosity (the porosity is defined as the ratio between the area of holes and the area of the screen, not the whole area of the baffle) of the screen can reach 90% as a maximum. This patent indicates that the smaller the porosity, the smaller "pass through" percentage of the gas passing through the screen and being exhausted by the vacuum system becomes and the slower a gas flow becomes. Conversely, the uniformity of the gas flow across the surface of silicon wafer can be increased and accordingly the etching results can be improved. When the porosity of the screen is 57%~76%, the etching uniformity is improved greatly. When the porosity of the screen is 57%, the etching uniformity is improved most remarkably and can be increased by 50%.

Though the structure disclosed above can improve the etching uniformity, it can

not effectively solve the problem of the non-uniformity of etching rate, which is encountered by most of the present etching apparatuses.

SUMMARY OF THE INVENTION

The purpose of the present invention is to overcome the defects of the prior art and to provide a semiconductor processing apparatus with a liner, which can provide a wide scope of protection for the processing chamber and the structure of which is more favorable for the uniformity of flow field in the reaction chamber.

According to one aspect of the present invention, the invention provides a semiconductor processing apparatus. The semiconductor processing apparatus comprises an inner sidewall and an outer sidewall, both of which are in a cylindrical shape; a flange, which extends outwards from said outer sidewall; and a shield plate between said inner sidewall and said outer sidewall, wherein, said outer sidewall extends upwardly perpendicularly or along an angle from the upper surface of said flange for a first distance and extends downwards perpendicularly or along an angle from said shield plate for a second distance; said inner sidewall extends upwardly perpendicularly or along an angle from the shield plate for a third distance and extends downwards perpendicularly or along an angle from said shield plate for a fourth distance.

According to another aspect of the present invention, the shield plate has a stepped structure, and one or more rows of apertures distributed uniformly are provided on an upper stepped surface and a lower stepped surface of said shield plate.

Compared with the prior art, the inner sidewall and the outer sidewall of the semiconductor processing apparatus provided by the present invention have following improvements: the outer sidewall extends upwardly perpendicularly or along an angle from the upper surface of said flange for a first distance and extends downwards perpendicularly or along an angle from the shield plate for a second distance; the inner sidewall extends upwardly perpendicularly or along an angle from the shield plate for a third distance and extends downwards perpendicularly or along an angle from the shield plate for a fourth distance. Therefore, the semiconductor processing apparatus

of the present invention can not only enlarge the protection area for the processing chamber, but also slower the speed of the film building up and further reduce the particles.

The shield plate of the liner structure of the semiconductor processing apparatus of the present invention can adopt a variety of structures, such as a stepped structure, which can not only improve the uniformity of the flow field, but also improve the speed field of flow field in the chamber, especially on the surface of the wafer, to make it more uniform.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of a liner structure of the prior art;

Fig. 2 is a perspective view of a processing chamber with a shield plate of the prior art;

Fig. 3 is a schematically perspective view of a liner structure of a semiconductor processing apparatus of the present invention;

Fig. 4 is a side sectional view of the liner structure of the present invention; and

Fig. 5 is a local enlarged view of a region "A" in Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred exemplary embodiments of the present invention will be illustrated below in detail in connection with accompanying drawings so that the features and advantages as mentioned above and other features and advantages of the present invention will become clearer.

But, the preferred embodiments described herein should not be construed as limiting the present invention. On the contrary, the preferred embodiments of the invention are provided here to present the present invention more clearly and to make those skilled in the art understand the present invention more easily.

As shown in Figs. 3 to 5, a liner structure 116 of the semiconductor processing apparatus of the present invention has an annular structure, which constitutes an inner

circumference and an outer circumference, i.e. an outer sidewall 116b and an inner sidewall 116d are cylindrical, and the outer sidewall 116b is provided with a wafer load port and several small diagnostic ports. A shield plate 116c (116c1-116c3) of the liner is located in an annular cylindrical region, which is constituted by the outer sidewall 116b and the inner sidewall 116d.

Wherein, the shield plate 116c of the liner adopts a stepped structure. Its basic shape is similar to one step. The step specifically includes an upper stepped surface 116c1, a lower stepped surface 116c2 and a side stepped surface (connection surface) 116c3 for connecting the upper and the lower stepped surfaces. The three stepped surfaces 116c1-116c3 as mentioned above are all located within the annular cylindrical region, which is constituted by the outer sidewall 116b and the inner sidewall 116d of the liner. And, rows of apertures 170 distributed uniformly can be provided on all the three surfaces so that the "pass through" area of the reaction gas is increased, i.e. the porosity of the screen is increased, and accordingly the uniformity can be improved.

Certainly, the stepped structure of the shield plate 116c of the liner is not limited to the stepped structure with one step illustrated in the present embodiment, but can also be a structure with a plurality of steps. In this case, said upper stepped surface refers to an upper stepped surface of the uppermost step and said lower stepped surface refers to a lower stepped surface of the lowest step. In addition, a height of a side stepped surface ranges from 0 mm to 40 mm. The different heights of the side stepped surface will bring different influences on the uniformity of the flow field of the reaction gas across the silicon wafer surface, therefore, an appropriate height of the side stepped surface can be selected to obtain an optimal uniformity of flow field across the silicon wafer surface. Certainly, the connection between a side stepped surface and a corresponding upper and lower stepped surfaces is not only limited to a vertical connection.

The outer sidewall 116b extends upwardly perpendicularly or along an angle from the upper surface of the outer flange 116a for a first distance 116g and extends downwards perpendicularly or along an angle from the shield plate 116c (i.e. from the connection between the shield plate 116c of the liner and the outer sidewall 116b, in

other words, i.e. from the upper stepped surface 116c1) of the liner for a second distance 116f. The inner sidewall 116d extends upwardly perpendicularly or along an angle from the shield plate 116c (i.e. from the connection between the shield plate 116c of the liner and the inner sidewall 116d, in other words, i.e. from the lower stepped surface 116c2) of the liner for a third distance and extends downwards perpendicularly or along an angle from the shield plate 116c (i.e. from the connection between the shield plate 116c of the liner and the inner sidewall 116d, in other words, i.e. from the lower stepped surface 116c2) of the liner for a fourth distance 116e. Therefore, a wider protection range for an adjustment support and an exhaust chamber can be realized. Wherein, the first distance 116g, the second distance 116f, the third distance and the fourth distance 116e all rang from 0 mm to 60 mm. The "an angle" as mentioned above refers to an angle ranging from –20 degrees to +20 degrees.

It should be noted that the shape of the shield plate of the semiconductor processing apparatus in the present invention is not limited to the step structure illustrated in the present embodiment. The shield plate can also be a straight plate placed slantwise or a curved plate. Also, it can be a plate with a cross section in a concave, convex, regular polygon, square wave, hackle or other irregular shape. As long as the shield plate can improve the uniformity of the flow field, improve the speed field of flow field of the chamber, especially improve the speed field of flow field on the surface of the silicon wafer and the manufacturing process can be met, the shape of the shield plate can be any one.

The embodiments of the present invention are described in the accompanying drawings and the description. Though some specific terms are used, such description using these terms is only for general and illustrative purpose, and is not for limitation. The scope of the present invention will be described in the following claims.

Claims

What is claimed is:

1. A semiconductor processing apparatus, comprising an inner sidewall and an outer sidewall, both of which are in a cylindrical shape, a flange extending outwards from said outer sidewall and a shield plate between said inner sidewall and said outer sidewall, characterized in that:

said outer sidewall extends upwardly perpendicularly or along an angle from the upper surface of said flange for a first distance and extends downwards perpendicularly or along an angle from said shield plate for a second distance;

said inner sidewall extends upwardly perpendicularly or along an angle from the shield plate for a third distance and extends downwards perpendicularly or along an angle from said shield plate for a fourth distance.

2. The semiconductor processing apparatus of claim 1, wherein said shield plate has a stepped structure.

3. The semiconductor processing apparatus of claim 2, wherein rows of apertures distributed uniformly are provided on an upper stepped surface and a lower stepped surface of said shield plate with the stepped structure.

4. The semiconductor processing apparatus of claim 2, wherein apertures are also provided on a connection surface between the upper stepped surface and the lower stepped surface of said shield plate with the stepped structure.

5. A semiconductor processing apparatus, comprising an inner sidewall and an outer sidewall, both of which are in a cylindrical shape, a flange extending outwards from said outer sidewall and a shield plate between said inner sidewall and said outer sidewall, characterized in that:

said shield plate has a stepped structure, and rows of apertures distributed uniformly are provided on an upper stepped surface and a lower stepped surface of

said shield plate with the stepped structure.

6. The semiconductor processing apparatus of claim 5, wherein said outer sidewall extends upwardly perpendicularly or along an angle from the upper surface of said flange for a first distance and extends downwards perpendicularly or along an angle from the upper stepped surface of said shield plate for a second distance.

7. The semiconductor processing apparatus of claim 5, wherein said inner sidewall extends upwardly perpendicularly or along an angle from said shield plate for a third distance and extends downwards perpendicularly or along an angle from the lower stepped surface of said shield plate for a fourth distance.

8. The semiconductor processing apparatus of claim 6 or 7, wherein apertures are also provided on a connection surface between the upper stepped surface and the lower stepped surface of said shield plate with the stepped structure.