

WHAT IS CLAIMED IS:

[Claim 1]. A three-dimensional (3D) memory device, comprising:
a substrate;
a memory stack comprising a plurality of interleaved conductor layers and dielectric layers on the substrate; and
a memory string extending vertically through the memory stack and comprising:
a semiconductor plug in a lower portion of the memory string;
a protective dielectric layer on the semiconductor plug, wherein the protective dielectric layer is a native oxide layer of the semiconductor plug, wherein a thickness of the protective dielectric layer is between 1 nm and 5 nm; and
a memory film above the protective dielectric layer and along a sidewall of the memory string, wherein the memory film is in direct contact with the plurality of interleaved conductor layers and dielectric layers.

[Claim 2]. The 3D memory device of claim 1, wherein an insulation layer is formed between the substrate and the memory stack.

[Claim 3]. The 3D memory device of claim 1, wherein the semiconductor plug is an epitaxially-grown silicon plug.

[Claim 4]. The 3D memory device of claim 1, wherein the protective dielectric layer comprises silicon oxide.

[Claim 5]. The 3D memory device of claim 1, wherein the protective dielectric layer is not disposed along the sidewall of the memory string.

[Claim 6]. The 3D memory device of claim 1, wherein the protective dielectric layer abuts the sidewall of the memory string.

[Claim 7]. A method for forming a three-dimensional (3D) memory device, comprising:

forming a first dielectric deck comprising a first plurality of interleaved sacrificial layers and dielectric layers on a substrate;

forming a first opening extending vertically through the first dielectric deck;

forming a semiconductor plug in a lower portion of the first opening;

oxidizing a top portion of the semiconductor plug forming a protective dielectric layer comprising a native oxide layer on the semiconductor plug;

controlling the thickness of the resulting native oxide layer wherein the thickness of the protective dielectric layer is between 1 nm and 5 nm;

forming a sacrificial layer on the protective dielectric layer in the first opening;

forming a second dielectric deck comprising a second plurality of interleaved sacrificial layers and dielectric layers on the first dielectric deck;

forming a second opening extending vertically through the second dielectric deck to expose the sacrificial layer in the first opening;

removing the sacrificial layer in the first opening;

forming a memory film on the protective dielectric layer and along sidewall of the first and second openings directly after removing the sacrificial layer in the first opening;

forming a third opening through the memory film and the protective dielectric layer in the lower portion of the first opening;

forming a semiconductor channel over the memory film and in the third opening to contact the semiconductor plug;

forming a channel plug in an upper portion of the second opening; and

replacing the first and second pluralities of interleaved sacrificial layers with conductor layers after forming the channel plug to form a plurality of interleaved conductor layers and dielectric layers, such that the memory film is in direct contact with the plurality of interleaved conductor layers and dielectric layers.

[Claim 8]. The method of claim 7, comprising forming an insulation layer between the substrate and the first dielectric deck.

[Claim 9]. The method of claim 7, wherein the thickness of the native oxide layer is controlled by thermal oxidation.

[Claim 10]. The method of claim 7, wherein the thickness of the native oxide layer is controlled by wet chemical oxidation.

[Claim 11]. The method of claim 7, wherein forming the semiconductor plug comprises epitaxially growing a silicon plug from the substrate.

[Claim 12]. The method of claim 7, wherein forming the protective dielectric layer as a silicon oxide.

[Claim 13]. The method of claim 7, wherein the protective dielectric layer is not formed along the sidewall of the first opening.

[Claim 14]. The method of claim 7, wherein the protective dielectric layer is formed to completely cover the semiconductor plug.

[Claim 15]. The method of claim 7, wherein removing the sacrificial layer comprising etching the sacrificial layer until being stopped by the protective dielectric layer.

[Claim 16]. The method of claim 7, wherein
forming the memory film comprises subsequently depositing a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer on the sidewall of the first and second openings in this order; and
forming the semiconductor channel comprises depositing a polysilicon layer over the second silicon oxide layer and in the third opening.