

ABSTRACT OF THE DISCLOSURE

LOW-VOLTAGE DIGITAL ROM CIRCUIT AND METHOD

A circuit and method of implementing a digital read-only memory (ROM) utilizes a means for selectively driving (410) one of two complementary logic state
5 signal lines (BIT, nBIT) to a voltage reference upon a readout signal (READOUT) for an addressable bit becoming active. Each complementary logic state signal line (BIT, nBIT) represents one of two logic states. The logic state of the addressed bit is determined by which of the two complementary logic state signal lines (BIT, nBIT) is driven. The logic level of each complementary logic state signal line (BIT, nBIT) is
10 then inverted and driven (420) onto the other so that both signal lines will be driven to their proper logic state, thereby allowing either signal line to be used in ascertaining the logic state of the bit being addressed.

FIG. 5