

02/04/03

200 3018595

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
25 April 2002 (25.04.2002)

PCT

(10) International Publication Number
WO 02/033706 A3(51) International Patent Classification⁷: G11C 11/4094,
7/18, H01L 27/108, G11C 7/14, 11/4097, 11/4099, 7/12

(21) International Application Number: PCT/US01/31159

(22) International Filing Date: 3 October 2001 (03.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/690,513 17 October 2000 (17.10.2000) US(71) Applicant (for all designated States except US): INTEL
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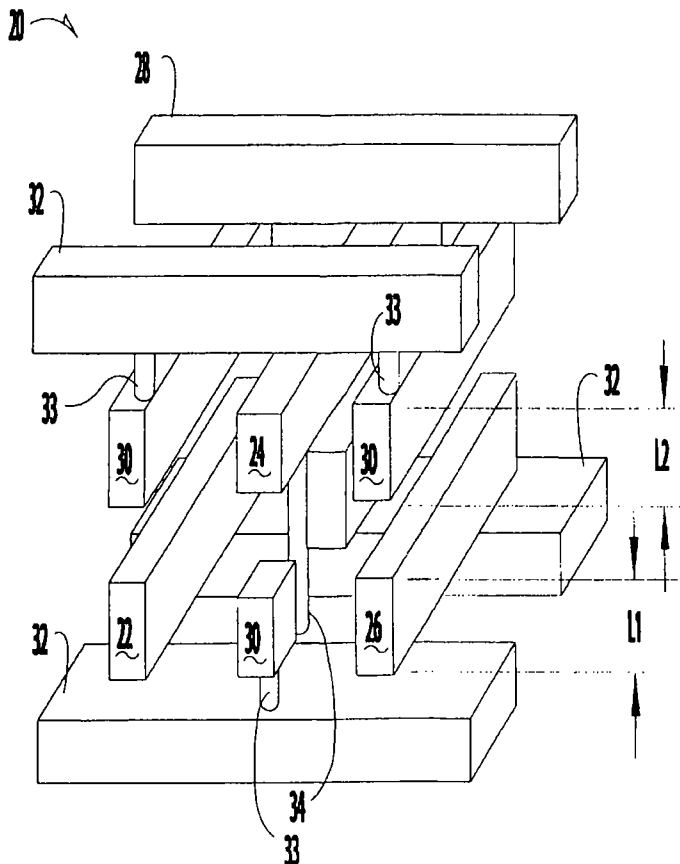
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lis, MN 55402 (US).(81) Designated States (national): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI,
SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU,
ZA, ZW.

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(54) Title: NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES



(57) Abstract: An open bit line dynamic random access memory (DRAM) architecture uses a multiple layer bit line configuration to reduce coupling between switching bit lines in the device. In one approach, each successive cell within a row of DRAM cells is coupled to a bit line segment that is on a different metallization layer than a previous cell in the row. Shielding members are also provided between adjacent bit lines on a common metallization layer to further reduce noise coupling. Functionality is also provided for reducing the effect of word line to bit line coupling in the DRAM device using dummy signal injection techniques. In this manner, common mode noise that could otherwise saturate one or more sense amplifiers within the DRAM device is reduced or eliminated before such saturation can take place. In one approach, dummy cells and reference cells are provided for use in performing the signal injection. The principles of the present invention are particularly well suited for use within embedded DRAM structures where low charge storage capacity within individual cells reduces the signal voltage levels that are achievable.

WO 02/033706 A3



162162



ACTION

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW). Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM). European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR). OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(88) Date of publication of the international search report:

17 April 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.