CLAIMS

What is claimed is:

1. A semiconductor structure comprising a plurality of tight pitch conductive lines each integrally formed with a conductive contact of a plurality of tight pitch conductive contacts.

2. The semiconductor structure of claim 1, wherein the plurality of tight pitch conductive contacts comprise a plurality of conductive vias.

3. The semiconductor structure of claim 2, wherein each conductive via of the plurality of conductive vias extends from one tight pitch conductive line of the plurality of tight pitch conductive lines to a tight pitch active area on a semiconductor substrate.

4. The semiconductor structure of claim 3, wherein each conductive via of the plurality of conductive vias extends through an aperture in a mask layer.

5. The semiconductor structure of claim 4, wherein each tight pitch contact of the plurality of tight pitch conductive contacts extends through a common aperture in the mask layer.

6. The semiconductor structure of claim 5, wherein the common aperture in the mask layer is elongated and extends in a lateral direction over the semiconductor substrate in a direction generally perpendicular to the plurality of tight pitch conductive lines.

7. The semiconductor structure of any one of claims 3 through 6, wherein the active area comprises at least a portion of a feature selected from the group consisting of a source, a drain, a gate, a conductive pad and a conductive trace.

8. The semiconductor structure of any one of claims 1 through 7, wherein the tight pitch conductive lines and the tight pitch conductive contacts each have a width of less than about 50 nm.

9. The semiconductor structure of claim 8, wherein the tight pitch conductive lines and the tight pitch conductive contacts each have a width of less than about 30 nm.

10. The semiconductor structure of any one of claims 1 through 9, wherein each integrally formed tight pitch conductive line and tight pitch conductive contact comprises a unitary mass of at least one of tungsten, copper, aluminum, and nickel.

11. A method of fabricating a semiconductor structure, the method comprising:
substantially concurrently forming a plurality of tight pitch conductive lines and a plurality of tight pitch conductive contacts; and
integrally forming each tight pitch conductive line of the plurality of tight pitch conductive lines with one tight pitch conductive contact of the plurality of tight pitch conductive contacts.

12. The method of claim 11, further comprising providing electrical contact between each tight pitch conductive contact and a corresponding tight pitch active area of a plurality of tight pitch active areas on a surface of a semiconductor substrate.

13. The method of claim 11 or claim 12, further comprising:
forming a first layer of dielectric material;
forming a mask layer over the first layer of dielectric material;
providing an aperture through the mask layer to the first layer of dielectric material;
forming a second layer of dielectric material over the mask layer and the aperture;
forming a plurality of tight pitch trenches in the second layer of dielectric material; and
forming a plurality of tight pitch contact holes in the first layer of dielectric material through the aperture in the mask layer.

14. The method of claim 13, further comprising sequentially forming the plurality of tight pitch trenches in the second layer of dielectric material and the plurality of tight pitch trenches in the first layer of dielectric material using a single etching process.

15. The method of claim 14, wherein using a single etching process comprises using an anisotropic plasma etching process.

16. The method of claim 15, further comprising causing at least one of the first layer of dielectric material and the second layer of dielectric material to exhibit a variable etch rate during the anisotropic plasma etching process.

17. The method of claim 16, further comprising doping the at least one of the first layer of dielectric material and the second layer of dielectric material with a dopant and causing the concentration of the dopant within the at least one of the first layer of dielectric material and the second layer of dielectric material to vary across a thickness of the at least one of the first layer of dielectric material and the second layer of dielectric material.

18. The method of any one of claims 13 through 17, further comprising forming a plurality of tight pitch spacers over the second layer of dielectric material, and etching the first layer of dielectric material through the plurality of spacers to form the plurality of tight pitch trenches.

19. The method of any one of claims 13 through 18, wherein at least one of forming the plurality of tight pitch trenches and forming the plurality of tight pitch contact holes comprises at least one of a pitch multiplication process, a double-patterning process, a double exposure process, a maskless photolithography process, and an advanced fine line lithography process.

20. The method of any one of claims 13 through 19, further comprising:

providing conductive material in each tight pitch trench of the plurality of tight pitch trenches to form the plurality of tight pitch conductive lines; and

providing the conductive material in each tight pitch contact hole of the plurality of tight pitch contact holes to form the plurality of tight pitch conductive contacts.

21. The method of claim 20, further comprising substantially concurrently introducing conductive material into each tight pitch trench of the plurality of tight pitch trenches and each tight pitch contact hole of the plurality of tight pitch contact holes.

22. The method of claim 13, further comprising:

forming another mask layer having a plurality of apertures having a tight pitch over the second layer of dielectric material; and

etching the second layer of dielectric material and the first layer of dielectric material through the plurality of apertures of the another mask layer and the aperture of the mask layer to form the plurality of tight pitch trenches in the second layer of dielectric material and the plurality of tight pitch contact holes in the first layer of dielectric material.

23. The method of claim 22, wherein forming another mask layer comprises using a spacer etch process to form the plurality of apertures in the another mask layer.

What is claimed is:

1. A semiconductor structure comprising:

a plurality of tight pitch conductive lines formed over a mask comprising a material being at least partially resistant to an etching process; and

a plurality of tight pitch conductive contacts each extending through an aperture formed in the mask, wherein each tight pitch conductive line of the plurality of tight pitch conductive lines is integrally formed with one tight pitch conductive contact of the plurality of tight pitch conductive contacts, wherein each tight pitch conductive contact of the plurality of tight pitch conductive contacts extends through a common aperture in the mask.

2. The semiconductor structure of claim 1, wherein the plurality of tight pitch conductive contacts comprise a plurality of conductive vias.

3. The semiconductor structure of claim 2, wherein each conductive via of the plurality of conductive vias extends from one tight pitch conductive line of the plurality of tight pitch conductive lines to a tight pitch active area on a semiconductor substrate.

4. The semiconductor structure of claim 2, wherein the tight pitch active area comprises at least a portion of a feature selected from the group consisting of a source, a drain, a gate, a conductive pad and a conductive trace.

5. The semiconductor structure of claim 1, wherein the plurality of tight pitch conductive lines and the plurality of tight pitch conductive contacts each have a width of less than about 50 nm.

6. The semiconductor structure of claim 1, wherein the plurality of tight pitch conductive lines and the plurality of tight pitch conductive contacts each have a width of less than about 30 nm.

7. The semiconductor structure of claim 1, wherein each integrally formed tight pitch conductive line of the plurality of tight pitch conductive lines and tight pitch conductive contact of the plurality of tight pitch conductive contacts comprises a unitary mass of at least one of tungsten, copper, aluminum, and nickel.

8. The semiconductor structure of claim 1, wherein the plurality of tight pitch conductive lines extend in a direction substantially parallel to one another.

9. The semiconductor structure of claim 1, wherein each of the plurality of tight pitch conductive contacts comprises a conductive via, and wherein each conductive via extends from one tight pitch conductive line of the plurality of tight pitch conductive lines to a tight pitch active area on a semiconductor substrate.

10. The semiconductor structure of claim 9, wherein the common aperture in the mask is elongated and extends over the semiconductor substrate in a direction generally perpendicular to the plurality of tight pitch conductive lines.

11. The semiconductor structure of claim 9, wherein each tight pitch conductive contact of the plurality of tight pitch conductive contacts extends through a dielectric layer disposed over the semiconductor substrate, and wherein the mask is disposed over the dielectric layer.

12. The semiconductor structure of claim 11, wherein the dielectric layer comprises a dopant gradient in a direction from a region proximate the mask to a region proximate the semiconductor substrate.

13. A semiconductor structure comprising:

a semiconductor substrate comprising a plurality of tight pitch active areas;

a plurality of tight pitch conductive lines extending over the semiconductor substrate; and

a plurality of tight pitch conductive contacts each extending from one conductive line of the plurality of conductive lines through a common aperture in a mask layer to one tight pitch active area of the plurality of tight pitch active areas.

14. The semiconductor structure of claim 13, wherein each tight pitch conductive line of the plurality of tight pitch conductive lines is integrally formed with a corresponding one tight pitch conductive contact of the plurality of tight pitch conductive contacts.

15. The semiconductor structure of claim 13, wherein the common aperture in the mask layer is elongated and extends in a lateral direction over the semiconductor substrate in a direction generally perpendicular to the plurality of tight pitch conductive lines.

16. The semiconductor structure of claim 13, wherein at least one of the plurality of tight pitch active areas comprises at least a portion of a feature selected from the group consisting of a source, a drain, a gate, a conductive pad and a conductive trace.

17. The semiconductor structure of claim 13, wherein the plurality of tight pitch conductive lines and the plurality of tight pitch conductive contacts each have a width of less than about 50 nm.

18. The semiconductor structure of claim 13, wherein the plurality of tight pitch conductive lines and the plurality of tight pitch conductive contacts each have a width of less than about 30 nm.

19. The semiconductor structure of claim 13, wherein the plurality of tight pitch conductive lines extend in a direction substantially parallel to one another.