[0034] The cross-over current mirror driver 144 may include fabricating the standard driver circuit 142 with a fifth transistor 146, such as a p-channel metal oxide semiconductor (pMOS) transistor, having a fifth source 148, a fifth drain 150, and a fifth gate 152. The fifth source 148 may be coupled to the first source voltage 110, and the fifth gate 152 may be coupled to the third gate 130 and an input node 154.

[0035] The input node 154 may be coupled to a signaling source (not shown) within the chip that contains the cross-over current mirror driver 144. A single ended signal (not shown) may switch in a specified pattern in order to activate the positive output node 112 and the negative output node 132 and thereby transfer information to a second chip.

[0036] The fifth drain 150 may be cross-coupled to an eighth drain 176 of an eighth transistor 178, such as an n-channel metal oxide semiconductor (nMOS) transistor, an eighth gate 180, and the second gate 120. An eighth source 182 may be coupled to the second voltage 122.

[0037] The cross-over current mirror driver 144 may also include fabricating a seventh transistor 164, such as a p-channel metal oxide semiconductor (pMOS) transistor, having a seventh source 166, a seventh drain 168, and a seventh gate 170. The seventh source 166 may be coupled to the first source voltage 110, and the seventh gate 170 may be coupled to the first gate 108 and an inverted input 172.

[0038] The inverted input 172, such as a single-ended input circuit, may be driven by an inverter 174 that is coupled between the input node 154 and the cross-over current mirror driver 144. The inverter 174 may be any high speed complimentary metal oxide semiconductor (CMOS) device. The inverter 174 may also have connections to the first source voltage 110 and the second voltage 122, but these connections have been omitted for clarity of the figure.

[0039] The seventh drain 168 may be cross-coupled to a sixth drain 156 of a sixth transistor 158, such as an n-channel metal oxide semiconductor (nMOS) transistor, a sixth gate 160, and the fourth gate 140. A sixth source 162 may be coupled to the second voltage 122.

[0040] It has been discovered that by coupling the fifth transistor 146, the sixth transistor 158, the seventh transistor 164, and the eighth transistor 178 in a cross-coupled configuration as described above, the positive output node 112 and the negative output node 132 will always switch symmetrically, such as the output crossing point being kept within the specification limits, independent of the process variations. This discovery may represent a significant increase in process yield delivering a reduction in cost of manufacture.

[0041] Thus, it has been discovered that the integrated circuit communication system and device of the present invention furnishes important and heretofore unknown and unavailable solutions, capabilities, and functional aspects for increasing the process yield for integrated circuits containing a differential driver without adding significant space to the design.

[0042] The invention is enabled by the fifth transistor 146 sourcing a first reference current to the eighth transistor 178 which is coupled to the second transistor 116 as a current mirror, such as a first current mirror. Any change in parametric capabilities in the transistors will be reflected in the reference current and thus regulate the transition of the positive output node 112 and the negative output node 132.

[0043] The same enabling takes place by the seventh transistor 164 sourcing a second reference current to the sixth transistor 158 which is coupled to the fourth transistor 136 as a current mirror, such as a second current mirror. The parametric characteristics of pMOS transistors, being the first transistor 102, the third transistor 124, the fifth transistor 146, and the seventh transistor 164, will always be matched because they are fabricated in close proximity on the integrated circuit (not shown).

[0044] The parametric characteristics of nMOS transistors, being the second transistor 116, the fourth transistor 136, the sixth transistor 158, and the eighth transistor 178, will always be matched because they are fabricated in close proximity on the integrated circuit (not shown). While the parametric characteristics of the pMOS transistors may be dramatically different from the parametric characteristics of the nMOS transistors, the configuration of the present invention maintains a symmetrical transition of the positive output node 112 and the negative output node 132.

[0045] The size of the transistors may be in a ratio such that the first transistor 102 may source the same amount of current that the fourth transistor 136 is capable of sinking. This balance of current handling capacity is necessary since the current flows from the first transistor 102 to the positive output node 112, through the external wiring (not shown), back into the negative output node 132 and through the fourth transistor 136. A similar crossing pattern is true for the third transistor 124 and the second transistor 116.

[0046] Thus it has been discovered that the integrated circuit communication system 100, of the present invention, provides a reliable and manufacturable differential driver for chip-to-chip communication that is not impacted by changes in the parametric characteristics caused by manufacturing process variations.

What is claimed is:

1. A method of manufacture of an integrated circuit communication system comprising:

providing a semiconductor wafer; and

fabricating a cross-over current mirror driver on the semiconductor wafer for generating a crossing point at a reference voltage.

2. The method as claimed in claim 1 further comprising fabricating a positive output node and a negative output node in the cross-over current mirror driver.

3. The method as claimed in claim 1 wherein providing the semiconductor wafer includes providing a wafer from outside of a nominal region of a process control chart.

4. The method as claimed in claim 1 wherein fabricating the cross-over current mirror driver includes coupling a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor to a standard driver circuit in a cross-coupled configuration.

5. The method as claimed in claim 1 further comprising fabricating an electronic device including:

providing a first integrated circuit having the cross-over current mirror driver;

coupling a second integrated circuit to the first integrated circuit; and

providing a conductive link between the first integrated circuit and the second integrated circuit for signaling by the cross-over current mirror driver.

6. A method of manufacture of an integrated circuit communication system comprising:

providing a semiconductor wafer having integrated circuits; and

fabricating a cross-over current mirror driver in the integrated circuits on the semiconductor wafer for generating a crossing point at a reference voltage including sending a clock, data, or a combination thereof.

7. The method as claimed in claim 6 further comprising fabricating a positive output node and a negative output node in the cross-over current mirror driver for sourcing a positive output waveform and a negative output waveform.

8. The method as claimed in claim 6 wherein providing the semiconductor wafer includes providing a wafer from outside of a nominal region of a process control chart

including providing a fast/fast wafer, a fast/slow wafer, a slow/slow wafer, or a slow/fast wafer.

9. The method as claimed in claim 6 wherein fabricating the cross-over current mirror driver includes coupling a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor to a standard driver circuit in a cross-coupled configuration including mirroring a current from the sixth transistor to a fourth transistor and from the eighth transistor to a second transistor.

10. The method as claimed in claim 6 further comprising fabricating an electronic device including:

providing a first integrated circuit having the cross-over current mirror driver including providing a microprocessor;

coupling a second integrated circuit to the first integrated circuit in which coupling the second integrated circuit includes coupling a display controller, a camera chip, an audio controller, or a combination thereof; and

providing a conductive link between the first integrated circuit and the second integrated circuit for signaling by the cross-over current mirror driver in which providing the conductive link includes providing a flex circuit, a cable, printed circuit board traces, or a combination thereof.

11. An integrated circuit communication system comprising:

a semiconductor wafer; and

a cross-over current mirror driver fabricated on the semiconductor wafer for generating a crossing point at a reference voltage.

12. The system as claimed in claim 11 further comprising a positive output node and a negative output node in the cross-over current mirror driver.

13. The system as claimed in claim 11 wherein the semiconductor wafer includes a wafer from outside of a nominal region of a process control chart.

14. The system as claimed in claim 11 wherein the cross-over current mirror driver includes a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor coupled to a standard driver circuit in a cross-coupled configuration.

15. The system as claimed in claim 11 further comprising an electronic device including:

a first integrated circuit having the cross-over current mirror driver;

a second integrated circuit coupled to the first integrated circuit; and

a conductive link between the first integrated circuit and the second integrated circuit coupled to the cross-over current mirror driver.

16. The system as claimed in claim 11 further comprising integrated circuits, having the cross-over current mirror driver, on the semiconductor wafer for sending a clock, data, or a combination thereof.

17. The system as claimed in claim 16 further comprising a positive output node and a negative output node, in the cross-over current mirror driver, for sourcing a positive output waveform and a negative output waveform.

18. The system as claimed in claim 16 wherein the semiconductor wafer includes a wafer from outside of a nominal region of a process control chart including a fast/fast wafer, a fast/slow wafer, a slow/slow wafer, or a slow/fast wafer.

19. The system as claimed in claim 16 wherein the cross-over current mirror driver includes a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor coupled to a standard driver circuit in a cross-coupled configuration including a current mirrored from the sixth transistor to a fourth transistor and from the eighth transistor to a second transistor.

20. The system as claimed in claim 16 further comprising an electronic device including:

a first integrated circuit having the cross-over current mirror driver in which the first integrated circuit is a microprocessor;

a second integrated circuit coupled to the first integrated circuit in which the second integrated circuit is a display controller, a camera chip, an audio controller, or a combination thereof; and

a conductive link between the first integrated circuit and the second integrated circuit coupled to the cross-over current mirror driver in which the conductive link is a flex circuit, a cable, printed circuit board traces, or a combination thereof.

What is claimed is:

1. A method of manufacture of an integrated circuit communication system comprising:

providing a semiconductor wafer; and

fabricating a cross-over current mirror driver, having a single ended input circuit coupled to a first current mirror and a second current mirror, on the semiconductor wafer, the first current mirror sourcing a first reference current and the second current mirror sourcing a second reference current for regulating a transition region of a positive output waveform and a negative output waveform.

2. The method as claimed in claim 1 further comprising fabricating a positive output node and a negative output node in the cross-over current mirror driver.

3. The method as claimed in claim 1 wherein providing the semiconductor wafer includes providing a wafer from outside of a nominal region of a process control chart.

4. The method as claimed in claim 1 wherein fabricating the cross-over current mirror driver including fabricating a first transistor, a second transistor, a third transistor, and a fourth transistor includes coupling a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor to a standard driver circuit in a cross-coupled configuration.

5. The method as claimed in claim 1 further comprising fabricating an electronic device including:

providing a first integrated circuit having the cross-over current mirror driver;

coupling a second integrated circuit to the first integrated circuit; and

providing a conductive link between the first integrated circuit and the second integrated circuit for signaling by the cross-over current mirror driver.

6. A method of manufacture of an integrated circuit communication system comprising:

providing a semiconductor wafer having integrated circuits; and

fabricating a cross-over current mirror driver, having a single ended input circuit coupled to a first current mirror and a second current mirror, in the integrated circuits on the semiconductor wafer for sending a clock, data, or a combination thereof, the first current mirror sourcing a first reference current and the second current mirror sourcing a second reference current for

regulating a transition region of a positive output waveform and a negative output waveform.

7. The method as claimed in claim 6 further comprising:

fabricating a positive output node and a negative output node in the cross-over current mirror driver for sourcing the positive output waveform and the negative output waveform; and

coupling an inverter to the cross-over current mirror driver.

8. The method as claimed in claim 6 wherein providing the semiconductor wafer includes providing a wafer from outside of a nominal region of a process control chart including providing a fast/fast wafer, a fast/slow wafer, a slow/slow wafer, or a slow/fast wafer.

9. The method as claimed in claim 6 wherein fabricating the cross-over current mirror driver including fabricating a first transistor, a second transistor, a third transistor, and a fourth transistor includes coupling a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor to a standard driver circuit in a cross-coupled configuration including mirroring a current from the sixth transistor to a fourth transistor and from the eighth transistor to a second transistor.

10. The method as claimed in claim 6 further comprising fabricating an electronic device including:

providing a first integrated circuit having the cross-over current mirror driver including providing a microprocessor;

coupling a second integrated circuit to the first integrated circuit in which coupling the second integrated circuit includes coupling a display controller, a camera chip, an audio controller, or a combination thereof; and

providing a conductive link between the first integrated circuit and the second integrated circuit for signaling by the cross-over current mirror driver in which providing the conductive link includes providing a flex circuit, a cable, printed circuit board traces, or a combination thereof.

11. An integrated circuit communication system comprising:

a semiconductor wafer; and

a cross-over current mirror driver, with a single ended input circuit, fabricated on the semiconductor wafer, the cross-over current mirror driver including:

a first current mirror coupled to the single ended input circuit, and

a second current mirror coupled to the single ended input circuit, the first current mirror sourcing a first reference current and the second current mirror sourcing a second reference current for regulating a transition region of the positive output waveform and the negative output waveform.

12. The system as claimed in claim 11 further comprising a positive output node and a negative output node in the cross-over current mirror driver.

13. The system as claimed in claim 11 wherein the semiconductor wafer includes a wafer from outside of a nominal region of a process control chart.

14. The system as claimed in claim 11 wherein the cross-over current mirror driver with a first transistor, a second transistor, a third transistor, and a fourth transistor includes a fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor coupled to a standard driver circuit in a cross-coupled configuration.

15. The system as claimed in claim 11 further comprising an electronic device including:

a first integrated circuit having the cross-over current mirror driver;

a second integrated circuit coupled to the first integrated circuit; and

a conductive link between the first integrated circuit and the second integrated circuit coupled to the cross-over current mirror driver.

16. The system as claimed in claim 11 further comprising integrated circuits, having the cross-over current mirror driver, on the semiconductor wafer for sending a clock, data, or a combination thereof.

17. The system as claimed in claim 16 further comprising a positive output node and a negative output node, in the cross-over current mirror driver, for sourcing the positive output waveform and the negative output waveform.

18. The system as claimed in claim 16 wherein the semiconductor wafer includes a wafer from outside of a nominal region of a process control chart including a fast/fast wafer, a fast/slow wafer, a slow/slow wafer, or a slow/fast wafer.

19. The system as claimed in claim 16 wherein the cross-over current mirror driver with a first transistor, a second transistor, a third transistor, and a fourth transistor includes a

fifth transistor, a sixth transistor, a seventh transistor, and an eighth transistor coupled to a standard driver circuit in a cross-coupled configuration including a current mirrored from the sixth transistor to a fourth transistor and from the eighth transistor to a second transistor.

20. The system as claimed in claim 16 further comprising an electronic device including:

a first integrated circuit having the cross-over current mirror driver in which the first integrated circuit is a microprocessor;

a second integrated circuit coupled to the first integrated circuit in which the second integrated circuit is a display controller, a camera chip, an audio controller, or a combination thereof; and

a conductive link between the first integrated circuit and the second integrated circuit coupled to the cross-over current mirror driver in which the conductive link is a flex circuit, a cable, printed circuit board traces, or a combination thereof.