For Reference only.
1) original specs
2) Replacement sheets
[8/10/99]

Coupling Spaced Bond Pads To A Contact

Background

This invention relates generally to packaging integrated circuit devices.

In some cases it is desirable to provide two integrated circuit devices inside a single package. Sometimes, it may not be feasible to integrate the components of both integrated circuits into a single integrated circuit. Thus, two integrated circuit devices may be combined within a single package to give combined capabilities at a plurality of output pins.

At times, signals from pads on the two different dice need to be coupled to the same output pin. One reason why this may occur is that the number of pins on the package may be limited. Thus, it may be undesirable to have two separate pins that provide or receive the same signal.

The location of bond pads between two dice may not allow direct wirebonding from both pads to a common leadfinger. This is especially likely to occur when two separate dice are used within the same package.

Thus, there is a need for a way to allow spaced apart bond pads to be coupled to the same contact.

Summary

In accordance with one aspect, a method of electrically coupling first and second bond pads on different chips to the same contact includes positioning a conductive trace on a support between the different chips. The first bond pad is coupled to the trace. The trace is coupled to the contact. The second bond pad is then coupled to the contact.

Other aspects are set forth in the accompanying detailed description and claims.

Brief Description of the Drawings

Fig. 1 is a greatly enlarged top plan view of one embodiment of the present invention;

Fig. 2 is cross-sectional view taken generally along the line 2-2 in Fig. 1;

Fig. 3 is a greatly enlarged top plan view of another embodiment of the present invention;

Fig. 4 is a greatly enlarged top plan view of still another embodiment of the present invention; and

Fig. 5 is a greatly enlarged longitudinal cross-sectional view of another embodiment of the present invention.

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Detailed Description

Referring to Fig. 1, an integrated circuit package 10 may contain a pair of chips 14 and 16. In one embodiment of the present invention, each chip may be a memory array. It may be desirable to couple some of the bond pads 18 and 20 on each chip to the same leadfinger 22a for connection to the same external pin 12a. This may be useful for pins that provide output or input signals for the pair of dice.

Each chip includes bond pads 18 or 20 which may be coupled by wire bond wires 30 to leadfingers 22 and pins 12. A bond pad 18 on the die 14 may be coupled to a leadfinger 22a on the die 20 using an adhesive tape 32. The adhesive tape 32, adhesively secured to both dice, bridges the gap A between the two dice. A plurality of parallel conductive traces 24 may be pre-formed on the tape 32. Thus, a plurality of avenues for interconnection between the two dice are made available by the parallel conductive traces 24.

Thus, for example, the bond pad 18a may be coupled by a wire bond wire 26 to one end of a trace 24. The other end of the trace 24 is coupled by a wire bond 28 to the leadfinger 22a. Similarly, the pad 20a is coupled by the wire 30 to the same leadfinger 22a. In this way, both pads 20a and 18a are coupled to the same pin 12a.

Referring to Fig. 2, the tape 32 may have a plurality of traces 24 deposited thereon on one side of the tape with adhesive on the other side of the tape. The tape may be adhesively secured to both die 14 and 16 with the traces 24 facing upwardly. A die coat may be used to electrically isolate the tape 32 from the chips 14 and 16. The conductive trace may be coated with gold, for example using an immersion technique, while the adhesive layer on the tape is protected. While a plurality of straight-lined conductive traces are illustrated, other shapes are possible as well, including diagonal or curved shapes.

The overall package 10 may be encapsulated in a material 34 as is conventional. The pins 12 extend out of the package 10 and are coupled to the dice 14 and 16 through the leadfingers 22 and the wires 28, 30 and 26. The leadfingers 22 may be coupled to the dice 14 and 20 using lead-on-chip (LOC) tape 36 as is conventional.

Thus, two dice can be contained in the same package and the pin count of the package may be reduced compared to the number of pins that would be needed to provide a separate pin for every single pad. This results in economies and compactness and makes it more feasible to combine multiple dice in a single integrated circuit package.

The tape 32 may be formed by bonding ductile copper foil to thin, flexible dielectric materials. Suitable dielectric materials including polyimide, polyester terephthalate, random fiber aramid, polyamide-imide Teflon®, and polyvinyl chloride. In addition, a non-woven mat of dacron polyester and glass fibers saturated in B-stage epoxy may be used. Copper foils may be directly clad to B-stage material. Suitable adhesives include epoxies, polyesters or acrylics. Epoxy systems include modified epoxies known as phenolic butyrals and nitrile phenolics. Acrylic adhesive systems may be used in high temperature applications. Polyesters can be used with polyester film. Metallic coated films may also be made using advanced vacuum deposition technology to bond copper to polyimide for example. Specially treated polyimide films may have an ultra thin coating of barrier metal applied to promote copper adhesion. The copper may then be electrodeposited onto the film.

In accordance with another embodiment of the present invention shown in Fig. 3, a die 40 may be contained in a package 42. A pin 12 may connect to a leadfinger 22 proximate to a bond pad 20. In this case, an adhesive tape 32a extends along the length of the die 40 from a leadfinger 22 on one end to a leadfinger 22b, on the other end, coupled to a pin 12b. A connection can be made from a bond pad 20c, widely spaced from the leadfinger 22b, using a conductive trace 24a formed on the tape 32a. For example, the bond pads 20 and 20c may be spaced too far apart to couple them by wirebonding.

Thus, a wire bond is made from the bond pad 20c to one end of the trace 24a. A wire bond is then made from the other end of the trace 24a to the leadfinger 22b. A wire bond may also be made from the bond pad 20b to the leadfinger 22b. In this way, two different bond pads, which are widely spaced apart, may be connected to the same leadfinger.

Referring next to Fig. 4, a package 44 includes a pair of bond pads 18b and 18c on a chip 14. The bond pads 18b and 18c may be coupled to the same leadfinger 22b on a chip 16 using a tape 32 with an L-shaped trace 24b. One end of the longer arm of the trace 24b may be wirebonded to the bond pad 18b. The other end of the longer arm of the trace may be wirebonded to the bond pad 18c. The short arm of the L-shaped trace 24b may be wirebonded directly to the leadfinger 22b. Similarly, the bond pad 20a on the chip 16 may be wirebonded to the trace 22b. In this case, three different wire bond bond pads on two different chips may be coupled to the same trace 22b. Thus, by custom designing the trace 24 on the tape 32, a variety of interconnection arrangements are possible.

Referring now to Fig. 5, still another embodiment of the present invention includes an adhesive tape 32b secured for example to a die 16. The embodiment shown in Fig. 5 is applicable to tape secured to one die as illustrated in Figs. 3 and tape secured across two dice as illustrated in Figs. 1, 2 and 4.

The tape 32b may be pre-attached to leadfingers 22. The tape 32b includes a tape core 42 covered by a conductive trace 24c which may extend along the entire length of the tape 32a. An insulator 44 may be disposed along two opposed longitudinally displaced edges. Thus, a window 43 is defined immediately between the longitudinal end portions which may be covered by the insulator 44. The insulator 44 may be covered by an adhesive material 46. The adhesive material 46 may be the same as the adhesive at the joint 48 formed by the tape 32b. Conventional adhesives used for lead-on-chip (LOC) tape may be utilized for this function.

Thus, the tape 32b may be pre-taped to the leadfingers 32. The tape 32b may then be applied using the adhesive 48 to the surface of one or more dice 16. Preferably, the tape runs longitudinally along the length of the die 16. This enables free access from either side in the latitudinal direction to bond pads along the die. For reference, in Fig. 1, the longitudinal direction would be up and down on the page.

With the embodiment shown in Fig. 5, the tape 32b may be pre-attached to an interposer such as a leadframe 22 without concern for shorting to the leadframe 22. Namely, the insulator 46 prevents shorting of the trace 24c to the leadframe fingers 22. Thus, in some instances, the tape 32b, shown in Fig. 5, may be more easily applied as a composite unit including a leadframe with the tape pre-attached. Moreover, the tape may not only provide the interconnection function described above, but may also function to secure the leadframe to one or more dice.

The tape 32b may be used in the same fashion as the tape 32. It may act as a bridge, for example, to allow wire bonds to extend from a bond pad to the conductive trace 24c and from the conductive trace 24c to a leadfinger.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

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1. A method of electrically coupling first and second bond pads to the same contact comprising:

securing a tape, with a conductive trace, on a support;

wirebonding said first bond pad to said trace;

wirebonding said trace to said contact; and

wirebonding said second bond pad to said contact.



2. The method of claim 1 wherein securing a tape includes forming a plurality of conductive traces on adhesive tape.

3. The method of claim 1 wherein securing a tape includes securing said tape across two chips, said first bond pad being on one of said chips and said second bond pad being on the other of said chips.

4. The method of claim 1 further including coupling said pair of bond pads on different chips to a leadfinger.

5. The method of claim 1 including coupling a first and second bond pad on the same chip.

6. The method of claim 1 including using said tape to secure a leadframe to a die.

7. A packaged integrated circuit device comprising:

a first chip and a second chip, one of said chips having a contact;

an adhesive tape adhesively coupled to said first and second chips, said tape having a trace formed on said tape;

a first bond pad on one of said chips and a second bond pad on the other of said chips, said first bond pad being wire bonded to said conductive trace, said conductive trace also being wirebonded to a contact; and

said second bond pad being wirebonded to said contact.

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8. The device of claim 7 including a plurality of conductive traces formed on said tape.



9. The device of claim 7 wherein said contact is a leadfinger.

10. The device of claim 7 including a package containing said first and second chips.

11. The device of claim 7 wherein said trace is gold coated.

12. The device of claim 7 including a leadframe, wherein said tape couples said leadframe to said chips and said contact is part of said leadframe.

13. A method of electrically coupling first and second bond pads on different dice to a leadfinger comprising:

packaging said first and second chips in the same package;

providing a leadframe for said chips;

positioning an adhesive tape on each of said chips, said adhesive tape having a conductive trace formed thereon;

wirebonding a first bond pad on said first chip to one end of said conductive trace and wirebonding the other end of said conductive trace to said leadframe; and

wirebonding a second bond pad on said second chip to said leadframe.

14. The method of claim 13 including using said tape to secure a leadframe to said chips.

15. The method of claim 14 including insulating said chips from said trace.

16. An integrated circuit device comprising:

an integrated circuit chip having a pair of spaced apart bond pads and a pin;

an adhesive tape having a conductive trace formed on said tape, said tape arranged along a path between said spaced apart bond pads;

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a wire bond from one said bond pads to said trace;
a wire bond from said trace to said pin; and
a wire bond from the other bond pad to said pin.



17. The device of claim 16 wherein said trace is gold coated.

18. The device of claim 16 wherein said pin includes a leadfinger.

19. The device of claim 16 wherein said bond pads are spaced too far apart to allow them to be wirebonded to one another.

20. The device of claim 16 including a leadframe, wherein said tape couples said leadframe to said chip and said contact is part of said leadframe.

21. A method of coupling spaced apart bond pads to the same contact comprising:
wirebonding one of said bond pads to a trace formed on an adhesive tape;
wirebonding the trace to the contact; and
wirebonding the other of said bond pads to said contact.

22. The method of claim 21 including securing said tape on a chip.

23. The method of claim 22 including arranging said tape so that said trace extends between said bond pads.

24. The method of claim 23 including gold coating said trace.

25. The method of claim 21 including using said tape to secure a leadframe to a die.

26. A method of coupling spaced apart bond pads to the same contact comprising:
securing an interposer to a die using adhesive tape;
wirebonding a first bond pad to a trace formed on said adhesive tape;

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wirebonding the trace to the contact; and

wirebonding a second bond pad to said contact.



27. The method of claim 26 wherein wirebonding the second bond pad to said contact includes wirebonding the second bond pad to said interposer.

28. The method of claim 26 including securing said tape on a chip.

29. The method of claim 28 including arranging said tape to extend longitudinally on said chip.

30. The method of claim 29 including gold coating said trace.

31. The method of claim 26 including adhesively securing said tape to said interposer and adhesively securing said tape to a die.

32. The method of claim 31 including insulating said interposer from said trace.

33. An adhesive tape for making connections on integrated circuit chips comprising:

a flexible tape layer having adhesive on one side thereof;

a conductive trace attached to the other side of said tape;

insulator covering a portion of said conductive trace; and

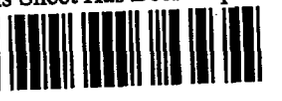
adhesive secured over said insulator.

34. The tape of claim 33 wherein said tape is adapted to couple an interposer to a die.

35. The tape of claim 33 wherein said interposer is a leadframe.

36. The tape of claim 35 wherein said insulator is positioned between said leadframe and said trace.

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37. An interposer comprising:

a structure;

an adhesive tape having a lower side and an upper side, said upper side secured to said structure;

a conductive trace defined on said upper side of said adhesive tape;

the lower side of said adhesive tape containing adhesive for securing said tape to a die;

an insulator covering a portion of said conductive trace; and

an adhesive material on said insulator to connect said tape to said structure.

38. The interposer of claim 37 wherein said structure is a leadframe.



39. A method comprising:

providing an adhesive tape on a leadframe;

using said adhesive tape to connect said leadframe to a die; and

forming wire bonds from said die to said adhesive tape.

40. The method of claim 39 including forming a conductive trace on said adhesive tape.

41. The method of claim 40 including insulating said conductive trace from said leadframe.

42. The method of claim 41 including wirebonding from a bond pad to said trace and from said trace to said leadfinger.

43. The method of claim 42 including securing said tape to a pair of dice.

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