CLAIMS:

1. An apparatus comprising:

a non-planar fin having first, second, and third portions each having major and minor axes and each being monolithic with each other; and

a system-on-chip (SoC);

wherein (a) the major axes of the first, second, and third portions are parallel with each other, (b) the major axes of the first and second portions are non-collinear with each other, (c) each of the first, second, and third portions includes a node of a transistor selected from the group comprising source, drain, or channel, (d) the first, second, and third portions comprise at least one finFET;

wherein the SoC includes the at least one finFET and an additional finFET;

wherein the additional finFET includes an additional non-planar fin that is not monolithic with the non-planar fin.

2. The apparatus of claim 1, wherein each of the first, second, and third portions includes a finFET having source, drain, and channel nodes, the non-planar fin included in at least three finFETs.

3. The apparatus of claim 1, wherein each of the first, second, and third portions includes a node of a single finFET.

4. The apparatus of claim 3, wherein the first, second, and third portions intersect with each other at a common portion that includes a channel for the single finFET.

5. The apparatus of claim 1 wherein (a) the non-planar fin includes a fourth portion having major and minor axes and being monolithic with the first, second, and third portions, (b) the major axes of the first, second, third, and fourth portions are parallel with each other, (c) the major axis of the fourth portion is non-collinear with at least one of the major axes of the first, second, or third portions.

6. The apparatus of claim 1:
wherein the additional non-planar fin includes additional first, second, and third portions each having additional major and minor axes and each being monolithic with each other;

wherein (a) the additional major axes of the additional first, second, and third portions are parallel with each other, (b) the additional major axes of the additional first and second portions are non-collinear with each other, (c) each of the additional first, second, and third portions includes a node of a transistor selected from the group comprising source, drain, or channel;

wherein the non-planar fin is immediately adjacent the additional non-planar fin, the non-planar fin and the additional non-planar fin are both included in the SoC, and the non-planar fin and the additional non-planar fin are not monolithic with each other.

7. The apparatus of claim 6, wherein the non-planar fin is antipodal to the additional non-planar fin such that the second portion is immediately adjacent the additional third portion and the third portion is immediately adjacent the additional first portion.

8. The apparatus of claim 1, wherein (a) each of the first, second, and third portions has a maximum width corresponding to its minor axis, and (b) the maximum width of the first portion is unequal to at least one of the maximum widths of the second or third portions.

9. The apparatus of claim 1, wherein the first and second portions each include a channel coupled to a single common gate contact, the channels for the first and second portions not directly contacting each other.

10. The apparatus of claim 1, wherein the first and second portions each include a source coupled to a single common source contact, the sources for the first and second portions not directly contacting each other.

11. The apparatus of claim 1, wherein the major axes of the first, second, and third portions are all non-collinear with each other.

12. The apparatus of claim 1 comprising a radio-frequency (RF) mixer that includes the first, second, and third portions.

13. The apparatus of claim 12, wherein the non-planar fin includes input nodes for a first signal and an oscillator signal and an output node for a mixed signal based on the first signal and the oscillator signal.

14. The apparatus of claim 13, wherein the first portion includes the input nodes for the first signal and the oscillator signal.

15. The apparatus of claim 14, wherein the second portion includes inputs nodes for an additional signal and an additional oscillator signal.

16. The apparatus of claim 13 wherein (a) the non-planar fin includes fourth and fifth portions each having major and minor axes and each being monolithic with the third portion, (b) the major axes of the third, fourth, and fifth portions are parallel with each other, (c) the major axes of the third and fourth portions are non-collinear with each other, (d) the third portion includes an additional input node.

17. The apparatus of claim 16, wherein the third portion is included in an amplifier.

18. The apparatus of claim 1 comprising a multiplexor (mux) that includes the first, second, and third portions.

19. The apparatus of claim 18, wherein (a) the first portion includes an input node for a first signal, (b) the second portion includes an input node for a second signal, (c) the third portion includes an output node for one of the first or second signals, and (d) and each of the first and second portions includes a selection node.

20. The apparatus of claim 19 wherein the selection nodes for the first and second portions each couple to a single selection signal source.

21. The apparatus of claim 19, wherein (a) the non-planar fin includes fourth and fifth portions each having major and minor axes and each being monolithic with the third portion, (b) the major axes of the third, fourth, and fifth portions are parallel with each other, (c) the major axes of the third and fourth portions are non-collinear with each other, (d) the third portion includes an additional signal selection node.

22. An apparatus comprising:

a non-planar fin having first, second, and third portions each having major and minor axes and each being monolithic with each other; and

an additional non-planar fin having additional first, second, and third portions each having additional major and minor axes and each being monolithic with each other;

wherein (a) the major axes of the first, second, and third portions are parallel with each other, (b) the major axes of the first and second portions are non-collinear with each other, (c) each of the first, second, and third portions includes a node of a transistor selected from the group comprising source, drain, and channel, (d) the first, second, and third portions comprise at least one finFET;

wherein (a) the additional major axes of the additional first, second, and third portions are parallel with each other, (b) the additional major axes of the additional first and second portions are non-collinear with each other, (c) each of the additional first, second, and third portions includes a node of a transistor selected from the group comprising source, drain, and channel, (d) the additional first, second, and third portions comprise at least one additional finFET;

wherein the non-planar fin is immediately adjacent the additional non-planar fin, the non-planar fin and the additional non-planar fin are both included in a single system-on-chip (SoC), and the non-planar fin and the additional non-planar fin are not monolithic with each other.