WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate including an active pattern;

a gate electrode crossing the active pattern in a plan view; and

a ferroelectric pattern interposed between the active pattern and the gate electrode,

wherein the gate electrode comprises:

a work function metal pattern disposed on the ferroelectric pattern;

an electrode pattern filling a recess formed in an upper portion of the work function metal pattern; and

a barrier pattern interposed between the electrode pattern and the work function metal pattern, the barrier pattern filling at least a portion of the recess,

wherein a top surface of a topmost portion of the ferroelectric pattern is lower than a bottom surface of the recess.

2. The device of claim 1, further comprising a gate spacer disposed on a side surface of the gate electrode,

wherein the ferroelectric pattern comprises a first portion disposed on a top surface of the active pattern and a second portion vertically extending from the first portion along an inner sidewall of the gate spacer.

3. The device of claim 1 or claim 2, wherein the ferroelectric pattern comprises hafnium oxide doped with at least one of zirconium (Zr), silicon (Si), aluminum (Al), and lanthanum (La).

4. The device of claim 3, wherein the ferroelectric pattern comprises a portion having an orthorhombic crystal structure, and

a volume of the portion having the orthorhombic crystal structure ranges from 10% to 50% of a volume of the ferroelectric pattern.

5. The device of any one of claims 1 to 4, wherein the work function metal pattern comprises a first work function metal pattern and a second work function metal pattern disposed on the first work function metal pattern,

wherein the first work function metal pattern comprises a metal nitride layer, and

wherein the second work function metal pattern comprises an aluminum-containing metal carbide or a silicon-containing metal carbide.

6. The device of any one of claims 1 to 5, further comprising a trench formed in the substrate to define the active pattern and a device isolation layer filling the trench,

wherein an upper portion of the active pattern vertically protrudes above the device isolation layer, and

wherein the ferroelectric pattern is provided on a top surface and opposite side surfaces of the upper portion of the active pattern.

7. The device of any one of claims 1 to 6, further comprising a pair of semiconductor patterns, the pair of semiconductor patterns stacked on the active pattern, and the pair of semiconductor patterns vertically spaced apart from each other,

wherein the ferroelectric pattern and the work function metal pattern fill a space

between the pair of the semiconductor patterns.

8. A semiconductor device, comprising:

a substrate including a first active pattern and a second active pattern;

a gate electrode crossing the first and second active patterns in a plan view; and

a ferroelectric pattern interposed between the first and second active patterns and the gate electrode,

wherein the gate electrode comprises:

a work function metal pattern disposed on the ferroelectric pattern;

a recess formed in an upper portion of the work function metal pattern;

an electrode pattern formed in the recess; and

a barrier pattern interposed between the electrode pattern and the work function metal pattern, the barrier pattern formed in the recess,

wherein a height difference between a bottom surface of the recess and a top surface of a topmost portion of the ferroelectric pattern formed on the first active pattern is different from a height difference between a bottom surface of the recess and a top surface of a topmost portion of the ferroelectric pattern formed on the second active pattern.

9. The device of claim 8, further comprising a gate spacer disposed on a side surface of the gate electrode,

wherein the ferroelectric pattern comprises a first portion disposed on a top surface of the first active pattern and a second portion vertically extending from the first portion along an inner sidewall of the gate spacer.

10. The device of claim 8 or claim 9, wherein the ferroelectric pattern comprises hafnium oxide doped with at least one of zirconium (Zr), silicon (Si), aluminum (Al), and lanthanum (La).

11. The device of claim 10, wherein the ferroelectric pattern comprises a portion having an orthorhombic crystal structure, and

wherein a volume of the portion having the orthorhombic crystal structure ranges from 10% to 50% of a volume of the ferroelectric pattern.

12. The device of any one of claims 8 to 11, further comprising a first source/drain pattern and a second source/drain pattern provided on the first active pattern and the second active pattern, respectively,

wherein the first and second source/drain patterns are disposed on side portions of the gate electrode in a plan view, and

wherein the first and second source/drain patterns have conductivity types different from each other.

13. The device of any one of claims 8 to 12, wherein the work function metal pattern comprises a first work function metal pattern and a second work function metal pattern disposed on the first work function metal pattern, and

wherein a thickness of the first work function metal pattern disposed on the first active pattern is different from a thickness of the first work function metal pattern disposed on the second active pattern.

14. A semiconductor device, comprising:

a substrate including an active pattern;

a gate electrode crossing the active pattern in a plan view;

a gate spacer disposed on a side surface of the gate electrode; and

a ferroelectric pattern interposed between the active pattern and the gate electrode,

wherein the ferroelectric pattern comprises a first portion disposed on a top surface of the active pattern and a second portion extending from the first portion along an inner sidewall of the gate spacer,

wherein the gate electrode comprises:

a first work function metal pattern disposed on the ferroelectric pattern and a second work function metal pattern disposed on the first work function metal pattern, wherein the second work function metal pattern has a recess formed in an upper portion of the second work function metal pattern;

an electrode pattern formed in the recess; and

a barrier pattern interposed between the electrode pattern and the second work function metal pattern, the barrier pattern formed in the recess,

wherein the second work function metal pattern covers a top surface of the second portion of the ferroelectric pattern.

15. The device of claim 14,

wherein a top surface of the second portion of the ferroelectric pattern is lower than a bottom surface of the recess.

16. The device of claim 14 or claim 15, wherein the ferroelectric pattern comprises

hafnium oxide doped with at least one of zirconium (Zr), silicon (Si), aluminum (Al), and lanthanum (La).

17. The device of any one of claims 14 to 16, wherein the first work function metal pattern comprises a metal nitride layer, and

wherein the second work function metal pattern comprises an aluminum-containing metal carbide or silicon-containing metal carbide.

18. The device of any one of claims 14 to 17, further comprising a trench formed in the substrate defining the active pattern and a device isolation layer formed in the trench,

wherein an upper portion of the active pattern vertically protrudes above the device isolation layer, and

wherein the ferroelectric pattern is provided on a top surface and opposite side surfaces of the upper portion of the active pattern.