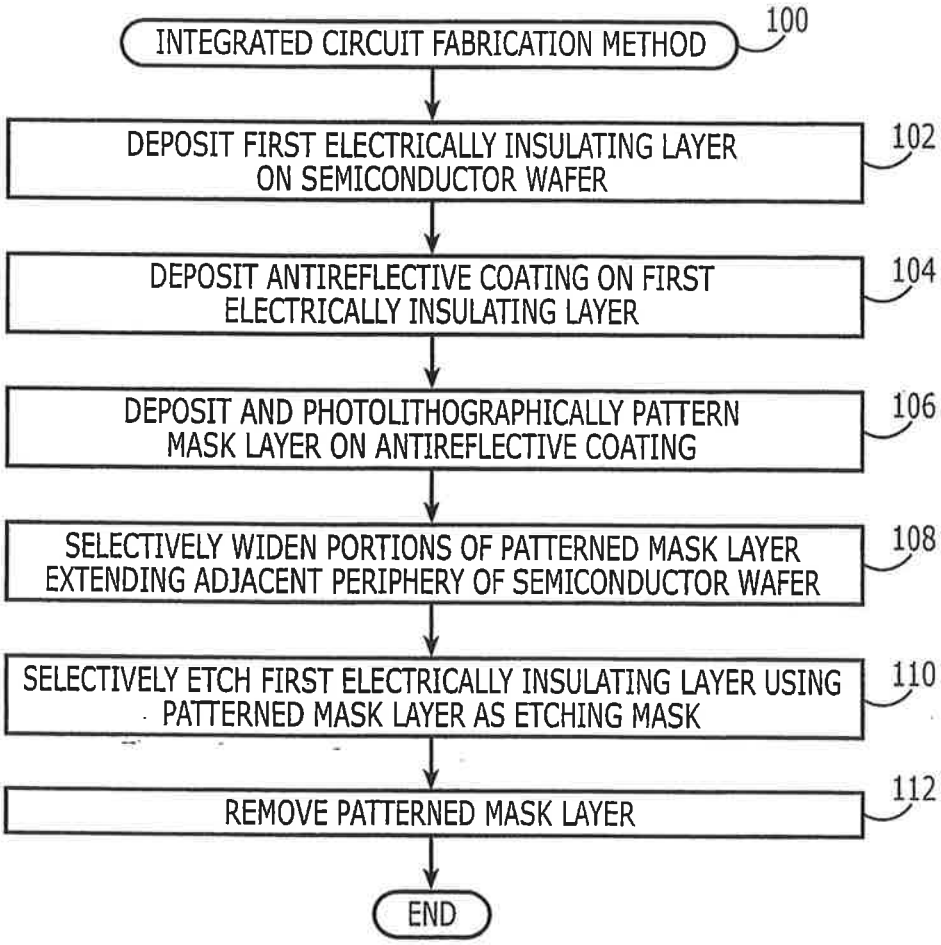

INTEGRATED CIRCUIT FABRICATION METHOD
100
DEPOSIT FIRST ELECTRICALLY INSULATING LAYER ON SEMICONDUCTOR WAFER
102
DEPOSIT ANTIREFLECTIVE COATING ON FIRST ELECTRICALLY INSULATING LAYER
104
DEPOSIT AND PHOTOLITHOGRAPHICALLY PATTERN MASK LAYER ON ANTIREFLECTIVE COATING
106
SELECTIVELY WIDEN PORTIONS OF PATTERNED MASK LAYER EXTENDING ADJACENT PERIPHERY OF SEMICONDUCTOR WAFER
108
SELECTIVELY ETCH FIRST ELECTRICALLY INSULATING LAYER USING PATTERNED MASK LAYER AS ETCHING MASK
110
REMOVE PATTERNED MASK LAYER
112
END

FIG. 1

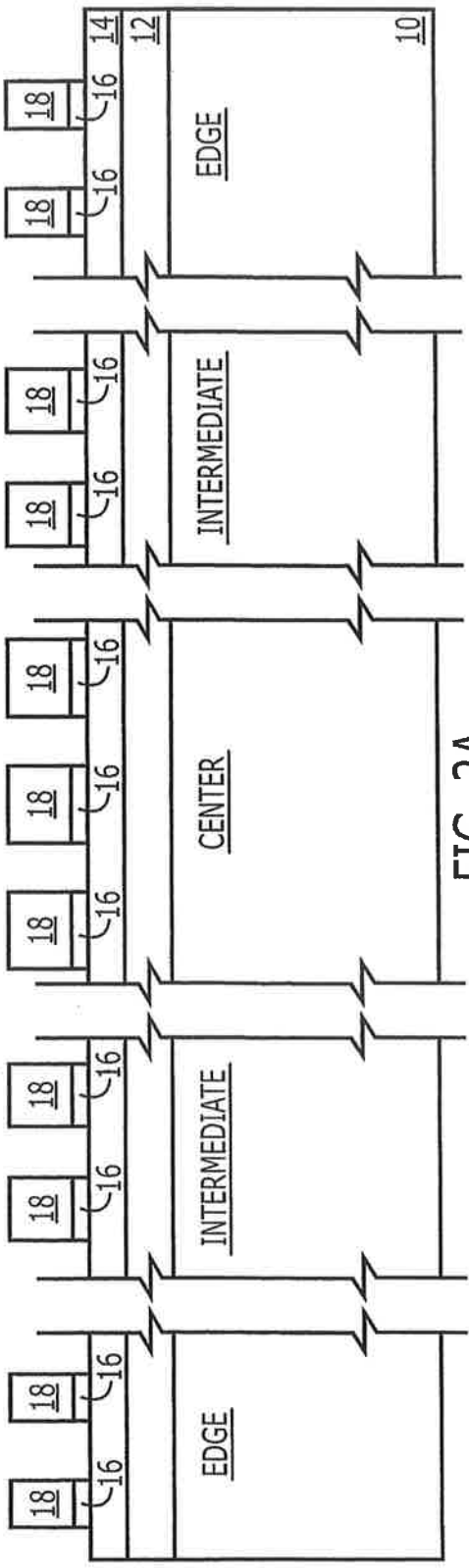


FIG. 2A

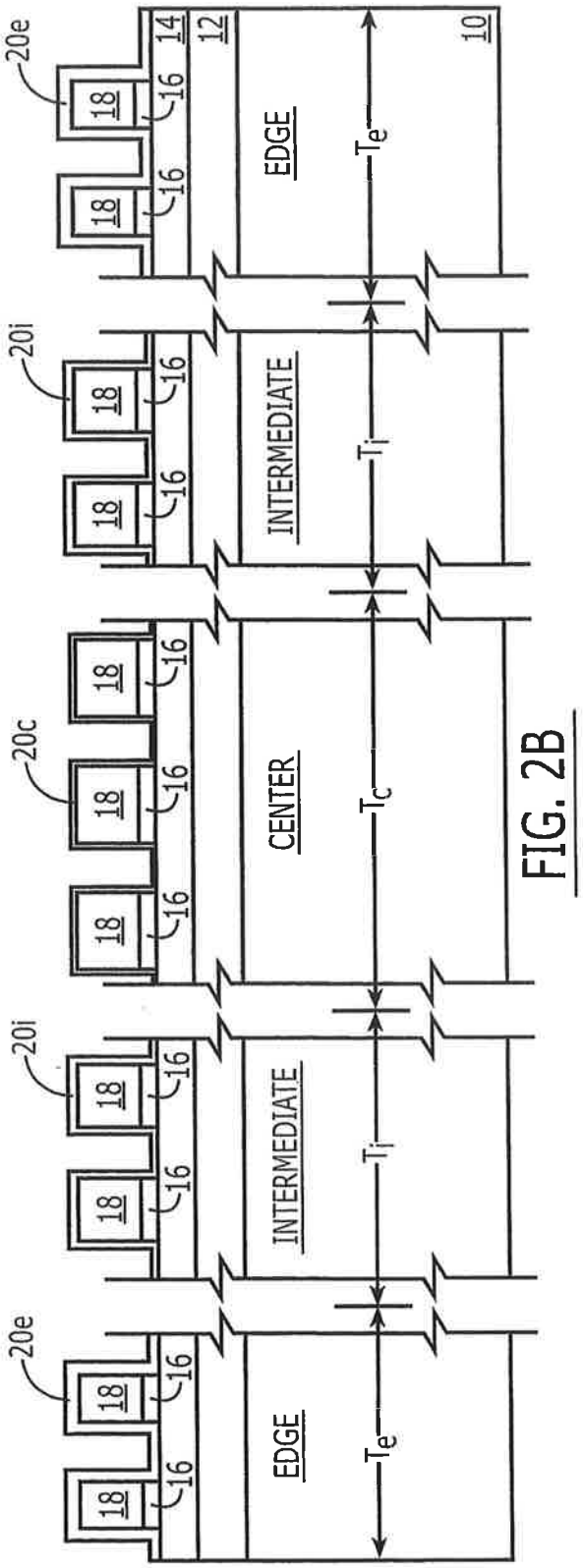

20e
20i
20c
20i
20e
18
16
14
12
10
EDGE
INTERMEDIATE
CENTER
INTERMEDIATE
EDGE
T_e
T_i
T_c
T_i
T_e

FIG. 2B

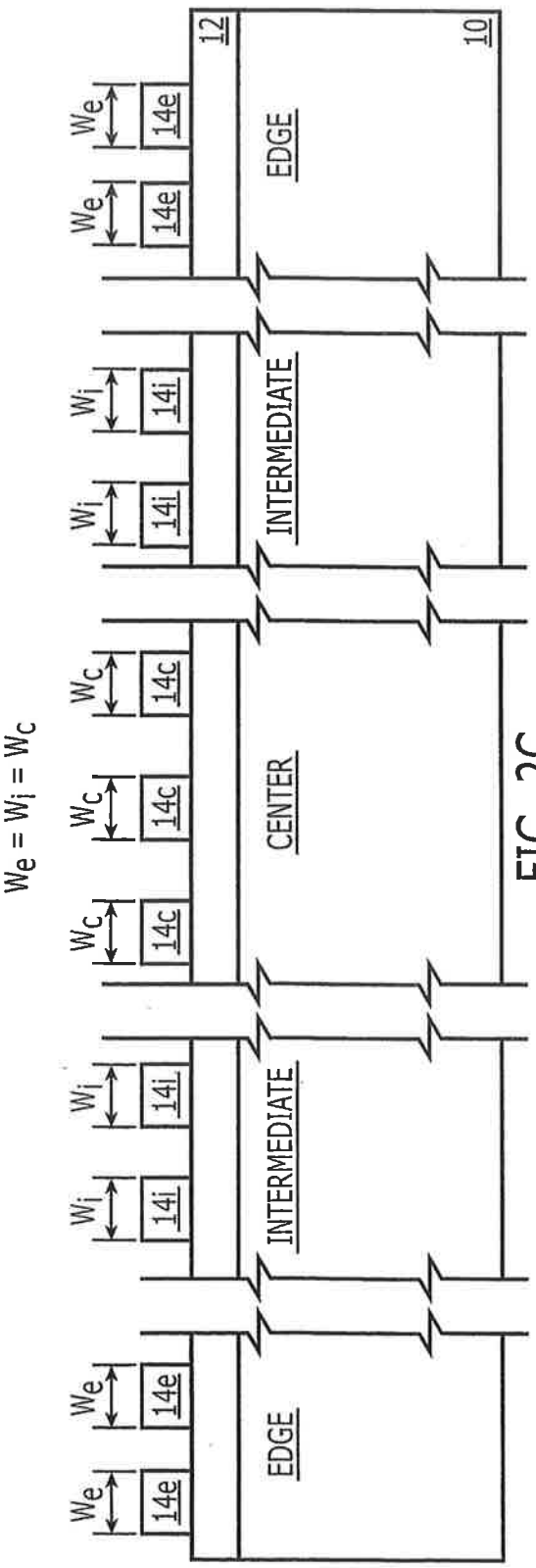

12
10
EDGE
INTERMEDIATE
CENTER
INTERMEDIATE
EDGE
We
Wi
Wc
14e
14i
14c
We = Wi = Wc

FIG. 2C