

QUANTUM CHIP OF QUBITS

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The present invention is related to a quantum chip of qubits, to a method for manufacturing a quantum chip for implementation of a local fermion-to-qubit mapping, to a method for simulating a fermionic system on the quantum chip and to a method for performing quantum error detection and/or correction using the quantum chip.

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Quantum chips based on superconducting qubits usually have a limited connectivity between them. In general, the qubit connectivity graph of these chips is planar, meaning that there are no crossings between coupling structures, like tunable couplers, providing connectivity between qubits. Examples of such architectures include the Sycamore square lattice architecture of Google, the IQM square lattice architecture as in <https://meetiqm.com/resources/press-releases/finland-launches-a-20-qubit-quantum-computer/>, the heavy-hex lattice of IBM, or the 4.8.8 lattice of Rigetti. The reason for the planar connectivity graph of all the existing quantum processors is that crossings of coupling structures are, from a technical point of view, challenging to implement.

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On one hand, one can engineer crossings of coupling structures by using airbridges (see e.g. EP 1 986 232 A2 or EP 3 869 553 A1). These are, however, considered as an unreliable hardware element, which may cause the deterioration of the quality of the chip. Furthermore, due to their vertical extent it is not possible to simultaneously implement airbridges and the flip-chip technology, where elements of the chip are placed at superimposed layers so that they face each other, and which is currently used by many manufacturers, see e.g. US 2022/0138611 A1.

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In terms of connectivity and the possibility to connect distant qubits with each other, (waveguide) resonators or other signal-conducting transmission lines, are far superior to tunable couplers which are standardly used in the aforementioned architectures. In particular, resonators may connect more than 10 qubits, and in some cases even more than 20 qubits with each other, whilst standard tunable couplers based on qubits allow for a connectivity roughly up to 8 before their performance starts to deteriorate significantly. However, as for tunable couplers, crossings between resonators/transmission lines or between resonators/transmission lines and tunable couplers located on the same layer are preferably avoided when designing a quantum chip.

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The understanding of fermionic quantum many-body systems is of fundamental importance in many fields including quantum chemistry, material science and pharmaceuticals. As the simulation of fermionic quantum many-body systems on a classical computer is often not possible due to the exponential growth of the underlying Hilbert space, it may be desirable to
5 compute or simulate properties of these systems using a quantum computer.

Whenever one is interested in computing properties of a fermionic quantum system on a quantum computer comprising a plurality of qubits, it is necessary to map the fermionic degrees of freedom to qubit degrees of freedom whilst adhering to the correct fermionic anti-
10 commutation relations. This may be achieved by fermion-to-qubit mappings and there are many different ones with various advantages and disadvantages depending on the particular problem. One of the most prominent fermion-to-qubit mappings is the Jordon-Wigner transformation, which maps m fermionic mode operators to Pauli operators defined on m qubits. However, this mapping generally introduces highly non-local operators with high
15 weight, especially when one aims at computing properties of fermionic systems in more than one spatial dimension.

An alternative class of mappings are so-called local fermionic-to-qubit mappings, where m fermionic mode operators are mapped to operators defined on more than m qubits in order
20 to resolve the anti-commutation relations locally. Examples of such mappings include the Bravyi-Kitaev Superfast (BKSF) Encoding (S. Bravyi, A. Kitaev, "Fermionic Quantum Computation", Annals of Physics, 298(1):210-226, 2002), the Generalized Superfast Encoding (GSE) (K. Setia et.al, "Superfast encodings for fermionic quantum simulation", Phys. Rev. Research, 1(3):033033, 2019), or Majorana Loop Stabilizer Encodings (MLSE), (Z. Jiang et.al,
25 "Majorana Loop Stabilizer Codes for Error Mitigation in Fermionic Quantum Simulations", Phys. Rev. Appl, 12(6):064041, 2019). These mappings have been shown to not only result in low operator weights and hence low gate counts and circuit depths for the encoding, but also have useful error correcting properties. More specifically, the addition of qubits exceeding the number of fermionic mode operators to the system enlarges the Hilbert space, in a subspace
30 of which a solution then has to be stabilized. This procedure has many similarities to quantum error correcting codes and indeed both can be put on equal footing in the sense that both have stabilizers and logical qubits. Being able to identify and possibly correct errors which occur during the simulation of fermionic systems is a promising feature of such mappings as such approaches might be able to bridge the gap between the NISQ and fault-tolerant eras. The
35 stabilizers, which may be naturally defined for such local fermionic-to-qubit mappings are generally geometrically local and have typical weights (number of qubits they act on) of 6-12. In general, the weights increase as the error correcting properties of such mappings improve. Whilst one can, in principle use tunable couplers to provide the necessary connectivity to

implement the low weight ones of these stabilizers, the efficient implementation of the higher weight ones of these stabilizers already requires the use of resonators/transmission lines to provide the necessary connectivity. Alternatively, one may use a series of SWAP operators in the implementation of the stabilizer operators, which, however, may introduce additional errors and increase the circuit depth.

Despite the importance of local fermion-to-qubit mappings, there have been no previous attempts at designing specific co-design superconducting hardware for the implementation of error-correcting local fermion-to-qubit mappings. Whilst such mappings have appeared in a number of prior art scientific publications as the ones cited above, it is always assumed that the hardware connectivity will allow for the measurements of all of the stabilizers as well as the direct implementation of all operators from a to-be-simulated fermionic Hamiltonian.

Due to these problems in the prior art, it is therefore an object of the present invention to provide a quantum chip which allows for an efficient implementation of a local fermion-to-qubit mapping, to a method of manufacturing such a chip, to a method for simulating a fermionic system on the quantum chip and to a method for performing quantum error detection and/or correction using said quantum chip.

According to a first aspect of the present invention, a quantum chip of qubits is provided comprising a number of at least two superimposed layers, wherein a plurality of unit cells is located at vertices of a lattice, said lattice comprising said vertices, a plurality of edges connecting neighboring vertices and a plurality of plaquettes, each plaquette being surrounded by a plurality of vertices, wherein each unit cell comprises a plurality of data qubits having connectivity between themselves, wherein each pair of neighboring unit cells at vertices connected by an edge has connectivity between at least one data qubit of one unit cell of the pair and at least one data qubit of another unit cell of the pair, said quantum chip further comprising for at least one plaquette at least one syndrome qubit, wherein there is connectivity between said at least one syndrome qubit and at least one data qubit of the unit cells at the vertices surrounding said plaquette, wherein the connectivity of the quantum chip is distributed over at least two layers and the data and syndrome qubits are located on at least one of the layers.

Connectivity between qubits is in particular provided by coupling structures which may include tunable couplers and/or (waveguide) resonators or other signal-conducting transmission lines and which may extend along a path between the qubits between which they provide connectivity.

In one example, the chip has only two layers, e.g., first and second layers. In another example, the chip comprises more than two layers, e.g. three, four or five layers.

5 In one example, the chip may comprise at least three layers, and each layer may comprise only qubits or only connectivities. E.g., all qubits may be arranged on a (first) layer, and the connectivities may be distributed over two other layers (second and third layer). In a further example, the chip may comprise at least two layers, and at least one layer may comprise at least some of the qubits and some of the connectivities. In one example, there may be layers without qubits and only with connectivities. In a further example, the chip may
10 comprise two layers (first and second layers), and the qubits and the connectivities may be distributed over the two layers. In one example, the qubits may be located only on the first layer, and the connectivities may be distributed over the two layers.

The quantum chip according to the first aspect of the present invention may provide the
15 necessary connectivity for the implementation of a local fermion-to-qubit mapping, in particular, for a direct implementation of all operators of a fermionic Hamiltonian, for state preparation and for implementing all measurements of stabilizers defined by said fermion-to-qubit mapping and allow for error detection and/or correction of a fermionic simulation.

20 To be more explicit, let's consider a system of m spinless fermionic modes (the spinful case is analogous). The definition of local fermion-to-qubit mappings, such as the BKSF encoding and variants thereof such as the GSE and MLSE are based on a graph $G(E, V)$ e.g., a lattice, comprising a set V of m vertices v_i and a set E of edges e_{ij} connecting pairs of neighboring vertices v_i and v_j of said lattice. The degree d_i of a vertex v_i is the number of edges
25 e_{ij} connected with said vertex v_i . With reference to said lattice, a set of edge operators $A_{j,k}$, each edge operator $A_{j,k}$ being associated with an edge $e_{j,k}$, and a set of vertex operators B_j , each vertex operator B_j being associated with a vertex v_j is defined. Each edge operator $A_{j,k}$ is a quadratic form of the fermionic mode operators (creation and annihilation operators or Majorana operators associated with a fermionic mode) of the fermionic modes at the
30 neighboring vertices v_j and v_k connected by the edge $e_{j,k}$. The vertex operator B_j is a quadratic form of the fermionic mode operators at the vertex B_j . The edge and vertex operators fulfill special commutation relations. This is explained in more detail in e.g. T. Hagge et.al "Error mitigation via error-detection using Generalized Superfast Encodings", arxiv:2309.11673v1, Section 2".

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For second-quantized Hamiltonians relevant to quantum computing applications, the Hamiltonian H is commonly represented using the fermionic operator algebra generated by

creation and annihilation operators $a_j^\dagger$ and a_j , respectively, indexed over m fermionic modes $j \in 1, \dots, m$. The creation and annihilation operators have the following anti-commutation relations:

$$5 \quad a_j a_k^\dagger + a_k^\dagger a_j = \delta_{j,k}, \quad a_j a_k + a_k a_j = 0, \quad a_j^\dagger a_k^\dagger + a_k^\dagger a_j^\dagger = 0.$$

The edge and vertex operators are usually defined in terms of the Majorana operators c_{2j} and c_{2j+1} , for $j \in 1, \dots, m$, which are as follows:

$$10 \quad c_{2j} := a_j + a_j^\dagger, \quad c_{2j+1} := (-i)(a_j - a_j^\dagger),$$

and which fulfill $c_j c_k + c_k c_j = 2\delta_{j,k}$.

The edge and vertex operators are then:

$$15 \quad B_j = -ic_{2j}c_{2j+1} = I - 2a_j^\dagger a_j, \quad A_{j,k} = -ic_{2j}c_{2k} = -i(a_j + a_j^\dagger)(a_k + a_k^\dagger).$$

For all edges $e_{j,k}$ in the graph G , the edge and vertex operators $A_{j,k}$, B_j , and B_k satisfy the following:

$$20 \quad \begin{aligned} A_{j,k}^\dagger &= A_{j,k}, \\ B_j^\dagger &= B_j, \\ A_{j,k}^2 &= B_j^2 = 1, \\ B_j B_k &= B_k B_j, \\ 25 \quad A_{j,k} &= -A_{k,j}, \\ A_{j,k} A_{k,l} &= -A_{k,l} A_{j,k}, \text{ if } j \neq l, \\ A_{j,k} A_{l,m} &= A_{l,m} A_{j,k} \text{ if } j, k, l, m \text{ are distinct,} \\ A_{j,k} B_j &= -B_j A_{j,k}, \\ A_{j,k} B_l &= B_l A_{j,k} \text{ if } j, k, l \text{ are distinct,} \end{aligned}$$

$$30 \quad \tilde{A}(\zeta) = i^n \prod_{j=0}^{n-1} A_{k_j, k_{(j+1) \bmod n}} = 1, \text{ for each closed loop } \zeta \text{ with ordered vertices } (k_0, \dots, k_{n-1}) \text{ in } G.$$

Then, $n_i \geq 2$ qubits are assigned to each vertex v_i and a number p_i of mutually anti-commuting Pauli operators $\gamma_{i,1} \dots \gamma_{i,p_i}$ with support on the qubits is defined at each vertex v_i

assigning one to each half-edge incident on v_i . In one example, $d_i/2$ qubits are assigned to each vertex with degree d_i , and $p_i = d_i$. The edge and vertex operators $A_{j,k}$, B_j are expressed in terms of these Pauli operators in a way so that the special commutation relations of the vertex and edge operators are fulfilled. For example, as explained in T. Hagge *et. al* cited above to

5 define the edge and vertex operators, for each edge $e_{j,k}$ choose an orientation $\epsilon_{j,k} \in \pm 1$, $\epsilon_{j,k} = -\epsilon_{k,j}$. Then define

$$A_{j,k} = \epsilon_{j,k} \gamma_{j,m_{j,k}} \gamma_{k,n_{j,k}}$$

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$$B_j = (-i)^{\frac{d_j}{2}} \prod_{m=1}^{d_j} \gamma_{j,m}$$

where $\gamma_{j,m_{j,k}}$ and $\gamma_{k,n_{j,k}}$ are the half-edge operators corresponding to edge $e_{j,k}$.

The operators $\gamma_{v,i}$ are called generalized Majorana operators. The anti-commutation

15 relations of generalized Majorana operators are leveraged to construct representations of $A_{j,k}$ and B_j with correct commutativity properties. The operators are "generalized" in the sense of having similar formal properties; there is no mapping or correspondence between the individual Majorana operators used to construct $A_{j,k}$ and B_j and the generalized operators $\gamma_{v,i}$.

20 To make the link to the quantum chip according to the first aspect of the present invention, the data qubits of the unit cell of the quantum chip may be arranged at a vertex v_i of the lattice such that they correspond to the set of n_i qubits assigned to the vertex v_i . The connectivity between the data qubits of a unit cell is preferably such that all vertex operators B_j on each vertex v_i may be directly implemented. As each vertex operator B_j acts on a subset of data

25 qubits in said unit cell (the subset may include all data qubits of said unit cell), the connectivity is in particular such that for each vertex operator B_j there is connectivity at least between the data qubits of the unit cell which are in the support of said vertex operator B_j . In one example, the connectivity between data qubits in the unit cell is only between those data qubits which are in the support of the vertex operator B_j defined at the unit cell at the vertex v_i .

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Each edge operator acts on qubits in neighboring unit cells of the lattice. In one example, connectivity between the data qubits in the neighboring unit cells is such that for each edge operator $A_{j,k}$ defined on data qubits in the neighboring unit cells at vertices connected by an edge there is connectivity at least between the data qubits in the support of said edge operator

35 $A_{j,k}$. In one example, the connectivity between the data qubits in neighboring unit cells is only

between those data qubits which are in the support of the edge operators defined on the data qubits in the neighboring unit cells.

5 A lattice comprising vertices defines edges between vertices (also called neighboring vertices of the lattice) and a plurality of plaquettes. The plaquettes may be defined by the shortest nontrivial closed loops along edges and vertices of the lattice. E.g., a square lattice has plaquettes which are squares, a triangular lattice has plaquettes which are triangles and a honeycomb lattice has plaquettes which are hexagons. The vertices on the closed loop may be denoted as the vertices which surround the plaquette. Thus, for each vertex v_i of the lattice
10 there are q_i plaquettes, and at each plaquette, there is a plurality of unit cells associated with the vertices surrounding the plaquette. For each plaquette, a plaquette operator may be defined as the product of the edge operators acting on the data qubits in the unit cells at the vertices surrounding the plaquette. By measuring the plaquette operators for all plaquettes, error detection and, in some cases even error correction, may be achieved, see, e.g. T. Hagge et.al, arxiv2309.11673v1 cited above. The measurement of the plaquette operators may be
15 efficiently implemented by associating to each plaquette operator at least one syndrome qubit and by performing a sequence of quantum gates including two-qubit gates between the syndrome qubits and the data qubits of each of said unit cells at the vertices surrounding said plaquette which are in the support of said plaquette operator. Thus, for each plaquette of the
20 quantum chip, there is in particular connectivity between the at least one syndrome qubit associated with the plaquette and the data qubits in the subsets of data qubits of each of said unit cells at the vertices surrounding said plaquette which are in the support of the respective plaquette operator. In one example, the connectivity between the at least one syndrome qubit at each plaquette and the data qubits in the unit cells at the vertices surrounding said plaquette
25 is only between those data qubits which are in the support of the stabilizer operator defined at said plaquette and said at least one syndrome qubit. In one example, there is at least one syndrome qubit arranged at each plaquette. In a further example, there is one syndrome qubit arranged at each plaquette.

30 In one example, there is for each plaquette connectivity between the at least one syndrome qubit and at least one data qubit in each unit cell at the vertices surrounding the plaquette.

35 In one example, the quantum chip has only the connectivity between data qubits of the unit cells, data qubits in neighboring unit cells and data qubits at the vertices surrounding the plaquettes and the respective syndrome qubits at the plaquettes mentioned above and no further connectivity.

In general, the connectivity graph of a local fermion-to-qubit mapping as defined above is not planar which results in unavoidable crossings of coupling structures when these are located on a single layer. Therefore, the quantum chip according to the present invention comprises at least two superimposed layers so that when the coupling structures are distributed over at least two of the superimposed layers there are no crossings between any coupling structures located on the same layer. In many useful examples, the connectivity graph is bi-planar. In this case, the quantum chip may comprise only the first and second layers, and this layer structure may be sufficient to provide the connectivity for implementing said local fermion-to-qubit mapping without crossings between any coupling structures in the same layer by appropriately distributing the respective coupling structures over the two layers of the chip.

In one embodiment, at least two of the layers may be superimposed according to a flip-chip architecture. This is a particular useful embodiment when the quantum chip comprises only two layers, but it is not limited to this. In an alternative embodiment, there may be a connection between the elements (qubits and coupling structures) on the different layers through vias, in particular through silicon vias (TSV). Alternatively, Indium bumps may be used to provide connections between different layers as it is disclosed, e.g., in M. Fields et.al, "Modular Superconducting Qubit Architecture with a Multi-Chip Tunable Coupler", arxiv.2308.09240v1.

The lattice may be a periodic lattice in one example. In one example, the lattice may be non-periodic. In one example, the lattice is a 2D lattice. Neighboring unit cells of the lattice are defined as those unit cells which are arranged at vertices which are connected by an edge according to the lattice. Lattices in more than 2D may be embedded in a 2D lattice structure.

Within one example of this disclosure "the unit cells are located at vertices of a lattice and located at least on one of the layers" may mean that in a planar view on the superimposed layers, there is a unit cell at each vertex of the lattice, and the qubits of the unit cell are located at least on one layer. In particular, all qubits of one unit cell may be located on the same layer. However, the qubits of one unit cell may also be distributed over the layers in one example.

In one embodiment of the present invention, all data and syndrome qubits of the chip may be located on the same layer. This arrangement is advantageous as the arrangement of a qubit at a layer is space-consuming, for example due to control electronics required for operating the qubit. When all data and syndrome qubits of the chip are located on the first layer, the qubits may be arranged in a space-saving layout.

In principle, the number of data qubits in the different unit cells may be different from each other. However, in one embodiment all unit cells comprise the same number of data qubits. Such a quantum chip may be particularly suitable for implementing the BKSF encoding, the GSE encoding or the MLSE encoding. In one embodiment, the number of data qubits in each unit cell is 6. In another example, the number of data qubits in each unit cell is 5. In yet another example, the number of data qubits in each unit cell is 4. In still another embodiment, the number of data qubits in each unit cell is 3. In yet another embodiment, the number of data qubits in each unit cell is 2.

In one embodiment, the quantum chip comprises for at least one unit cell of the plurality a first unit cell coupling structure for providing connectivity between data qubits of said same unit cell, said first unit cell coupling structure being located on one of the layers. In one example, the data qubits of the unit cell are located on at one of the layers, and the first unit cell coupling structure is located on the same layer as the data qubits. In one example, the connectivity between the data qubits of the same unit cell may be provided only by the unit cell coupling structure associated with said unit cell. This example is particularly suitable when the connectivity graph of the data qubits in the unit cell is planar. In one example, the first unit cell coupling structure may comprise a plurality of parts, e.g., a (waveguide) resonator or other signal-conducting transmission line and a plurality of tunable couplers for connecting the data qubits to said waveguide resonator/transmission line. The first unit cell coupling structure may comprise a plurality of individual first unit cell coupling structures each providing connectivity between a subset of data qubits, e.g., a pair of data qubits. In this case, connectivity between the data qubits may be provided by tunable couplers which are the individual unit cell coupling structures and which are connecting pairs of data qubits in one example.

In one example, each unit cell may comprise the same number of data qubits and the connectivity between the data qubits in each unit cell may be the same. However, the invention is not limited to this.

In one embodiment, the quantum chip may comprise for each unit cell a corresponding first unit cell coupling structure for providing connectivity between the data qubits of said unit cell, said first unit cell coupling structures being located on the same layer. In one example, all data qubits are located on the same layer, and all first unit cell coupling structures are located on the same layer as the data qubits.

In an alternative example, the first unit cell coupling structure comprises first and second parts, the first part being located on one of the layers and the second part being located on another one of the layers. For example, the first part may comprise a (waveguide) resonator

and at least one tunable coupler for connecting a data qubit and the (waveguide) resonator/transmission line, and the second part may comprise at least one tunable coupler for connecting another qubit and the (waveguide) resonator/transmission line. The first part may be located on the first layer and the second part may be located on the second layer.

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In one embodiment, the quantum chip may further comprise, for the at least one unit cell a second unit cell coupling structure for providing connectivity between the data qubits of said same unit cell, wherein the second unit cell coupling structure is located on another layer of the at least two layers than the first unit cell coupling structure. Such a layout is preferable, when the connectivity graph of the qubits in the unit cell is no longer planar, e.g. bi-planar, as crossings between the first and second unit cell coupling structures on individual layers may be prevented in this way. In one example, the second unit cell coupling structure may comprise a plurality of individual second unit cell coupling structures each providing connectivity between a subset of data qubits, e.g., a pair of data qubits. In one example, the individual second unit cell coupling structures may comprise each a tunable coupler for providing connectivity between a subset of data qubits of the unit cell, e.g. between a pair of data qubits. In one embodiment, the quantum chip comprises for each unit cell at least one second unit cell coupling structure. In one example, the connectivity between the data qubits in the same unit cell may be provided only by the first and second unit cell coupling structures. In one embodiment, where each unit cell comprises the same number of data qubits and the same connectivity, the arrangement of the first and second unit cell coupling structures may be the same for each unit cell.

In one embodiment, the quantum chip is such that for at least one unit cell the data qubits of said unit cell have all-to-all connectivity. In one example, the quantum chip is such that for all unit cells the data qubits of each unit cell have all-to-all connectivity. If the data qubits are superconducting qubits, all-to-all connectivity may for example be provided by use of a (waveguide) resonator or other signal-conducting transmission line and a plurality of tunable couplers. Each data qubit of one unit cell may be connectable to the respective (waveguide) resonator/transmission line of said unit cell by a tunable coupler. Then, the unit cell coupling structure comprises the waveguide resonator/transmission line and the plurality of tunable couplers. In another example, all-to-all connectivity may be provided by providing for each pair of data qubits of the unit cell a tunable coupler providing connectivity between the data qubits of the pair.

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In one embodiment, the quantum chip may further comprise for at least one pair of neighboring unit cells at vertices connected by an edge a neighbor coupling structure for providing connectivity between the at least one data qubit of the one unit cell of the pair and

the at least one data qubit of the other unit cell of the pair, said neighbor coupling structure being located on one of the layers. In one example, the quantum chip may comprise for each pair of neighboring unit cells a respective neighbor coupling structure. In this example, all neighbor coupling structures may be located on the same layer. In a further example, all data
5 qubits of the unit cells and all neighbor coupling structures may be located on the same layer of the chip. Such a layout is particularly suitable when the connectivity graph between the neighboring unit cells is planar, as it is the case for many useful local fermion-to-qubit mappings. In one example, said neighbor coupling structure may comprise a tunable coupler which is connectable to the one data qubit of the one unit cell and the one data qubit of the
10 other unit cell. In one example, the tunable coupler may be a long-range tunable coupler as it is disclosed, e.g., in F. Marxer et.al "Long-distance transmon coupler with gate fidelity above 99.8 %, arxiv:2208.09460.

In a further example, there may be a connectivity between a plurality of data qubits of
15 the one unit cell and one or a plurality of data qubits of the other unit cell. The neighbor coupling structure may be configured to provide this connectivity. In another example, the neighbor coupling structure may comprise a plurality of individual neighbor coupling structures, each providing connectivity between a subset of data qubits, e.g., a pair of data qubits in two neighboring unit cells. In one example, each individual neighbor coupling structure may
20 comprise a tunable coupler for providing connectivity between a pair of data qubits. In one example, there may be connectivity between one data qubit of the one unit cell and more than one data qubit of the other unit cell. In a further example, different neighbor coupling structures may be located on different layers of the chip. In yet another example, at least one neighbor coupling structure may comprise first and second parts, whereas the first and second parts are
25 located on different layers of the chip. In one example, the first part may be located on the first layer, and the second part may be located on the second layer.

In a further embodiment of the present invention the quantum chip may be such that, for at least one plaquette, the data qubits of the unit cells at the vertices surrounding said plaquette
30 and the at least one syndrome qubit associated with said plaquette are located on the same layer and said at least one syndrome qubit is arranged between the unit cells at the vertices surrounding said plaquette. In particular, the data qubits of all unit cells at the vertices surrounding the plaquette may be located on the first layer and the at least one syndrome qubit may be located on the same layer as the data qubits of the unit cells at the vertices surrounding
35 the plaquette. With such an arrangement the space required for the arrangement of the data and syndrome qubits on the chip may be further reduced.

In a further embodiment, the quantum chip may comprise for at least one plaquette a plaquette coupling structure for providing connectivity between data qubits of the subset of data qubits of each unit cell at vertices surrounding the plaquette and the at least one syndrome qubit associated with said plaquette. In one example, all data qubits of the unit cells and all
5 syndrome qubits may be arranged at the same layer, and the plaquette coupling structure may be arranged at least partially at the same layer as the qubits.

In general, the connectivity graph between the data qubits of the subset of data qubits of each unit cell at vertices surrounding the plaquette and the at least one syndrome qubit
10 associated with said plaquette is not planar. In some examples, the connectivity graph may be bi-planar. Thus, according to another embodiment of the present invention, said plaquette coupling structure comprises a first part, which is located on one of the layers and a second part which is located on another layer. In particular, the first part is located on the first layer and the second part is located on the second layer in one example. In particular, the first part
15 may be without crossings on the one layer and the second part may be without crossings on the other layer. In this way, the connectivity between the data and syndrome qubits may be provided without any crossings of coupling structures in individual planes. In one example, the first part may comprise a (waveguide) resonator or other signal-conducting transmission line and at least one tunable coupler for connecting the waveguide resonator and at least one qubit,
20 and the second part may comprise at least one tunable coupler for connecting another qubit and the (waveguide) resonator/transmission line.

In another example, the plaquette coupling structure may comprise a first plaquette coupling structure located on one of the layers and providing connectivity between some of the
25 data qubits of the subset and the at least one syndrome qubit, and a second plaquette coupling structure located on another layer or other layers and providing connectivity between the remaining data qubits of the subset (which are not connected with the syndrome qubit by the first plaquette coupling structure) and the at least one syndrome qubit. For example, each of the first and second plaquette coupling structures may comprise a plurality of tunable couplers,
30 each providing connectivity between one data qubit of the subset and the at least one syndrome qubit.

In another embodiment, the subset of data qubits of each unit cell consists of all data qubits in each unit cell at the vertices surrounding the plaquette. That is, there is connectivity
35 between the at least one syndrome qubit associated with the plaquette and all data qubits in each unit cell at the vertices surrounding the plaquette. In this case, the connectivity graph is in general not planar, and it is thus preferable that the quantum chip comprises the plaquette coupling structure with the first and second parts or the first and second plaquette coupling

structures arranged at the different layers as explained above in order to avoid crossings between the two parts of the coupling structure or the two coupling structures in individual layers which would be present if the two parts or two coupling structures were located on the same layer.

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In a further embodiment, the quantum chip is such that there is for at least one plaquette all-to-all connectivity between the data qubits of the subset of qubits of each unit cell at the vertices surrounding the plaquette and the at least one syndrome qubit associated with said plaquette. If the qubits are superconducting qubits, all-to-all connectivity may for example be provided by use of a (waveguide) resonator or transmission line and tunable couplers for connecting the qubits and the (waveguide) resonator/transmission line.

Within the invention, the lattice structure is not limited to a special case. However, in an embodiment of the invention, said lattice may be a square lattice, a triangular lattice or a honeycomb lattice. In particular, the lattice may be a periodic lattice. Even more particular, the lattice may be a 2D lattice. Such arrangements are advantageous with regard to manufacturing and also are useful for the implementation of many useful local fermion-to-qubit mappings.

In one embodiment of the present invention, all data qubits and all syndrome qubits may be located on the first layer, the quantum chip may comprise for each unit cell a first unit cell coupling structure located on the first layer and being configured for providing connectivity between data qubits of said unit cell, for each pair of neighboring unit cells a respective neighbor coupling structure located on the first layer and being configured for providing the connectivity between the at least one data qubit of the one unit cell of the pair and the at least one data qubit of said other unit cell of the pair, and for each plaquette a plaquette coupling structure with a first part located on the first layer and a second part located on a second layer, said plaquette coupling structures being configured for providing connectivity between the data qubits of the subset of data qubits of each unit cell at the vertices surrounding the plaquette and the at least one syndrome qubit. In one example, the quantum chip may comprise no further coupling structures for providing the connectivity between the qubits. In another embodiment, the quantum chip may comprise for at least one unit cell, and in particular for each unit cell, a second unit cell coupling structure located on the second layer, so that the first unit cell coupling structure and the second unit cell coupling structure together provide all connectivity between the data qubits of the unit cell. Alternatively, the first unit cell coupling structures may comprise first and second parts distributed over the two layers without crossings on individual layers as explained above.

In principle, the qubits of the quantum chip are not limited to a certain type as long as the qubits may be located on a layer of a chip. In one embodiment, said qubits may be superconducting qubits, and in particular transmons or fluxoniums or unimonos.

5 In a further embodiment, the unit cell coupling structure and/or the neighbor coupling structure and/or the plaquette coupling structure may comprise a (waveguide) resonator or transmission line and/or a tunable coupler. In one example, all coupling structures comprise a (waveguide) resonator or transmission line and/or tunable coupler. In one embodiment, the neighbor coupling structure may comprise a tunable coupler and the plaquette coupling
10 structure may comprise a (waveguide) resonator or transmission line and a plurality of tunable couplers, each being configured for connecting one qubit and said (waveguide) resonator/transmission line. In one example, the unit cell coupling structures may not comprise a waveguide resonator or transmission line but only tunable couplers. In another example, the unit cell coupling structure(s) may comprise a waveguide resonator/transmission line and a
15 plurality of tunable couplers each being configured for connecting one qubit and said waveguide resonator/ transmission line. The tunable couplers may be standard tunable couplers or long-range tunable couplers as disclosed, e.g. in F. Marxer et.al "Long-distance transmon coupler with CZ gate fidelity above 99.8 %", arxiv: 2208. 09460.

20 In a further embodiment, a connectivity graph of the quantum chip may be bi-planar and the coupling structures may be located on the first and second layers without crossings in individual layers. In particular, the arrangement of the coupling structures may be according to the connectivity graph. In a further embodiment where the connectivity graph is no longer bi-planar, connectivity between the qubits and/or the qubits and the resonators/transmission lines
25 may be provided by use of tunable couplers which switch between the first and second layers a plurality of times using Indium bumps, as was recently disclosed in M. Fields et.al "Modular Superconducting Qubit Architecture with a Multi-chip Tunable Coupler", arxiv.2308.09240v1 to thereby avoid crossings between the coupling structures at one of the layers. Alternatively, the chip may comprise more than two layers so that the coupling structures may be located on the
30 layers without crossings in individual layers.

According to a second aspect of the present invention, a method of manufacturing a quantum chip for an implementation of an encoding according to a local fermion-to-qubit mapping for m fermionic modes is provided, wherein said mapping is defined by associating
35 the m fermionic modes to m vertices v_i of a lattice having edges connecting neighboring vertices v_i, v_j and a plurality of plaquettes, each plaquette being surrounded by a plurality of vertices, by associating to each vertex v_i a plurality of data qubits and a plurality of mutually anticommuting Pauli operators with support on the data qubits at said vertex, by defining for

the vertices v_i and edges $e_{i,j}$ of the lattice a plurality of vertex and edge operators $B_i, A_{i,j}$ which are expressed in terms of fermionic operators associated with the mode at said vertex v_i or modes at the vertices connected by a respective edge $e_{i,j}$, and by expressing said edge and vertex operators $B_i, A_{i,j}$ in terms of said Pauli operators. The method comprises providing first and second layers of the quantum chip, wherein m unit cells are arranged at the m vertices of said lattice and located at least on one of the layers, wherein each unit cell comprises the plurality of data qubits associated with said vertex, wherein for each vertex v_i the data qubits in the support of the associated vertex operator have connectivity between themselves, wherein for each pair of neighboring unit cells at neighboring vertices v_i, v_j , the qubits in the support of the edge operator $A_{i,j}$ associated with the edge $e_{i,j}$ connecting said vertices v_i, v_j have connectivity between themselves, wherein said layers further comprise for each plaquette of said lattice at least one syndrome qubit located on one of the layers, wherein the at least one syndrome qubit and the data qubits of the unit cells at vertices surrounding the plaquette and which are in the support of the edge operators at the edges of the plaquette have connectivity between themselves, wherein the connectivity of the qubits is distributed over the two layers; superimposing the first and second layers to thereby manufacture the quantum chip. In particular, the two layers are superimposed according to a flip-chip architecture.

In one example, the connectivity of the quantum chip provides all the connectivity according to the connectivity graph of the local fermion-to-qubit mapping. In one example, the connectivity of the quantum chip is identical to the connectivity according to the connectivity graph of the local fermion-to-qubit mapping. This provides for a chip which has the minimum connectivity for implementing the fermion-to-qubit mapping and is very efficient to manufacture.

Everything which was said above in relation to the quantum chip according to the first aspect of the invention also applies to the method according to the second aspect of the present invention.

The invention also relates to a quantum chip manufactured according to the method according to the second aspect of the present invention.

According to a third aspect of the present invention, a method is provided for simulating a fermionic system on a quantum chip according to any one of the above or manufactured according to the method above, wherein said method comprises implementing a fermionic operator encoded according to the local fermion-to-qubit mapping by use of the connectivity between the qubits. In particular, the implementation may be only by use of connectivity and

without the use of SWAP operators in one example. The method according to the third aspect of the present invention is highly efficient for the purpose of simulating fermionic systems on a quantum chip.

5 According to a fourth aspect of the present invention, there is provided a method for performing quantum error detection and/or correction on a quantum chip according to anyone of the above or manufactured according to the method above wherein said method comprises implementing at least one plaquette operator according to the local fermion-to-qubit mapping by use of the connectivity between the qubits. As explained above, local fermion-to-qubit
10 mappings are closely related to quantum error correction codes. In particular, by measuring the plaquette operators defined for a plaquette, quantum errors may be detected and even corrected in certain examples. As the quantum chip according to any one of the above or manufactured according to the method above may provide the necessary connectivities for implementing the stabilizer operators of the quantum error correction code, the method
15 according to the fourth aspect of the present invention is a highly efficient method for performing error correction. In particular, quantum error detection and/or correction may be implemented without the use of SWAP operators.

20 In the following, the invention will be described in greater detail by way of example with reference to the drawings in which:

Figure 1a is a schematic representation of a first embodiment of a quantum chip according to the present invention,
Figure 1b is a schematic representation of the first layer of an alternative quantum chip
25 similar to the one of the first embodiment for a lattice with more vertices,
Figure 2 is a schematic representation of a second embodiment of a quantum chip according to the present invention,
Figure 3a is a schematic representation of an arrangement of the second part of the plaquette coupling structures at the second layer for providing connectivity
30 between data qubits of one unit cell and waveguide resonators/syndrome qubits of the quantum chip of the second embodiment shown in Figure 2,
Figure 3b is a schematic representation of an arrangement of the second part of the plaquette coupling structures at the second layer for providing connectivity
between a waveguide resonator/a syndrome qubit and the data qubits of the
35 unit cells at the plaquette corresponding to said syndrome qubit for the quantum chip of the second embodiment shown in Figure 2,
Figure 4 is a schematic representation of a third embodiment of a quantum chip according to the present invention,

Figure 5 is a schematic representation of a fourth embodiment of a quantum chip according to the present invention,

Figure 6 is a schematic representation of a fifth embodiment of a quantum chip according to the present invention.

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The quantum chips schematically represented in the following figures each comprise nine unit cells of data qubits for the purpose of illustration. However, the quantum chips are not limited to nine unit cells and may comprise more unit cells which are arranged and have connectivity according to the lattice structures of the figures.

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Figure 1a is a schematic representation of a first embodiment of a quantum chip 101 according to the present invention. The quantum chip 101 comprises two layers (first and second layer) which are superimposed, in particular according to a flip-chip architecture. For the illustration, elements at the first layer are represented by solid lines or symbols, and elements at the second layer are represented by dashed lines.

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The quantum chip 101 comprises nine unit cells 1, 2, ..., 9 which are arranged at the vertices of a square lattice and located on the first layer of the chip 101. The lattice comprises the vertices and defines a plurality of edges connecting neighboring vertices and a plurality of plaquettes, each plaquette being surrounded by a plurality of vertices. The configuration of each unit cell 1, 2, 3, ..., 9 is a square configuration, as opposed to hex or triangular configurations. Each unit cell 1, 2, 3, ..., 9 comprises two data qubits 1a, 1b; 2a, 2b; ...; 9a, 9b. The data qubits are superconducting qubits, for example transmons, fluxoniums or unimon. For each unit cell 1, 2, ..., 9 a unit cell coupling structure U provides connectivity between each pair of data qubits 1a, 1b; 2a, 2b; ...; 9a, 9b in each unit cell 1, 2, ... 9. The unit cell coupling structure U may comprise a tunable coupler, for example a transmon qubit, a fluxonium or an unimon. The unit cell coupling structure U is located on the first layer.

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The quantum chip 101 further comprises a plurality of neighbor coupling structures N for providing connectivity between each pair of neighboring unit cells arranged at vertices connected by an edge, to be more precise, between one data qubit of one unit cell of the pair and another data qubit of another one of the unit cells of the pair (for example, between unit cell 1 and 4 the neighbor coupling structure N provides connectivity between the data qubit 1a and the data qubit 4b). The neighbor coupling structure N is located on the first layer. In one example, the neighbor coupling structure N comprises a tunable coupler, for example a tunable coupler comprising a transmon qubit.

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The quantum chip 101 further comprises for each plaquette 10, 20, 30, 40 of the lattice surrounded by four unit cells, a syndrome qubit 11, 21, 31, 41 which is located on the first layer and within said plaquette 10, 20, 30, 40. For each plaquette 10, 20, 30, 40 there is connectivity between all data qubits of the unit cells at said plaquette and the syndrome qubit 11, 21, 31, 41 associated with said plaquette 10, 20, 30, 40. For example, there is connectivity between the syndrome qubit 11 and the data qubits 1a, 1b, 2a, 2b, 4a, 4b, 5a, 5b of the unit cells 1, 2, 4, 5 at the plaquette 10. Connectivity is provided by a plaquette coupling structure comprising a first part P1a, P1b located on the first layer and a second part P2 located on the second layer. The first part P1a, P1b comprises a waveguide resonator or transmission line P1a and a plurality of tunable couplers P1b for connecting, for the example of the plaquette 10, the data qubits 1a, 1b, 2a, 4b, 5a, 5b with the waveguide resonator/transmission line P1a arranged at the plaquette 10. Furthermore, the waveguide resonator/transmission line P1a is connected, by a tunable coupler P1b, with the syndrome qubit 11. The second part of the plaquette coupling structure comprises two tunable couplers P2 (dashed lines) for connecting the data qubits which are not connected via the tunable couplers P1b of the first part of the plaquette coupling structure with the waveguide resonator/transmission line P1a (in the example above, for connecting data qubits 2b and 4a with waveguide resonator/transmission line P1a arranged at the plaquette 10). As it is obvious from Figure 1, there are no crossings between coupling structures, or any parts thereof located on the same layer of the quantum chip 101.

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As each syndrome qubit 11, 21, 31, 41 is connected with six data qubits of the unit cells, the connectivity may alternatively be provided by connecting the syndrome qubit with each of the six data qubits by one tunable coupler, wherein four of these tunable couplers are located on the first layer, and two of them, as indicated by dashed lines, are located on the second layer.

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The connectivity of the quantum chip 101 is sufficient to implement all vertex edge, and plaquette operators of the following fermion-to-qubit mapping:

Denote each vertex of the lattice by $v(x,y)$, wherein $x, y, =1, \dots, N$ are values for x - and y -coordinates of an $N \times N$ lattice. For the 3×3 lattice shown in Fig. 1, $v(x,y) = (x-1)*3 + y$ (for an $N \times N$ lattice: $v(x,y) = (x-1)*N + y$). Denote the two qubits in the unit cell at the vertex $v(x,y)$ by $q_{v(x,y),a}$ and $q_{v(x,y),b}$. Then, the edge and vertex operators with support at least on the vertex $v(x,y)$ are given by

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$$\begin{aligned} B_{v(x,y)} &= Z_{v(x,y),a} \otimes Z_{v(x,y),b} \\ A_{v(x,y),v(x+1,y)} &= Z_{v(x,y),a} \otimes X_{v(x,y),b} \otimes Y_{v(x+1,y),a} \\ A_{v(x,y),v(x,y+1)} &= Z_{v(x,y),a} \otimes Y_{v(x,y),b} \otimes X_{v(x,y+1),a} \end{aligned}$$

The stabilizers correspond to a code of distance 2, meaning that all one-qubit errors can be detected.

5 Figure 1b is a schematic representation of a part (indicated by a black square S) of the first layer of an alternative quantum chip 101' similar to the one of the first embodiment for a lattice with more vertices. Similar to the quantum chip 101, the quantum chip 101' comprises a plurality of unit cells, each comprising two data qubits (e.g. qubits 1a and 1b of the unit cell 1) and a syndrome qubit (e.g. syndrome qubit 11) arranged within a plaquette of the lattice.
10 (The qubits are located on the first layer). As for the quantum chip 101, the data qubits in each unit cell are connected by a unit cell coupling structure U, and the qubits in neighboring unit cells are connected by neighbor coupling structures N. However, different from the quantum chip 101, the quantum chip 101' comprises for each syndrome qubit six first plaquette coupling structures P1 (e.g., tunable couplers), located on the first layer, each providing connectivity
15 between a data qubit of one of the unit cells at the vertices surrounding the plaquette, and the syndrome qubit associated with said plaquette. The remaining two qubits in the unit cells at the vertices surrounding the plaquette are each connected with the syndrome qubit by a second plaquette coupling structure located on the second layer (not shown). The first layer continues to the right and downwards according to the pattern shown within the black square
20 S.

Figure 2 is a schematic representation of a second embodiment of a quantum chip 102 according to the present invention. The representation is similar to the representation of the first embodiment shown in Figure 1. As for the first embodiment, nine unit cells 1, ..., 9 are
25 arranged at the vertices of a square lattice and located on the first layer. Each unit cell comprises four data qubits 1a, 1b, 1c, 1d;; 9a, 9b, 9c, 9d. There is all-to-all connectivity between the four data qubits of each unit cell. Thereby, the connectivity graph of the data qubits in each unit cell is no longer planar but bi-planar. Each unit cell 1, ..., 9 comprises a first unit cell coupling structure U1 and a second unit cell coupling structure U2 for providing the all-to-
30 all connectivity between the data qubits in the respective unit cell. The first unit cell coupling structure U1 comprises five individual first unit cell coupling structures which are located on the first layer. Each of the five individual first unit cell coupling structures U1 provides connectivity between data qubits of a pair, namely of the pairs 1a, 1b; 1b, 1c; 1c, 1d; 1d, 1a; 1a, 1c, respectively. There is no crossing between these coupling structures. The second unit
35 cell coupling structure U2 is located on the second layer and provides connectivity between the data qubits 1b and 1d. As the connectivity between the data qubits of each unit cell is distributed among the two layers, there is no crossing between the coupling structures at the same layer. Each of the unit cell coupling structures U1, U2 may comprise a tunable coupler.

Such an embodiment may allow for a fast execution of quantum circuits for the implementation of the vertex, edge and plaquette operators.

Furthermore, the quantum chip 102 comprises a plurality of neighbor coupling structures N for providing connectivity between neighboring unit cells. To be more precise, the neighbor coupling structure N provides connectivity between one data qubit of one unit cell and another data qubit of another neighboring unit cell, for example between the data qubit 1d of the unit cell 1 and the data qubit 4b of the unit cell 4. The neighbor coupling structure N may comprise a tunable coupler.

Furthermore, the quantum chip 102 comprises, for each plaquette, a plaquette coupling structure P1a, P1b, P2 for providing all-to-all connectivity between all data qubits in the unit cells at the vertices surrounding said plaquette 10, 20, 30, 40 and the syndrome qubit 11, 21, 31, 41 associated with said plaquette 10, 20, 30, 40. For example, consider the plaquette 10. The plaquette coupling structure P1a, P1b, P2 provides connectivity between the syndrome qubit 11 and all data qubits in the unit cells 1, 2, 4 and 5.

The plaquette coupling structure comprises a first part P1a, P1b located on the first layer. The first part comprises a waveguide resonator/transmission line P1a arranged inside the plaquette 10, 20, 30, 40 and eight tunable couplers P1b for connecting the data qubits in the unit cells at the plaquette with the waveguide resonator/transmission line P1a. Furthermore, the first part also comprises a tunable coupler P1b for connecting the syndrome qubit associated with the plaquette and the waveguide resonator/transmission line P1a. The plaquette coupling structure further comprises a second part P2 which is located on the second layer. The second part P2 comprises eight tunable couplers for connecting the remaining data qubits in the unit cells at the vertices surrounding the plaquette and the waveguide resonator/transmission line P1b. For example, for the plaquette 10, data qubits 1a, 1b, 2b, 2c, 5c, 5d, 4a, 4d are connected by tunable couplers P2 located on the second layer with the waveguide resonator/transmission line P1a arranged at the plaquette 10.

The waveguide resonator/transmission line P1a connects 17 qubits which is still in the reach of present technology.

While Figure 2 suggests that the tunable couplers of the second part P2 located on the second layer might potentially cross in the second layer (see in particular unit cell 5), it is possible to arrange the tunable couplers of the second part P2 on the second layer in a way that avoids crossings. I.e., it is possible to provide connectivity by a bi-planar flip-chip without any crossings. Such an arrangement is shown in Figures 3a and 3b.

Figure 3a is a schematic representation of an arrangement of the second part of the plaquette coupling structures P2 for providing connectivity between data qubits of the unit cell 5 and waveguide resonators P1a/syndrome qubits 11, 21, 31, 41 at the four plaquettes 10, 20, 30, 40 at the vertices surrounding said unit cell 5 for the quantum chip 102 of the second embodiment shown in Figure 2. As has been explained above, the data qubits 5a, 5b, 5c, 5d of the unit cell 5 are located on the first layer. Similarly, the waveguide resonators P1a (here depicted as dots for simplicity), respectively the syndrome qubits 11, 21, 31, 41 are also located on the first layer. The eight tunable couplers P2 for connecting the data qubits 5a, 5b, 5c, 5d of the unit cell 5 with the respective waveguide resonators P1a/syndrome qubits 11, 21, 31, 41 are located on the second layer. By arranging the tunable couplers P2, in particular their extensions in the shape depicted in Figure 3a, crossings between the tunable couplers P2 may be prevented.

In general, one may show that for a square lattice the connectivity graph for the data qubits of the unit cells at the vertices surrounding the plaquette and the syndrome qubit is bi-planar as long as the number of data qubits in a unit cell is at most four. For a honeycomb lattice where three plaquette coupling structures are connected to a given unit cell, the connectivity graph is bi-planar as long as the number of data qubits in each unit cell is at most six. For a triangular lattice, this number is three.

Figure 3b is a schematic representation of an arrangement of the second part of the plaquette coupling structures P2 for providing the connectivity between the waveguide resonator/transmission line P1a/the syndrome qubit 11 arranged at the plaquette 10 and the data qubits of the unit cells 1, 2, 4, 5 arranged at the vertices surrounding the plaquette for the quantum chip 102 of the second embodiment shown in Figure 2. Again, the data qubits of the unit cells 1, 2, 4, 5 and the syndrome qubit 11, respectively the waveguide resonator/transmission line P1a connected with the syndrome qubit 11 are located on the first layer. The tunable couplers P2 for connecting the data qubits of the unit cells 1, 2, 4, 5 with the waveguide resonator/transmission line P1a at the first plaquette 10 are located on the second layer. It is obvious from Figure 3b that there are no crossings between the tunable couplers P2 located on the second layer.

Figure 4 is a schematic representation of a third embodiment of a quantum chip 103 according to the present invention. The quantum chip 103 shown in Figure 4 is similar to the quantum chip 102 shown in Figure 2. The only difference between the quantum chips 103 and 102 is the way how connectivity is provided between the data qubits in each unit cell 1, 2, ..., 9. Contrary to the quantum chip 102 shown in Figure 2, the quantum chip 103 does not

comprise the second unit cell coupling structure U2 located on the second layer. The quantum chip 103 comprises, similar to the quantum chip 102, the four first individual unit cell coupling structure U1 located on the first layer, and an additional first unit cell coupling structure U1a, U1b also located on the first layer. For the example of the unit cell 1, the first unit cell coupling structure comprises four tunable couplers U1 for providing connectivity between pairs of data qubits, namely between the data qubit pairs 1a 1b; 1b, 1c; 1c, 1d; and 1a, 1d. The additional first unit cell coupling structure comprises a waveguide resonator/transmission line U1a arranged within the unit cell 1 and four tunable couplers U1b for connecting the data qubits 1a, 1b, 1c, 1d and the waveguide resonator/transmission line U1a. In this way, the connectivity between data qubits of the same unit cell is completely provided by the first individual and additional unit cell coupling structures U1, U1a, U1b located on the first layer, and the second layer is only required for providing connectivity between some of the qubits of the unit cells and the plaquette coupling structures as was explained above for the quantum chip 102 according to the second embodiment.

Figure 5 is a schematic representation of a third embodiment of a quantum chip 104 according to the present invention. The representation is similar to Figures 1, 2, and 4. The quantum chip 104 comprises nine unit cells, 1, ... 9 arranged at the vertices of a square lattice and located on the first layer. Each of the nine unit cells comprises three data qubits 1a, 1b, 1c; 2a, 2b, 2c; ...; 9a, 9b, 9c. The data qubits within a unit cell have all-to-all connectivity. For the three data qubits in a unit cell, the connectivity graph is planar. Connectivity between the data qubits in a unit cell is provided by three individual coupling structures U forming the unit cell coupling structure, wherein each individual unit cell coupling structure U provides connectivity between two neighboring data qubits of a unit cell, e.g., between data qubit 1a and 1b, between data qubit 1b and 1c, and between data qubits 1c and 1a for the example of the first unit cell. All data qubits in the unit cells and all coupling structures U of the unit cells are located on the first layer.

Furthermore, the quantum chip 104 comprises for two neighboring unit cells in two neighboring columns of the lattice one individual neighbor coupling structure N for providing connectivity between one data qubit of one unit cell (for example, data qubit 1c of unit cell 1) and another data qubit of a neighboring unit cell (for example data qubit 2a of unit cell 2). Further, the quantum chip 104 comprises for each pair of neighboring unit cells in two neighboring rows two individual neighbor coupling structures N1a, N1b for providing connectivity between the two unit cells. To be more precise, one data qubit of one of the unit cells is connected to two different data qubits of the other unit cell of the pair by two individual neighbor coupling structures N1a, N1b (for example data qubit 4b in unit cell 4 is connected by neighbor coupling structure N1a with data qubit 1a, and data qubit 4b of unit cell 4 is also

connected to data qubit 1c in unit cell 1 by another neighbor coupling structure N1b). The neighbor coupling structures N, N1a and N1b may be the same type of coupling structures, or they may be different from each other. In one example, the neighbor coupling structure N may comprise a standard tunable coupler, and the neighbor coupling structures N1a, N1b may each
5 comprise a long-range tunable coupler.

The quantum chip 104 may further comprise for each plaquette 10, 20, 30, 40 a plaquette coupling structure for providing all-to-all connectivity between all data qubits in the unit cells at said plaquette 10, 20, 30, 40 and the syndrome qubit 11, 21, 31, 41 associated
10 with said plaquette 10, 20, 30, 40. For example, for the plaquette 10, there is connectivity between the syndrome qubit 11 and all data qubits in the unit cells 1, 2, 4, 5, that is the data qubits 1a, 1b, 1c; 2a, 2b, 2c; 4a, 4b, 4c; 5a, 5b, 5c. The plaquette coupling structure comprises a first part P1a, P1b located on the first layer. The first part comprises a waveguide resonator/
15 transmission line P1a and seven tunable couplers P1b for connecting the data qubits 1c, 2a, 5b, 5a, 4c, 4b and the syndrome qubit 11 with the waveguide resonator/transmission line P1a arranged at the plaquette 10. The second part P2 of the plaquette coupling structure is located on the second layer and comprises six tunable couplers for connecting the data qubits 1a, 1b,
20 2b, 2c, 5c, 4a with the waveguide resonator/transmission line P1a located on the first layer and at the plaquette. Obviously, the tunable couplers P2 on the second layer may be arranged such that there is no crossing between them. This may be understood with reference to Figures 3a and 3b, which is similar for the quantum chip 104 shown in Figure 5 if one removes the data
qubit 5d and the respective connections.

The quantum chip 104 of the third embodiment allows to directly implement all
25 operators of a fermion-to-qubit mapping which corresponds to an error correction code with distance 3. Quantum chips that allow to implement fermion-to-qubit mappings with larger distances may also be realized with and are within the scope of the present invention.

Figure 6 is a fourth embodiment of a quantum chip 105 according to the present
30 invention. The quantum chip 105 differs from the quantum chips 102 and 103 shown in Figures 2 and 4 in that there are six data qubits (e.g. data qubits 1a, 1b, 1c, 1d, 1e, 1f) per unit cell. While it is possible to provide all-to-all connectivity between the data qubits of each unit cell by use of the waveguide resonator/transmission line U1a connected to the data qubits in the unit
cell by tunable couplers U1b, it is not possible to establish all-to-all connectivity between all
35 data qubits of the unit cells arranged at one of the plaquettes 10, 20, 30, 40 and the respective syndrome qubit 11, 21, 31 or 41 by using a plaquette coupling structure distributed over the first and second layers, as the connectivity graph is no longer bi-planar. However, by designing a chip with tunable couplers which are switching between the two layers an arbitrary number

of times using Indium bumps, as was recently suggested in arxiv:2308.09240, an arbitrary connectivity graph may be established on the two layers as long as elements have a reasonable number of connections and the distances between connected elements are short enough. These restrictions will be satisfied by the layout shown in Figure 6, since elements
5 are clearly local and the maximum connectivity per qubit is 8, and the connectivity of waveguide resonators/transmission lines is 25 which is achievable by current state of the art waveguide resonators/transmission lines. Alternatively, the coupling structures providing the connectivity between the qubits may be distributed over more than two layers so that there are no crossings in any layer.

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PATENT CLAIMS

1. Quantum chip (101, 102, 103, 104) of qubits comprising a number of at least two
5 superimposed layers, characterized in that a plurality of unit cells (1-9) is located at vertices of
a lattice, said lattice comprising said vertices, and defining a plurality of edges connecting
neighboring vertices and a plurality of plaquettes, each plaquette being surrounded by a
plurality of vertices, wherein each unit cell (1-9) comprises a plurality of data qubits (1a, b, c,
d, e, f – 9a, b, c, d, e, f) having connectivity between themselves, wherein each pair of
10 neighboring unit cells (1-9) at vertices connected by an edge has connectivity between at least
one data qubit of one unit cell of the pair and at least one data qubit of another unit cell of the
pair, said quantum chip (101, 102, 103, 104) further comprising for at least one plaquette (10,
20, 30, 40) at least one syndrome qubit (11, 21, 31, 41), wherein there is connectivity between
said at least one syndrome qubit (11, 21, 31, 41) and at least one data qubit of the unit cells at
15 the vertices surrounding said plaquette (10, 20, 30, 40), wherein the connectivity of the
quantum chip (101, 102, 103, 104) is distributed over at least two of the layers, and the data
and syndrome qubits (1a, b, c, d, e, f – 9a, b, c, d, e, f; 11, 21, 31, 41) are located on at least
one of the layers.
2. Quantum chip (101, 102, 103, 104) according to claim 1, wherein at least two of the
20 layers are superimposed according to a flip-chip architecture.
3. Quantum chip (101, 102, 103, 104) according to claim 1 or 2, wherein all data and
syndrome qubits of the chip are located on the same layer.
- 25 4. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein all unit cells (1-9) comprise the same number of data qubits.
5. Quantum chip (101, 102, 103, 104) according to any one of the preceding claims, said
30 quantum chip (101, 102, 103, 104) comprising for at least one unit cell (1-9) of the plurality of
unit cells (1-9) a first unit cell coupling structure (U, U1, U1a, U1b) for providing connectivity
between data qubits of said same unit cell (1-9), said first unit cell coupling structure (U, U1,
U1a, U1b) being located on one of the layers.
- 35 6. Quantum chip (102) according to claim 5, said quantum chip (102) further comprising
for the at least one unit cell (1-9) a second unit cell coupling structure (U2) for providing
connectivity between the data qubits of said same unit cell (1-9), wherein the second unit cell

coupling structure (U2) is located on another layer than the first unit cell coupling structure (U1).

7. Quantum chip (101, 102, 103, 104) according to any one of the preceding claims,
5 wherein for at least one unit cell (1-9) the data qubits of said same unit cell have all-to-all connectivity.

8. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims, further
comprising for at least one pair of neighboring unit cells (1-9) at vertices connected by an edge
10 a neighbor coupling structure (N, N1, N2) for providing connectivity between the at least one
data qubit of the one unit cell of the pair and the at least one data qubit of the other unit cell of
the pair, said neighbor coupling structure (N, N1a, N1b) being located on one of the layers.

9. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
15 wherein for at least one plaquette (10, 20, 30, 40) the data qubits of the unit cells at the vertices
surrounding said plaquette (10, 20, 30, 40) and the at least one syndrome qubit (11, 21, 31,
41) associated with said plaquette (10, 20, 30, 40) are located on the same layer, and wherein
said at least one syndrome qubit (11, 21, 31, 41) is arranged between the unit cells (1-9) at the
vertices surrounding said plaquette (10, 20, 30, 40).

20 10. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims, said
quantum chip (101, 102, 103, 104) comprising for at least one plaquette (10, 20, 30, 40) a
plaquette coupling structure (P1a, P1b, P2) for providing connectivity between data qubits of
the subset of data qubits of each unit cell at the vertices surrounding the plaquette (10, 20, 30,
25 40) and the at least one syndrome qubit (11, 21, 31, 41) associated with said plaquette (10,
20, 30, 40).

11. Quantum chip (101, 102, 103, 104) according to claim 10, wherein said plaquette
coupling structure comprises a first part (P1a, P1b) which is located on one of the layers and
30 a second part (P2) which is located on another layer.

12. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein the subset of data qubits of each unit cell (1-9) consists of all data qubits in each unit
cell at the vertices surrounding the plaquette (10, 20, 30, 40).

35 13. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein for at least one plaquette (10, 20, 30, 40) there is all-to-all connectivity between the
data qubits of the subset of data qubits of each unit cell at the vertices surrounding the

plaquette (10, 20, 30, 40) and the at least one syndrome qubit (11, 21, 31, 41) associated with said plaquette (10, 20, 30, 40).

14. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
5 wherein said lattice is a square lattice, a triangular lattice, or a honeycomb lattice.

15. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein all data and syndrome qubits are located on a first layer, the quantum chip (101, 102,
103, 104) comprises for each unit cell (1-9) a unit cell coupling structure (U, U1, U1a, U1b)
10 located on the first layer and being configured for providing connectivity between data qubits
of said unit cell (1-9), for each pair of neighboring unit cells (1-9) at vertices connected by an
edge, a respective neighbor coupling structure (N, N1a, N1b) located on the first layer and
being configured for providing the connectivity between the at least one data qubit of the one
unit cell (1-9) of the pair and the at least one data qubit of said other unit cell (1-9) of the pair,
15 and for each plaquette (10, 20, 30, 40) a plaquette coupling structure (P1a, P1b, P2) with a
first part (P1a, P1b) located on the first layer and a second part (P2) located on a second layer,
said plaquette coupling structures (P1a, P1b, P2) being configured for providing connectivity
between the data qubits of the subset of data qubits of each unit cell (1-9) at the vertices
surrounding the plaquette (10, 20, 30, 40) and the syndrome qubit (11, 21, 31, 41) associated
20 with said plaquette (10, 20, 30, 40).

16. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein said data and syndrome qubits are superconducting qubits, and in particular
transmons or fluxoniums or unimonos.

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17. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein the unit cell coupling structure (U, U1, U1a, U1b, U2), and/or the neighbor coupling
structure (N, N1a, N1b) and/or the plaquette coupling structure (P1a, P1b, P2) comprises a
waveguide resonator and/or a tunable coupler.

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18. Quantum chip (101, 102, 103, 104) according to anyone of the preceding claims,
wherein a connectivity graph of the quantum chip is bi-planar and the coupling structures (U,
U1, U1a, U1b, U2, N, N1a, N1b, P1a, P1b, P2) are located on two layers without crossings on
individual layers.

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19. Method of manufacturing a quantum chip (101, 102, 103, 104) for an implementation
of an encoding according to a local fermion-to-qubit mapping for m fermionic modes, wherein
said mapping is defined by associating the m fermionic modes to m vertices v_i of a lattice

having edges e_{ij} connecting neighboring vertices v_i, v_j , and a plurality of plaquettes, each plaquette being surrounded by a plurality of vertices, by associating to each vertex a plurality of data qubits and a plurality of mutually anticommuting Pauli operators with support on the data qubits at said vertex, by defining for the vertices v_i and edges e_{ij} of the lattice a plurality

5 of vertex and edge operators B_i, A_{ij} which are expressed in terms of fermionic operators associated with the mode at said vertex v_i or modes at the vertices connected by a respective edge e_{ij} , and by expressing said edge and vertex operators B_i, A_{ij} in terms of said Pauli operators, said method comprising:

- providing first and second layers of the quantum chip (101, 102, 103, 104), wherein
- 10 m unit cells (1-9) are arranged at the m vertices of said lattice and located at least on the first layer, wherein each unit cell (1-9) comprises the plurality of data qubits (1a, b, c, d, e, f – 9a, b, c, d, e, f) associated with said vertex, wherein for each vertex v_i the data qubits in the support of the associated vertex operator have connectivity between themselves, wherein for each pair of neighboring unit cells (1-9) at
- 15 neighboring vertices v_i, v_j , the data qubits in the support of the edge operator A_{ij} associated with the edge e_{ij} connecting said vertices v_i, v_j have connectivity between themselves, wherein said layers further comprise for each plaquette (10, 20, 30, 40) of said lattice at least one syndrome qubit (11, 21, 31, 41) located on one of the layers, wherein the syndrome qubit (11, 21, 31, 41) and the data qubits of the unit
- 20 cells at the vertices surrounding the plaquette and which are in the support of the edge operators at the edges of the plaquette have connectivity between themselves, wherein the connectivity of the data and syndrome qubits is distributed over the two layers;
- superimposing the first and second layers to thereby manufacture the quantum chip
- 25 (101, 102, 103, 104).

20. Method for simulating a fermionic system on a quantum chip (101, 102, 103, 104) according to anyone of claims 1-18 or manufactured according to claim 19, wherein said method comprises implementing a fermionic operator encoded according to the local fermion-

30 to-qubit mapping by use of the connectivity between the qubits.

21. Method for performing quantum error detection and/or correction on a quantum chip (101, 102, 103, 104) according to anyone of claims 1-18 or manufactured according to claim 19, wherein said method comprises implementing at least one plaquette operator according to

35 the local fermion-to-qubit mapping by use of the connectivity between the qubits.