

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
31 July 2003 (31.07.2003)

PCT

(10) International Publication Number
WO 03/063250 A1

(51) International Patent Classification⁷: **H01L 27/108**

(21) International Application Number: PCT/US02/03244

(22) International Filing Date: 6 February 2002 (06.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/780,126 9 February 2001 (09.02.2001) US

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(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

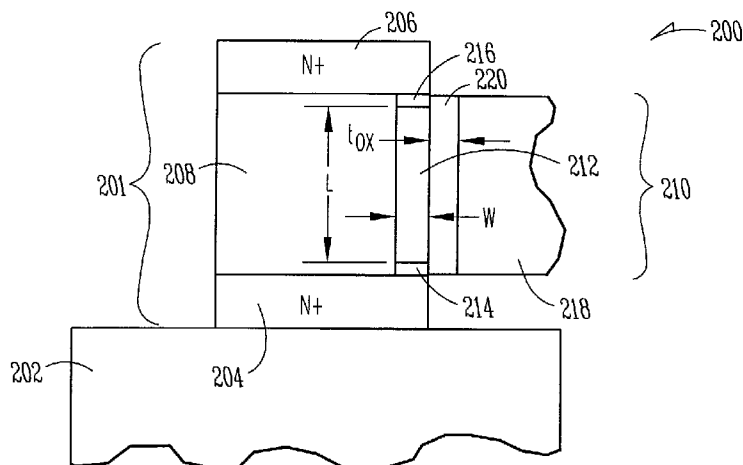
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Published:
— with international search report

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH ULTRA THIN VERTICAL BODY TRANSISTORS



(57) **Abstract:** Structures and method for programmable memory address and decode circuits with ultra thin vertical body transistor are provided. The memory address and decode circuits (200) includes a number of address lines and a number of output lines such that the address lines and the output lines form an array. A number of vertical pillars extend outwardly from a semiconductor substrate at intersections of output lines and address lines. Each pillar (201) includes a single crystalline first contact layer (204) and second contact layer (206) separated by an oxide (208). A number of single crystalline ultra thin vertical floating gate transistors that are selectively disposed adjacent the number of vertical pillars. Each single crystalline vertical floating gate transistor includes an ultra thin single crystalline vertical first source/drain region (214) coupled to the first contact layer, an ultra thin single crystalline vertical second source/drain region (216) coupled to the second contact layer, and an ultra thin single crystalline vertical body region (212) which opposes the oxide layer and couples the first and the second source/drain regions.