A DATA INTERFACE AND METHOD THEREFOR

Field of the Invention

This invention relates to a data interface for interfacing a slow speed data source with a higher speed data device, and more particularly to a data interface for interfacing slow speed display data from a source to a higher speed display device.

Background of the Invention

As is known, a liquid crystal display (LCD) has a fixed number of picture elements or pixels which determine the highest resolution the LCD can display. The higher the resolution of the LCD, the higher the speed at which display data must be supplied to the LCD.

There exist various different display modes such as video graphics adapter (VGA), super video graphics adapter (SVGA), and (XGA), each having different display resolutions, and consequently, having different display data speed requirements.

In order to couple sources having slower display data speeds than that required by the LCD, a converter interface is used to convert the data from the slower display data speed to the higher display data speed required by the LCD.

A conventional converter requires a large buffer memory into which each frame of the slower speed display data is stored, and the stored display data is then retrieved from the large buffer memory at the higher speed and provided to the LCD.

Consequently, as cost is directly proportional to the size of semiconductor memory employed, the conventional converter is expensive.

Brief Summary of the Invention

The present invention therefore seeks to provide an interface which overcomes, or at least reduces the above-mentioned problem of the prior art.

Accordingly, in one aspect the present invention provides a data interface comprising: an input for receiving a sequence of data packets at a first data rate; an input switching module coupled to the input for receiving the data packets, for switching the data packets alternately to a first and second output, and for providing output signals indicating the status of the data packets switched to the first and second outputs; a first and second memory coupled to the first and second outputs of the input switching module for storing the data packets and the first and second memory each having an output for providing the data packets retrieved therefrom at a second data rate greater than the first data rate; an output switching module coupled to the outputs of the first and second memory and coupled to an output for switching the data packets retrieved from the first and second memory to the output, the output switching module having an input for receiving a memory select signal indicating from which of the first or second memory to switch the data packets, and for providing output signals indicating the status of the retrieved data packets switched to the output; and a control module coupled to receive the output signals indicating the status of the data packets switched to the first and second outputs of the input switching module and the output signals indicating the status of the retrieved data packets switched to the output, for determining which of the first and second memory to retrieve the data packets from, and for providing the select signal in accordance with the determination.

In another aspect the present invention provides a method comprising the steps of: receiving a sequence of data packets at a first data rate; alternately storing the data packets in a first and second memory at the first data rate; and retrieving the data packets from the first and second memory at a second data rate, wherein retrieving the data packets from the first and second memory at a second data rate further comprises the steps of: retrieving one of the data packets from the first memory at the second data rate;determining whether another one of the data packets is completely stored in the second memory; retrieving the another one of the data packets from the second memory at the second data rate if the another one of the data packets is completely stored in the second memory; if the another data packet

is not completely stored in the second memory, determining whether storage time required to complete storage of the another one of the data packets in the second memory at the first data rate is greater than retrieval time required to completely retrieve the another one of the data packets from the second memory at the second data rate; repeating retrieval of the one of the data packets from the first memory when the storage time is greater than the retrieval time; and retrieving the another one of the data packets from the second memory when the storage time is less than the retrieval time.

Brief Description of the Drawings

The invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a schematic of an interface; and

FIGS. 2A and 2B show a flowchart detailing the operation of the interface in FIG. 1.

Detailed Description of the Drawings

The present invention uses a first and second memory. A storing process continuously stores received data packets alternately in the first memory or the second memory at a first data rate. Simultaneously, a retrieval process makes a determination as to from which of the first or second memory to retrieve data at a second data rate.

For example, after retrieving data from the first memory, the retrieval process makes a determination as to whether data is being stored in the second memory, if not then the data in the second memory is retrieved.

However, if data is being stored in the second memory, then a further determination is made as to whether the time required to complete storing data in the second memory is greater than the time that would be required to retrieve the data from the second memory if all the data was completely stored in the second memory.

If the time required to complete storing is greater, then the retrieval process repeats retrieval of the data in the first memory. Alternatively, if the time required to complete retrieval is less, then the data in the second memory is retrieved.

In FIG. 1 the interface includes an input 105 for receiving a sequence of data packets. Each data packet has a predetermined number of data bits which are received at the input 105 at a first bit rate. The predetermined number of data bits represent a line of video data for a video display. For example, a display having a display resolution of 480 by 680 indicates that there are 480 horizontal lines of video data that form a frame of a video display.

The input 105 is coupled to a receive bit counter 107 which counts the data bits and provides the counted data bits from an output. The receive bit counter 107 also provides a count signal indicating the number of data bits that have been counted, and a switch signal when the number of data bits counted is equal to the predetermined number. When the receive bit counter produces the switch signal it resets itself and starts counting the data bits of the next data packet.

A store multiplexer 109 is coupled to receive the counted data bits and the switch signal from the receive bit counter 107. The store multiplexer 109 alternately switches the counted data bits to a first output or a second output whenever the switch signal is received. In this way the sequence of data packets are alternately provided from the first and second outputs of the store multiplexer 109. In addition, the store multiplexer 109 also has a third output for providing a store status signal indicating whether the counted data bits are switched to the first or the second output.

A first memory 111 and a second memory 113 are coupled to the first and second outputs of the store multiplexer 109, respectively. The first and second memory 111 and 113 store the counted data bits provided from the store multiplexer 109 at the first data rate. Each of the first and second memory 111 and 113 have an output for providing data retrieved from the first and second memory 111 and 113 at a second rate, which is greater than the first rate. The first and second memory are dual ported memory device that support simultaneous storage and retrieval of data.

A store time calculator 120 includes a store time subtractor 121 coupled to receive the count signal from the receive bit counter 107 which indicates the number of data bits counted. The store time calculator 120 also includes a store time multiplier 123 and a store time memory 122. The store time memory 122 stores the first data rate and the predetermined number. The subtractor 121 is coupled to the memory 122 to receive the predetermined number and subtracts the number of data bits counted from the predetermined number to produce a difference signal. When a data packet is being received, the difference signal indicates the number of data bits to be received to complete reception of the data packet.

A retrieve multiplexer 115 has a first input coupled to the first output of the first memory 111, and a second input coupled to the output of the second memory 113. The retrieve multiplexer 115 also has a third input which receives a select signal. The select signal determines whether the retrieved data bits are switched from the first or second input to a data output. When the select signal has a first state the first input is switched to a data output, and when the select signal has a second state the second input is switched to the data output. In addition, the read multiplexer 115 provides a retrieve status signal indicating whether the first or second input is switched to the data output.

A retrieve bit counter 117 is coupled to the data output of the retrieve multiplexer 117 to receive the retrieved data bits. The retrieve bit counter 117 counts the retrieved data bits and provides the counted data bits to an output 119 at the second data rate. In addition the retrieve bit counter 117 provides a retrieve count signal indicating the number of retrieved data bits, and a retrieval complete signal when the number of retrieved data bits is equal to the predetermined number.

A retrieve time calculator 130 is coupled to receive the retrieve count signal from the retrieve bit counter 117 indicating the number of data bits retrieved. The retrieve time calculator 130 includes a retrieve time subtractor 121 coupled to a retrieve time multiplier 131 and a retrieve time memory 122. The predetermined number and the second data rate are stored in the retrieve time memory 122. The retrieve time subtractor 121 subtracts the number of data bits retrieved

from the predetermined number to produce a retrieve difference signal which indicates the number of data bits to be retrieved for each data packet being retrieved.

A controller 125 is coupled to receive the retrieval complete signal from the retrieve bit counter 117 and the retrieve status signal from the retrieve multiplexer 115. The controller 125 determines that the data bits stored in the first memory 111 have been completely retrieved when the retrieval complete signal and the retrieve status signal indicating the data output of the retrieve multiplexer is switched to the first output, are received.

The controller 125 is also coupled to receive the store status signal from the store multiplexer 109. The controller 125 determines that the counted data bits from the receive bit counter 107 are switched by the store multiplexer 109 to the second output when the store status signal is received indicating that the counted data bits from the receive bit counter 107 are switched by the store multiplexer 109 to the second output.

The controller includes a comparator 127 which is coupled to receive the storage time signal from the store time calculator and the retrieval time signal from the retrieval time calculator.

When the time required to complete reception of the number of data bits to be received for storage in the second memory is greater than the time required to completely retrieve the predetermined number of the data bits from the second memory, the comparator produces a select signal having the first state.

However, when the time required to retrieve the predetermined number of data bits from the second memory is greater than the time required to complete reception of the number of data bits to be received for storage in the second memory, the comparator produces the select signal having the second state.

In FIG. 2 when a first data bit of a data packet is received 202 at the first rate it is stored 204 in the first memory. A determination is then made as to whether the predetermined number of data bits have been received 205. If the number of data bits received 202 and stored 204 in the first memory is less than the predetermined number, then steps 202, 204 and 205 are repeated until the predetermined number of data bits are received and stored in the first memory.

Subsequently, a determination is made as to whether a next data packet has been received 206. Again, steps 206 of receiving a data bit , step 207 of storing the data bit, and step 208 of determine whether the predetermined number of data bits of the next data packet have been received and stored in the second memory, are repeated until the predetermined number of data bits have been received and stored.

The process the repeats by returning to step 202 and continuing as described above for each of the data packets in the sequence.

Simultaneously, an initial predetermined data packet is stored 210 in the second memory, and the following steps executed. Retrieval 212 of the data packet stored in the second memory is started, and a determination is then made as to whether the predetermined number of data bits have been retrieved 214. When the number of data bits retrieved is less than the predetermined number, a next data bit is retrieved 213. The steps of 214 and 213 continue until the predetermined number of data bits are retrieved from the second memory.

Next, a determination is made as to whether a data packet is being stored 216 in the first memory. If a data packet is being stored in the first memory, then the time required to complete storage of the data packet in the first memory is calculated 218.

Subsequently, the time required to complete storage of the data packet in the first memory at the first data rate compared 220 with the time required to completely retrieve a data packet from the first memory at the second data rate.

If the time required to store the time required to complete storage of the data packet in the first memory at the first data rate is greater than the time required to completely retrieve a data packet from the first memory at the second data rate, then the process returns to step 212 and again starts retrieving the data packet stored in the second memory and continues the process as described earlier.

If the time required to store the time required to complete storage of the data packet in the first memory at the first data rate is not greater than the time required to completely retrieve a data packet

from the first memory at the second data rate, the retrieval 222 of the data packet stored in the first memory is started.

A determination is then made as to whether the predetermined number of data bits have been retrieved 224. If the predetermined number of data bits have not been received the next data bit stored in the first memory is retrieved 223. Steps 224 and 223 are repeated until the predetermined number of data bits are retrieved from the first memory.

After the data packet stored in the first memory has been completely retrieved, a determination is made as to whether a data packet is being stored 226 in the second memory.

If a data packet is not being stored in the second memory, retrieval 212 of the data packet stored in the second memory at the second data rate is started, and the process continues from step 212 as described earlier.

However, if a data packet is being stored in the second memory, the time required to complete storage of the data packet at the first data rate in the second memory is calculated 228, and compared 229 with the time required to completely retrieve a data packet at the second data rate from the second memory.

If the time required to complete storage of the data packet at the first data rate in the second memory is not greater than the time required to completely retrieve a data packet at the second data rate from the second memory, then retrieval 212 of the data packet stored in the second memory at the second data rate is started, and the process continues from step 212 as described earlier.

In addition, if the time required to complete storage of the data packet at the first data rate in the second memory is greater than the time required to completely retrieve a data packet at the second data rate from the second memory, then re-retrieval 222 of the data packet stored in the second memory at the second data rate is started, and the process continues from step 222 as described earlier.

The present invention advantageously allows a memory that stores only two lines of video data to be used to provide a video interface. As such a small memory requirement is a fraction of the large memory employed in conventional video interfaces, a substantially cheaper video interface is realised.

Thus, in accordance with the described embodiments of the present invention, a first process stores data at a first rate in a first and second memory. A simultaneous retrieval process selectively retrieves the stored data at a second data rate which is greater than the first data rate. To prevent the retrieval process from catching up with the storing process, the retrieval process retrieves data only when the data can be retrieved completely without catching up with the storing process. When catch up is imminent, the retrieval process re-retrieves data.

Hence, the described video interface reduces the amount of memory required compared with video interfaces of the prior art, and as cost is directly proportional to the size of memory employed, the described video interface is cheaper.

* C L M S *

Claims

1. A data interface comprising:

an input for receiving a sequence of data packets at a first data rate;

an input switching module coupled to the input for receiving the data packets, for switching the data packets alternately to a first and second output, and for providing output signals indicating the status of the data packets switched to the first and second outputs;

a first and second memory coupled to the first and second outputs of the input switching module for storing the data packets and the first and second memory each having an output for providing the data packets retrieved therefrom at a second data rate greater than the first data rate;

an output switching module coupled to the outputs of the first and second memory and coupled to an output for switching the data packets retrieved from the first and second memory to the output, the output switching module having an input for receiving a memory select signal indicating from which of the first or second memory to switch the data packets, and for providing output signals indicating the status of the retrieved data packets switched to the output; and

a control module coupled to receive the output signals indicating the status of the data packets switched to the first and second outputs of the input switching module and the output signals indicating the status of the retrieved data packets switched to the output, for determining which of the first and second memory to retrieve the data packets from, and for providing the select signal in accordance with the determination.

2. A data interface according to claim 1 wherein each of the data packets have a predetermined number of data bits, and wherein the input switching module comprises:

* C L M S *

a receive bit counter coupled to the input for counting each data bit and having an output providing the counted data bits, the receive bit counter for providing a receive count signal which indicates the number of data bits counted and for providing a switch signal when the predetermined number of data bits are counted; and

a store multiplexer coupled to receive the counted data bits and the switch signal from the receive bit counter, the store multiplexer for switching the counted data bits alternately to the first output or the second output whenever the switch signal is received, and the store multiplexer including a third output for providing a store status signal indicating whether the counted data bits are switched to the first or the second output.

3. A data interface according to claim 1 wherein each of the data packets have a predetermined number of data bits, and wherein the output switching module comprises:

a retrieve multiplexer having a first and second input coupled to the outputs of the first and second memory respectively, a third input for receiving a memory select signal, the retrieve multiplexer for switching the first input to a data output when the memory select signal has a first state and for switching the second input to the data output when the memory select signal has a second state, and the retrieve multiplexer for providing a retrieve status signal indicating whether the data output is switched to the first or second input; and

a retrieve bit counter coupled to the data output for counting the retrieved data bits and for providing the counted data bits to the output at the second data rate, the retrieve bit counter for providing a retrieve count signal indicating the number of retrieved data bits, and for providing a retrieval complete signal when the number of retrieved data bits is equal to the predetermined number.

4. A data interface according to claims 1,2 and 3 wherein each of the data packets have a predetermined number of data bits, and wherein the control module comprises:

a store time calculator coupled to receive the receive count signal and including a store time subtractor for subtracting the number of data bits counted from the predetermined number to produce a receive difference signal indicating the number of data bits to be received, and a store time multiplier coupled to receive the receive difference signal from the subtractor for multiplying the number of data bits to be received by the first data rate to produce a storage time signal indicating the time required to complete reception of the number of data bits to be received for each data packet being received;

a retrieve time calculator coupled to receive the retrieve count signal and including a retrieve time subtractor for subtracting the number of retrieved data bits from the predetermined number to produce a retrieve difference signal indicating the number of data bits to be retrieved, the retrieve time calculator having a retrieve time multiplier coupled to receive the read difference signal for multiplying the number of data bits to be retrieved by the second data rate to produce a retrieval time signal indicating the time required to complete retrieval of the number of data bits to be retrieved for each data packet being retrieved; and

a controller for determining that the data bits stored in the first memory have been completely retrieved when the retrieval complete signal and the retrieve status signal indicating the data output of the retrieve multiplexer is switched to the first output are received, the controller for determining that counted data bits are switched to the second memory when the store status signal indicating that counted data bits are switched to the second output is received,
the controller including a comparator coupled to receive the output signals from the store time calculator and the retrieve time calculator, for producing the select signal having the first state when the time required to complete reception of the number of data bits to be

received for storage in the second memory is greater than the time required to completely retrieve the predetermined number of the data bits from the second memory, and the comparator for producing the select signal having the second state when the time required to retrieve the predetermined number of data bits from the second memory is greater than the time required to complete reception of the number of data bits to be received for storage in the second memory.

5. A data interface according to claim 1 wherein the first memory has an input for receiving a store signal from the controller module when the data bits received from the input are to be stored in the first memory, and having an input for receiving a retrieve signal from the controller module when the data bits stored in the first memory are to be retrieved.

6. A data interface according to claim 1 wherein the second memory has an input for receiving a store signal from the controller module when the data bits received from the input are to be stored in the second memory, and having an input for receiving a retrieve signal from the controller module when the data bits stored in the second memory are to be retrieved.

7. A data interface according to claim 4 wherein the store time calculator further comprises a store time memory coupled to the store time subtractor for storing the predetermined number and the first data rate.

8. A data interface according to claim 4 wherein the retrieve time calculator further comprises a retrieval time memory coupled to the retrieve time subtractor for storing the predetermined number and the second data rate.

9. A data interface according to any one preceding claim wherein each data packet comprises a line of video data for a video display.

10. A method comprising the steps of:

a) receiving a sequence of data packets at a first data rate;

b) alternately storing the data packets in a first and second memory at the first data rate:

c) retrieving the data packets from the first and second memory at a second data rate,

wherein step (c) further comprises the steps of:

c1) retrieving one of the data packets from the first memory at the second data rate;

c2) determining whether another one of the data packets is completely stored in the second memory;

c3) retrieving the another one of the data packets from the second memory at the second data rate if the another one of the data packets is completely stored in the second memory;

c4) if the another data packet is not completely stored in the second memory, determining whether storage time required to complete storage of the another one of the data packets in the second memory at the first data rate is greater than retrieval time required to completely retrieve the another one of the data packets from the second memory at the second data rate;

c5) repeating retrieval of the one of the data packets from the first memory when the storage time is greater than the retrieval time; and

c6) retrieving the another one of the data packets from the second memory when the storage time is less than the retrieval time.