

SEMICONDUCTOR PACKAGING METHOD AND SEMICONDUCTOR PACKAGING STRUCTURE

TECHNICAL FIELD

Embodiments of this disclosure relate to a semiconductor packaging method and a semiconductor packaging structure.

BACKGROUND

In the related art, a packaging process may involve placing, among other components to be packaged, an inductor and a die side by side on a carrier board. Such a parallelly constructed package resulting from the process is bulky in size and lacks structural compactness.

In view of the demand for increasingly miniaturized electronics with lighter weights, structurally compact small-size chip packages would become more and more popular in the marketplace.

SUMMARY OF THE INVENTION

At least one embodiment of the present disclosure provides a semiconductor packaging method, including:

fixing a die, an inductance element and a conductive post to a carrier board, wherein a front side of the die faces the carrier board, the inductance element is disposed on a back side of the die opposite to the front side, and the conductive post is located beside the die;

forming a plastic encapsulation layer on the carrier board, the plastic encapsulation layer encapsulating the die, the inductance element and the conductive post, with at least part of the inductance element and an end face of the first end of the

conductive post being both exposed from the plastic encapsulation layer;

forming a first conductive trace on a surface of the plastic encapsulation layer close to the back side of the die, the first conductive trace connecting the at least part of the inductance element to the first end of the conductive post;

removing the carrier board; and

forming a second conductive trace on a surface of the plastic encapsulation layer close to the front side of the die, the second conductive trace connecting a bond pad on the die to a second end of the conductive post.

At least one embodiment of the present disclosure also provides a semiconductor packaging structure including: a plastic encapsulation layer; a die disposed within the plastic encapsulation layer, the die provided on a front side thereof with a bond pad; an inductance element disposed on a back side of the die so as to be located between the die and the plastic encapsulation layer; a conductive post disposed in the plastic encapsulation layer beside the die in such a manner that a first end of the conductive post is exposed from a surface of the plastic encapsulation layer close to the back side of the die and that a second end of the conductive post is exposed from a surface of the plastic encapsulation layer close to the front side of the die; a first conductive trace disposed on the surface of the plastic encapsulation layer close to the back side of the die and connecting the inductance element to the first end of the conductive post; and a second conductive trace disposed on the surface of the plastic encapsulation layer close to the front side of the die and connecting the bond pad to the second end of the conductive post.

In embodiments of the present disclosure, through disposing the inductance element on the back side of the die, the die and the inductance element are stacked together along the thickness direction of the die. This sensible spatial utilization in the thickness direction of the die enables the semiconductor packaging structure to have a compact structure and a reduced size. Therefore, the semiconductor packaging structure

according to the embodiments of the disclosure is small in size, compact in structure and suitable for use in a small-size, lightweight electronic device.

The details of one or more embodiments of this disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to more clearly explain the subject matter of embodiments of the present disclosure, the accompanying drawings, to which reference is to be made in connection with the following description of the embodiments, will be briefed below. Apparently, these drawings show only some embodiments of, but do not imply any limitation on, the disclosure.

Fig. 1 is a schematic diagram showing the structure of a semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 2 is a flowchart of a semiconductor packaging method according to an embodiment of the present disclosure.

Fig. 3A shows a structural schematic of an intermediate structure formed during a process for producing a semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 3B shows a structural schematic of an intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 3C shows a structural schematic of an intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 4 shows a structural schematic of another intermediate structure formed

during the process according to an embodiment of the present disclosure.

Fig. 5 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 6 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 7 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 8A shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 8B shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 9 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 10 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 11 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 12 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to

an embodiment of the present disclosure.

Fig. 13 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 14 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 15 shows a structural schematic of a further intermediate structure formed during the process for producing the semiconductor packaging structure according to an embodiment of the present disclosure.

Fig. 16 is a schematic diagram showing dicing of a plastic encapsulation body according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

Here, exemplary embodiments will be described in detail, examples of which are illustrated in the accompanying drawings. When referring to the drawings below, unless otherwise indicated, like numerals throughout different ones of them represent the same or similar elements. The exemplary embodiments described hereunder do not represent all possible embodiments consistent with the present application. Rather, they are merely examples of devices and methods consistent with some aspects of this disclosure as detailed in the appended claims.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of this disclosure. As used herein and in the appended claims, the singular forms “a”, “an”, and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be also understood that, as used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

It should be understood that although the terms such as “first”, “second”, “third” and the like may be used herein to describe various types of information, such information is not limited to these terms. These terms serve only to distinguish between information of the same type. For example, without departing from the scope of the present application, “first information” may be alternatively referred to as “second information”. Similarly, “second information” may be alternatively referred to as “first information”. Depending on the context, the term “if” as used herein may be interpreted as “when”, “upon” or “in response to a determination that”.

Several embodiments of the present disclosure will be described in detail below with reference to the accompanying drawings. Whenever there is no conflict, the following embodiments and features thereof can be combined with one another.

At least one embodiment of this disclosure provides a semiconductor packaging structure including: a plastic encapsulation layer; a die disposed in the plastic encapsulation layer, the die provided on a front side thereof with a bond pad; an inductance element provided on a back side of the die so as to be situated between the die and the plastic encapsulation layer; a conductive post disposed in the plastic encapsulation layer beside the die so as to be exposed both at a first end from a surface of the plastic encapsulation layer close to the back side of the die and at a second end from a surface of the plastic encapsulation layer close to the front side of the die; a first conductive trace disposed on the first surface of the plastic encapsulation layer close to the back side of the die and connecting the inductance element to the first end of the conductive post; and a second conductive trace disposed on the second surface of the plastic encapsulation layer close to the front side of the die and connecting the bond pad to the second end of the conductive post.

The semiconductor packaging structure is a chip package and is suitable for use in the packaging of an antenna chip. The semiconductor packaging structure can be used in an electronic device such as a mobile phone, a computer or the like. As shown in Fig.

1, the semiconductor packaging structure 1 may include: the plastic encapsulation layer 14; the die 11 that is disposed in the plastic encapsulation layer 14 and is provided on the front side 101 with the bond pad 102; the inductance element 12 that is disposed on the back side 103 of the die 11 opposing the front side 101 so as to be situated between the die 11 and the plastic encapsulation layer 14; the conductive post 13 that is disposed in the plastic encapsulation layer 14 beside the die 11; the first conductive trace 15 that is disposed on the first surface 141 of the plastic encapsulation layer 14 close to the back side 103 of the die 11; the second conductive trace 16 that is disposed on the second surface 142 of the plastic encapsulation layer 14 close to the front side 101 of the die 11; and a protective layer 17 disposed on the front side 101 of the die 11. The semiconductor packaging structure 1 may further include a first conductive filled interconnect 18, a second conductive filled interconnect 19, a first dielectric layer 110, a conductive bump 111, a second dielectric layer 112 and a surface finish layer 1111.

In one embodiment of the present disclosure, the die 11 has the front side 101 and the back side 103, which oppose each other. The front side is an active surface provided thereon with the bond pad 102 which is configured for external electrical connection.

In one embodiment of the present disclosure, as shown in Fig. 1, the inductance element 12 is provided on the back side 103 of the die 11. The inductance element 12 is an electromagnetic conversion component. In one embodiment of the present disclosure, without wishing to be limiting, the inductance element 12 may be made of copper.

In one embodiment of the present disclosure, the inductance element 12 has a first electrical connection point located on the side of the inductance element 12 away from the die 11. The first electrical connection point is configured for external electrical connection.

In one embodiment of the present disclosure, as shown in Fig. 1, the conductive post 13 is disposed beside the die 11. Without wishing to be limiting, the conductive

post 13 may be made of copper. The conductive post 13 has the first end 131 and the second end 132. The first end 131 of the conductive post 13 is close to the inductance element 12, while the second end 132 of the conductive post 13 is away from the inductance element 12. The first end 131 of the conductive post 13 is opposite to the second end 132 of the conductive post 13. End faces of the conductive post 13 at the first 131 and second 132 ends are both exposed from the plastic encapsulation layer 14.

In one embodiment of the present disclosure, as shown in Fig. 1, the plastic encapsulation layer 14 encapsulates the die 11, the inductance element 12 and the conductive post 13. The plastic encapsulation layer 14 may be made of a polymer, a resin, a composite resin material or a composite polymer material. For example, the plastic encapsulation layer 14 may be made of a resin embedded with a filler. The filler may be inorganic particles.

In one embodiment of the present disclosure, the plastic encapsulation layer 14 includes a first opening 143 in which the first electrical connection point of the inductance element 12 is exposed. For example, the first opening 143 is provided on the side of the plastic encapsulation layer 14 close to the inductance element 12. A projection of the first opening 143 on the inductance element 12 at least partially overlaps with a projection of the first electrical connection point on the inductance element 12, resulting in exposure of at least part of the first electrical connection point from the plastic encapsulation layer 14. For example, the projection of the first opening 143 on the inductance element 12 may completely overlap with the projection of the first electrical connection point on the inductance element 12, resulting in exposure of the first electrical connection point from the plastic encapsulation layer 14. As another example, the projection of the first opening 143 on the inductance element 12 may partially overlap with the projection of the first electrical connection point on the inductance element 12, resulting in exposure of part of the first electrical connection point from the plastic encapsulation layer 14.

In one embodiment of the present disclosure, as shown in Fig. 1, the semiconductor packaging structure further includes the first conductive filled interconnect 18 located within the first opening 143. The first conductive filled interconnect 18 is electrically connected to both the first electrical connection point of the inductance element 12 and the first conductive trace 15. Without wishing to be limiting, the first conductive filled interconnect 18 may be formed of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the semiconductor packaging structure further includes the first conductive trace 15 that is disposed on the side of the plastic encapsulation layer 14 close to the back side of die 11 and connects the first electrical connection point of the inductance element 12 to the first end 131 of the conductive post 13. Without wishing to be limiting, the first conductive trace 15 may be made of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the semiconductor packaging structure further includes the first dielectric layer 110 disposed on the first surface 141 of the plastic encapsulation layer 14 so as to cover at least the first conductive trace 15. The first dielectric layer 110 may be composed of one or more layers of insulating materials, each of which may be polyimide (PI), polybenzoxazole (PBO), an organic polymer, an organic composite polymer material or another material with similar properties.

In one embodiment of the present disclosure, as shown in Fig. 1, the semiconductor packaging structure further includes the protective layer 17 that is disposed on the front side 101 of the die 11. The protective layer 17 may be composed of one or more layers of insulating materials, each of which may be PI, PBO, an organic polymer, an organic composite polymer material or another material with similar properties.

In one embodiment of the present disclosure, the protective layer 17 has a second opening 171 in which the bond pad 102 on the die 11 is exposed. A projection of the

second opening 171 on the die 11 at least partially overlaps with a projection of the bond pad on the die 11, resulting in exposure of at least part of the bond pad 102 from the protective layer 17. For example, the projection of the second opening 171 on the die 11 may completely overlap with the projection of the bond pad 102 on the die 11, resulting in exposure of the bond pad 102 from the protective layer 17. As an example, the projection of the second opening 171 on the die 11 may partially overlap with the projection of the bond pad 102 on the die 11, resulting in exposure of part of the bond pad 102 from the protective layer 17.

In one embodiment of the present disclosure, as shown in Fig. 1, the second conductive filled interconnect 19 is located in the second opening 171 and is electrically connected to both the bond pad 102 on the die 11 and the second conductive trace 16. Without wishing to be limiting, the second conductive filled interconnect 19 may be formed of copper.

In one embodiment of the present disclosure, the semiconductor packaging structure further includes the second conductive trace 16 that is disposed on both the protective layer 17 and the second surface 142 of the plastic encapsulation layer 14 close to the front side of the die 11 and connects the bond pad 102 on the die 11 to the second end 132 of the conductive post 13. Without wishing to be limiting, the second conductive trace 16 may be made of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the semiconductor packaging structure further includes the conductive bump 111 that is disposed on the second conductive trace 16. Without wishing to be limiting, the conductive bump 111 may be made of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the semiconductor packaging structure further includes the second dielectric layer 112 that is disposed on the side of the protective layer 17 away from the die 11 so as to cover at least the second conductive trace 16 and encapsulate the conductive bump 111, with a

surface of the conductive bump 111 away from the die 11 being exposed from the second dielectric layer 112. The second dielectric layer 112 may be composed of one or more layers of insulating materials, each of which may be PI, PBO, an organic polymer, an organic composite polymer material or another material with similar properties.

In one embodiment of the present disclosure, the semiconductor packaging structure may further include the surface finish layer 1111 that is disposed on the exposed surface of the conductive bump 111 and configured to slow down oxidation of the conductive bump 111. The surface finish layer may be formed of matte tin or an electroplated composite layer. For example, the electroplated composite layer may include a third metal layer and a fourth metal layer. The third metal layer may reside on the surface of the conductive bump 111, and the fourth metal layer may reside on the third metal layer. The third metal layer may be a nickel (Ni) layer, while the fourth metal layer may be a gold (Au) layer. As another example, the electroplated composite layer may further include a fifth metal layer sandwiched between the third and fourth metal layers. The fifth metal may be a palladium (Pd) layer.

In one embodiment of the present disclosure, the inductance element 12 is electrically connected to the bond pad 102 on the die 11 through the first conductive filled interconnect 18, the first conductive trace 15, the conductive post 13, the second conductive trace 16 and the second conductive filled interconnect 19.

According to the embodiments of this disclosure, through disposing the inductance element on the back side of the die, the die and the inductance element are stacked together along the thickness direction of the die. This sensible spatial utilization in the thickness direction of the die enables the semiconductor packaging structure to have a compact structure and a reduced size. Therefore, the semiconductor packaging structure according to the embodiments of the disclosure is small in size, compact in structure and suitable for use in a small-size, lightweight electronic device.

At least one embodiment of the present disclosure also provides a semiconductor

packaging method. As shown in Fig. 2, the semiconductor packaging method includes steps S201 to S211 below.

In step 201, a die, an inductance element and a conductive post are fixed to a carrier board. A front side 101 of the die 11 is provided thereon with a bond pad 102 and is oriented to face the carrier board. A protective layer 17 is also provided on the front side 101 of the die 11, and an inductance element 12 is provided on a back side 103 of die 11. The conductive post 13 is located beside the die 11.

In one embodiment of the present disclosure, the front side 101 of the die 11 is provided with the protective layer 17 whose surface away from the inductance element 12 is spaced from a surface of the inductance element 12 away from the protective layer 17 by a distance smaller than a height of the conductive post 13, which is measured as a distance between a first end 131 of the conductive post 13 and a second end 132 of the conductive post 13.

In one embodiment of the present disclosure, as a result of fixing the die 11, the inductance element 12 and the conductive post 13 to the carrier board 31, an intermediate structure as shown in Fig. 3A is obtained. Although Fig. 3A shows three of the dies 11 being fixed to the carrier board, in practice, either one or more of the dies may be fixed to the carrier board, and the present disclosure is not limited to any particular number of the dies.

In one embodiment of the present disclosure, the fixation of the die 11 and the conductive post 13 to the carrier board 31 is accomplished with an adhesive layer applied to the carrier board 31. In one embodiment of the present disclosure, the adhesive layer is a thermally removable layer.

In one embodiment of the present disclosure, step S201 may include: at first, as shown in Fig. 3B, forming a metal layer 32 on the carrier board 31; then, as shown in Fig. 3C, etching the metal layer 32 to form the conductive post 13; and subsequently, bonding the die 11 onto the carrier board 31 with the adhesive layer.

In an alternative embodiment of this disclosure, the conductive post may be pre-formed. In this case, step S201 may include: at first, providing the die 11 and the pre-formed conductive post 13; and then, bonding the die 11 and the conductive post 13 onto the carrier board 31 with the adhesive layer.

In some embodiments of the present disclosure, prior to step S201, the following steps are included.

At first, a seed layer is formed over a back side of a silicon wafer by a sputtering process.

As shown in Fig. 4, in one embodiment of the present disclosure, the seed layer 40 includes a first seed layer 401 on the silicon wafer 42. The first seed layer 401 is a copper layer.

In an alternative embodiment of this disclosure, the seed layer 40 further includes a second seed layer 402 between the silicon wafer 42 and the first seed layer 401. The second seed layer 402 is a titanium layer. In this case, the formation of the seed layer involves first forming the second seed layer 402 on the back side of the silicon wafer and then forming the first seed layer 401 on the second seed layer. Forming first the titanium second seed layer 402 on the silicon wafer 42 and then the copper first seed layer 401 on the second seed layer 402 enables increased adhesion between the silicon wafer 42 and the first seed layer 401. The copper first seed layer 401 provides good mechanical properties and electrical conductivity.

Subsequently, a first metal layer is formed on the seed layer by an electroplating process. In one embodiment of the present disclosure, the first metal layer may be a copper layer. As a result of forming the first metal layer 41 on the seed layer, an intermediate structure as shown in Fig. 4 is obtained. The first metal layer 41 is spaced apart from the silicon wafer 42 by the seed layer.

It is to be noted that the seed layer between the first metal layer and the back side of the silicon wafer may be omitted. In the remaining drawings, the seed layer 40 is not

shown for the sake of simplicity.

Afterward, an etching process is performed on the first metal layer 41 and the seed layer, resulting in the formation of the inductance element 12. In one embodiment, as shown in Fig. 5, the inductance element 12 is formed by etching the first metal layer 41. For example, the formation of the inductance element (inductor/coil) on the back side of the silicon wafer may involve spin coating of photoresist, exposure, development, etching and stripping of the photoresist. In one embodiment of the present disclosure, the inductance element may be a coil.

After that, the protective layer 17 is formed on a front side of the silicon wafer. In one embodiment of the present disclosure, as shown in Fig. 6, the protective layer 17 is formed on the front side of the silicon wafer 42. The protective layer 17 may be formed by lamination, spin coating, printing, molding or another suitable method. The protective layer 17 may be formed of a laser-reactive material or a photosensitive material.

The die 11 is then obtained by dicing the silicon wafer. In one embodiment of the present disclosure, as shown in Fig. 7, the die 11 is obtained by dicing the silicon wafer 42.

It is to be noted that, in practical implementations, the seed layer may be omitted from between the silicon wafer 42 and the inductance element 12.

It is to be also noted that although the formation of the inductance element 12 on the back side of the silicon wafer has been described above as preceding the formation of the protective layer on the front side of the silicon wafer, in some embodiments of this disclosure, it is also possible that the formation of the protective layer on the front side of the silicon wafer precedes the formation of the inductance element on the back side of the silicon wafer. The present disclosure is not limited in this regard.

In step S202, a plastic encapsulation layer is formed on the carrier board so as to encapsulate the die 11, the inductance element 12 and the conductive post 13, with a

first electrical connection point of the inductance element 12 and the end face of the first end of the conductive post 13 being both exposed from the plastic encapsulation layer 14.

In one embodiment of the present disclosure, as shown in Fig. 8A, the plastic encapsulation layer 14 encapsulates the die 11, the inductance element 12 and the conductive post 13, while the first end face of the conductive post 13 is exposed from the plastic encapsulation layer 14. A thickness of the plastic encapsulation layer 14 is equal to a height of the conductive post 13.

In one embodiment of the present disclosure, step S202 may include the steps of: at first, as shown in Fig. 8B, forming, on the carrier board, an encapsulation layer 81 which encapsulates the die 11, the inductance element 12 and the conductive post 13 and has a thickness greater than the height of the conductive post 13; and then thinning the encapsulation layer 81 to form the plastic encapsulation layer 14, from which the first end of the conductive post 13 is exposed. The thickness of the plastic encapsulation layer 14 is equal to the height of the conductive post 13. The thinning of the encapsulation layer 81 may be accomplished by mechanical polishing.

In one embodiment of the present disclosure, as shown in Fig. 9, a first opening 143 in which the first electrical connection point of the inductance element 12 is exposed is formed in the plastic encapsulation layer 14. A projection of the first opening 143 on the inductance element 12 at least partially overlaps with a projection of the first electrical connection point on the inductance element 12, resulting in exposure of at least part of the first electrical connection point.

In one embodiment of the present disclosure, as shown in Fig. 9, the first opening 143 may be formed by performing a laser drilling process on a surface of the plastic encapsulation layer 14. For example, the first opening in which the first electrical connection point of the inductance element 12 is exposed may be formed in the plastic encapsulation layer 14 using a laser.

In step S203, a first conductive trace connecting the first electrical connection point of the inductance element to the first end of the conductive post is formed on a surface of the plastic encapsulation layer close to the back side of the die.

In one embodiment of the present disclosure, as shown in Fig. 10, a first conductive filled interconnect 18 may be formed by filling a first conductive medium in the first opening 143, and a first conductive layer may be formed on the plastic encapsulation layer 14. The first conductive filled interconnect 18 is electrically connected to the first electrical connection point of the inductance element, and the first conductive layer is electrically connected to the first conductive filled interconnect 18. The first conductive layer may be formed by metal sputtering, electrolytic plating, electroless plating or another technique. The first conductive filled interconnect 18 and the first conductive layer may be formed in the same process step. After that, the first conductive layer may be patterned to form the first conductive trace 15. In this way, the inductance element 12 is electrically connected to the conductive post 13 via the first conductive trace 15.

In step S204, a first dielectric layer 110 covering at least the first conductive trace 15 is formed on the surface of the plastic encapsulation layer close to the back side of the die.

In one embodiment of the present disclosure, as shown in Fig. 11, the first dielectric layer 110 covering at least the first conductive trace 15 is formed on the surface of the plastic encapsulation layer close to the back side of the die. In one embodiment of the present disclosure, a projection of the first dielectric layer 110 on the carrier board may encompass the entire carrier board. The first dielectric layer 110 may be formed by lamination, spin coating, printing, molding or another suitable method.

In step S205, the carrier board is removed.

In step S206, a second opening in which the bond pad on the die is exposed is

formed in the protective layer 17.

In one embodiment of the present disclosure, as shown in Fig. 12, at least part of the bond pad is exposed in the second opening 171 formed in the protective layer 17. In case of the protective layer 17 being formed of a laser-reactive material, the second opening may be formed in the protective layer 17 by a laser drilling process. In case of the protective layer 17 being formed of photosensitive material, the second opening may be formed in the protective layer 17 by a photolithography process.

Although the method has been described above in the context of step S206 being performed after step S205 as an example, the formation of the second opening in the protective layer 17 may also be performed after the step of forming the protective layer on the front side of the silicon wafer and before the step of fixing the die and the conductive post to the carrier board.

In step S207, a second conductive trace connecting the bond pad on the die to the second end of the conductive post 13 is formed on a surface of the plastic encapsulation layer close to the front side of the die.

In one embodiment of the present disclosure, as shown in Fig. 13, a second conductive filled interconnect 19 electrically connected to the bond pad on the die 11 may be first formed by filling a second conductive medium in the second opening 171, and a second conductive layer electrically connected to the second conductive filled interconnect 19 may be formed over the plastic encapsulation layer 14 and the protective layer 17. The second conductive layer may be formed by metal sputtering, electrolytic plating, electroless plating or another technique. The second conductive filled interconnect 19 and the second conductive layer may be formed in the same process step. The second conductive layer may be then patterned to form the second conductive trace 16.

In step S208, a conductive bump is formed at a second electrical connection point of the second conductive trace.

In one embodiment of the present disclosure, as shown in Fig. 14, the conductive bump 111 is formed at the second electrical connection point of the second conductive trace 16.

In step S209, a second dielectric layer 112 covering at least the second conductive trace 16 and encapsulating the conductive bump 111 is formed on the surface close to the front side of the die, with a surface of the conductive bump 111 away from the die 11 being exposed from the second dielectric layer 112, resulting in the formation of a plastic encapsulation body.

In one embodiment of the present disclosure, as shown in Fig. 15, in the resulting plastic encapsulation body 20, the second dielectric layer 112 may cover the second conductive trace 16, while a surface of the second dielectric layer 112 away from the die 11 may be flush with the surface of the conductive bump 111 away from the die 11. In practical use, the second dielectric layer 112 may be so formed as to have a distance between its surfaces away from and close to the die 11, which may be greater than a distance of the die 11 between its surfaces away from and close to the die 11. The so-formed second dielectric layer 112 may be then thinned until its surface away from the die 11 becomes flush with the surface of the conductive bump 111 away from the die 11.

In step S210, a surface finish layer is formed on the exposed surface of the conductive bump.

Of course, in an alternative embodiment of the present disclosure, the surface finish layer may not be formed on the surface of the conductive bump 111.

In step S211, a semiconductor packaging structure is obtained by dicing the plastic encapsulation body. The semiconductor packaging structure includes the die, the inductance element, the conductive post, the plastic encapsulation layer, the first conductive trace and the second conductive trace.

In one embodiment of the present disclosure, as shown in Fig. 16, the

semiconductor packaging structure as shown in Fig. 1 may be obtained by performing a dicing operation on the plastic encapsulation body 20 at a dicing location P.

In the embodiments of the present disclosure, through disposing the inductance element on the back side of the die, the die and the inductance element are stacked together along the thickness direction of the die. This sensible spatial utilization in the thickness direction of the die enables the semiconductor packaging structure to have a compact structure and a reduced size. Therefore, the semiconductor packaging structure according to the embodiments of the disclosure is small in size, compact in structure and suitable for use in a small-size, lightweight electronic device.

In this disclosure, the device embodiments and the method embodiments may supplement each other if there is no conflict therebetween. The foregoing device embodiments are only illustrative, and the modules thereof that have been described as separate components may be physically separated or not, and the components that have been shown as modules may be physical modules or not. They may be deployed in a single location or distributed across a plurality of network devices. As practically required, either all or some of such modules may be selected in accordance with embodiments disclosed herein. Those of ordinary skill in the art can understand and implement them without paying any creative effort.

Presented above are merely several exemplary embodiments of the present disclosure, and they are not intended to limit this disclosure in any way. Any and all alternations, equivalent substitutions, modification and so on made within the spirit and principles of the present disclosure are considered to fall within the scope of protection of this disclosure.

CLAIMS

1. A semiconductor packaging method, comprising:

fixing a die, an inductance element and a conductive post to a carrier board, wherein a front side of the die faces the carrier board, the inductance element is disposed on a back side of the die opposite to the front side, and the conductive post is located beside the die;

forming a plastic encapsulation layer on the carrier board, the plastic encapsulation layer encapsulating the die, the inductance element and the conductive post so that at least part of the inductance element and an end face of a first end of the conductive post are both exposed from the plastic encapsulation layer;

forming a first conductive trace on a surface of the plastic encapsulation layer close to the back side of the die, the first conductive trace connecting the at least part of the inductance element to the first end of the conductive post;

removing the carrier board; and

forming a second conductive trace on a surface of the plastic encapsulation layer close to the front side of the die, the second conductive trace connecting a bond pad on the die to a second end of the conductive post.

2. The semiconductor packaging method according to claim 1,

wherein prior to fixing the die, the inductance element and the conductive post to the carrier board, the method further comprises:

forming a first metal layer on a back side of a silicon wafer by an electroplating process;

etching the first metal layer to form the inductance element; and

dicing the silicon wafer to form the die;

or

wherein prior to fixing the die and the conductive post to the carrier board, the method further comprises:

forming a seed layer on a back side of a silicon wafer by a sputtering process;
forming a first metal layer on the seed layer by an electroplating process;
etching the first metal layer and the seed layer to form the inductance element;
and
dicing the silicon wafer to form the die.

3. The semiconductor packaging method according to claim 2, wherein the seed layer comprises a first seed layer disposed on the silicon wafer, the first seed layer made of copper; preferably the seed layer further comprises a second seed layer disposed between the silicon wafer and the first seed layer, the second seed layer made of titanium.

4. The semiconductor packaging method according to any one of claims 1 to 3, wherein prior to fixing the die to the carrier board, the method further comprises forming a protective layer on the front side of the die, wherein a distance between a surface of the protective layer away from the inductance element and a surface of the inductance element away from the protective layer is smaller than a height of the conductive post.

5. The semiconductor packaging method according to any one of claims 1 to 4, wherein the conductive post is pre-formed, and wherein fixing the die and the conductive post to the carrier board comprises bonding the die and the conductive post to the carrier board with an adhesive layer.

6. The semiconductor packaging method according to any one of claims 1 to 4, wherein fixing the die and the conductive post to the carrier board comprises:

forming a second metal layer on the carrier board;

etching the second metal layer to form the conductive post; and

bonding the die to the carrier board with an adhesive layer.

7. The semiconductor packaging method according to any one of claims 1 to 6, wherein forming the plastic encapsulation layer on the carrier board comprises:

forming an encapsulation layer on the carrier board, the encapsulation layer encapsulating the die, the inductance element and the conductive post, the encapsulation layer having a thickness greater than a height of the conductive post; and

thinning the encapsulation layer to form the plastic encapsulation layer, from which the first end of the conductive post is exposed.

8. The semiconductor packaging method according to any one of claims 1 to 7, wherein after the plastic encapsulation layer is formed on the carrier board, the method further comprises forming, in the plastic encapsulation layer by a laser drilling process, a first opening in which at least part of the inductance element is exposed.

9. The semiconductor packaging method according to claim 8, wherein forming the first conductive trace on the surface of the plastic encapsulation layer close to the back side of the die comprises:

filling a first conductive medium in the first opening to form a first conductive filled interconnect and forming a first conductive layer on the plastic encapsulation

layer so that the first conductive filled interconnect is electrically connected to at least part of the inductance element, and the first conductive layer is electrically connected to the first conductive filled interconnect; and

patterning the first conductive layer to form the first conductive trace,

wherein the first conductive filled interconnect and the first conductive layer are formed in a same process step.

10. The semiconductor packaging method according to any one of claims 1 to 9, wherein after the first conductive trace is formed on the surface of the plastic encapsulation layer close to the back side of the die, the method further comprises:

forming a first dielectric layer on the surface of the plastic encapsulation layer close to the back side of the die, the first dielectric layer covering at least the first conductive trace.

11. The semiconductor packaging method according to claim 4, further comprising:

forming a second opening in the protective layer, in which the bond pad on the die is exposed, before the die is fixed to the carrier board or after the carrier board is removed.

12. The semiconductor packaging method according to claim 10, wherein forming the second conductive trace on the surface of the plastic encapsulation layer close to the front side of the die comprises:

filling a second conductive medium in the second opening to form a second conductive filled interconnect and forming a second conductive layer over both the

plastic encapsulation layer and the protective layer so that the second conductive filled interconnect is electrically connected to the bond pad on the die, and the second conductive layer is electrically connected to the second conductive filled interconnect; and

patterning the second conductive layer to form the second conductive trace;

wherein the second conductive filled interconnect and the second conductive layer are formed in a same process step.

13. The semiconductor packaging method according to claim 1, wherein after the second conductive trace is formed on the surface of the plastic encapsulation layer close to the front side of the die, the semiconductor packaging method further comprises:

forming a conductive bump on a surface of second conductive trace away from the die;

forming a second dielectric layer on the surface of the plastic encapsulation layer close to the front side of the die to form a plastic encapsulation body; wherein the second dielectric layer covers the second conductive trace and encapsulates the conductive bump so that a surface of the conductive bump away from the die is exposed from the second dielectric layer.

14. The semiconductor packaging method according to claim 13, further comprising finishing the exposed surface of the conductive bump.

15. A semiconductor packaging structure, comprising:

a plastic encapsulation layer;

a die disposed within the plastic encapsulation layer, the die provided on a front

side thereof with a bond pad;

an inductance element disposed on a back side of the die so as to be located between the die and the plastic encapsulation layer;

a conductive post disposed in the plastic encapsulation layer beside the die so that a first end of the conductive post is exposed from a surface of the plastic encapsulation layer close to the back side of the die and that a second end of the conductive post is exposed from a surface of the plastic encapsulation layer close to the front side of the die;

a first conductive trace disposed on the surface of the plastic encapsulation layer close to the back side of the die and connecting the inductance element to the first end of the conductive post; and

a second conductive trace disposed on the surface of the plastic encapsulation layer close to the front side of the die and connecting the bond pad to the second end of the conductive post.

16. The semiconductor packaging structure according to claim 15, further comprising:

a first dielectric layer disposed on the surface of the plastic encapsulation layer close to the back side of the die so as to cover the first conductive trace;

a protective layer covering the front side of the die and provided therein with an opening through which the second conductive trace is connected to the bond pad; and

a second dielectric layer disposed on the side of the protective layer away from the die so as to cover at least the second conductive trace.

17. The semiconductor packaging structure according to claim 16,

wherein the first dielectric layer comprises at least one layer of first insulating material comprising at least one of polyimide, polybenzoxazole, an organic polymer and an organic composite polymer material,

wherein the second dielectric layer comprises at least one layer of second insulating material comprising at least one of polyimide, polybenzoxazole, an organic polymer and an organic composite polymer material, and

wherein the protective layer comprises at least one layer of third insulating material comprising at least one of polyimide, polybenzoxazole, an organic polymer and an organic composite polymer material.

18. The semiconductor packaging structure according to claim 16 or 17, further comprising a conductive bump disposed so as to be in direct contact with the second conductive trace and encapsulated within the second dielectric layer, with a surface of the conductive bump away from the die being exposed from the second dielectric layer.

19. The semiconductor packaging structure according to claim 18, further comprising a surface finish layer disposed on the surface of the conductive bump exposed from the second dielectric layer.

20. The semiconductor packaging structure according to claim 19, wherein the surface finish layer is made of a material comprising one of matte tin and an electroplated composite layer.