SEMICONDUCTOR STRUCTURE FOR DIGITAL AND RADIOFREQUENCY APPLICATIONS, AND A PROCESS FOR FABRICATING SUCH A STRUCTURE

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a semiconductor-on-insulator structure for digital and radiofrequency applications. The invention also relates to a process for fabricating such a structure via transfer of a layer from a first substrate, called the “donor substrate”, to a second substrate, called the “receiver substrate”.

PRIOR ART

Semiconductor-on-insulator structures are multilayer structures comprising a substrate, which is generally made of silicon, an electrically insulating layer arranged on top of the substrate, which is generally a layer of oxide such as a layer of silicon oxide, and, arranged on top of the insulating layer, a semiconductor layer in which the source and drain of the structure are produced and which is generally a layer of silicon.

Such structures are referred to as semiconductor-on-insulator (SeOI) structures, and in particular are referred to as "silicon-on-insulator" (SOI) structures when the semiconductor is silicon.

Among existing SOI structures, fully-depleted silicon-on-insulator (FD-SOI) structures are commonly used for digital applications. FD-SOI structures are characterized by the presence of a thin oxide layer, arranged on a silicon carrier substrate, and of a very thin semiconductor layer called the SOI layer arranged on the oxide layer.

The oxide layer is located between the substrate and the SOI layer. The oxide layer is then said to be “buried” and is called the “BOX” for Buried OXide.

The SOI layer allows the conduction channel to be formed in the FD-SOI structure.

Because of the small thickness and of the uniformity of the BOX layer and of the SOI layer, it is not necessary to dope the conduction channel, and hence the structure is able to operate in a fully depleted mode.

FD-SOI structures have improved electrostatic characteristics with respect to structures without BOX layers. The BOX layer decreases the parasitic electrical capacitance between the source and drain, and also allows leakage of electrons from the conduction channel to the substrate to be considerably decreased by confining the flow of electrons to the conduction channel, thus decreasing electric current losses and improving the performance of the structure.

FD-SOI structures can be compatible with radio-frequency (RF) applications, but however suffer from the appearance of electrical losses in said substrate.

To compensate for these electrical losses and improve RF performance, it is known to use a substrate, in particular an SOI substrate, having a high electrical resistivity, this type of substrate commonly being referred to as an “HR substrate” for high-resistivity substrate. The latter is advantageously combined with a charge-trapping layer, i.e. a trap-rich layer. However, this type of substrate is incompatible with use of transistors the threshold voltage of which may be controlled via a back-side gate (back bias voltage).

Specifically, the presence of this layer containing trapped charges hinders back biasing (application of a potential difference to the back side) and may furthermore lead to an accelerated diffusion of dopants, thus preventing the production of high-quality PN junctions, because of problems with junction leakage.

In addition to FD-SOI structures comprising one BOX layer, FD-SOI structures comprising two BOX layers, which are called “double BOX” structures, have been produced.

The double-BOX-layer technology is advantageous in the case where the FD-SOI structure comprises double-gate transistors the gate electrodes of which are formed both above and below the conduction channel. Thus, the SOI layer of the back gate, which is called the back-gate SOI layer, is electrically separated from the SOI layer of the front gate, which is called the front-gate SOI layer, by a first BOX layer, and is also electrically separated from the base substrate by a second BOX layer.

Document US 2010/0176482 describes an example of such an FD-SOI structure comprising two BOX layers, for a CMOS technology.

According to this document, CMOS structures with a high-k gate dielectric and with a gate length of as small as 30 nm are fabricated using an optimized process allowing a good isolation between the devices and the back gate to be obtained.

The existing double-BOX technology is used for digital applications, and not both for radiofrequency and digital applications.

Moreover, the maximum power rating of double-BOX FD-SOI structures is limited with BOX layers of standard thickness. This is a problem for radiofrequency applications.

Specifically, to increase the power rating of certain radiofrequency components, such as power amplifiers and antenna switches, it is necessary to stack MOSFETs (MOSFET being the acronym of Metal-Oxide-Semiconductor Field-Effect Transistor) in order to ensure that the voltage between the drain and source is lower than the maximum permitted operating voltage.

However, the maximum voltage between the drain and the carrier substrate and the maximum voltage between the source and the carrier substrate are limited by the breakdown voltage of the BOX layer. With a BOX layer of standard thickness of 20 nm, the breakdown voltage is only 25 V (this leading to the design of devices with a much lower maximum voltage, ranging from 10 to 15 V), this being a substantial limitation.

Thus, the existing double-BOX technology for digital applications is incompatible with radiofrequency applications.

BRIEF DESCRIPTION OF THE INVENTION

One aim of the invention is to provide a semiconductor-on-insulator structure allowing the aforementioned drawbacks to be overcome. The invention aims to provide such a structure allowing digital applications and radiofrequency applications to be combined.

An aspect of the invention provides a semiconductor-on-insulator multilayer structure, comprising in succession from a back side to a front side of the structure:

- a semiconductor carrier substrate having an electrical resistivity comprised between 500 Ω.cm and 30 kΩ.cm,
- a first electrically insulating layer,
- an intermediate layer,
- a second electrically insulating layer, which has a thickness smaller than that of the first electrically insulating layer,
- an active semiconductor layer,

the multilayer structure being characterized in that it comprises:

- at least one FD-SOI region, in which the intermediate layer is a semiconductor layer,
- at least one RF-SOI region, adjacent to the FD-SOI region, in which the intermediate layer is a third electrically insulating layer, said RF-SOI region comprising at least one radiofrequency component plumb with the third electrically insulating layer.

According to example embodiments, the structure has the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the sum of the thicknesses of the first electrically insulating layer, of the second electrically insulating layer, and of the third electrically insulating layer is comprised between 50 nm and 1500 nm;
- the structure furthermore comprises a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer;
- the charge-trapping layer is made of polysilicon or of porous silicon;
- the intermediate semiconductor layer is made of crystalline or polycrystalline material;
- the intermediate semiconductor layer is made of amorphous material;
- the first electrically insulating layer is a layer of silicon oxide;
- the second electrically insulating layer is a layer of silicon oxide;
- the third electrically insulating layer is a layer of silicon oxide;

- the first electrically insulating layer has a thickness comprised between 20 nm and 1000 nm;
- the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm;
- the active semiconductor layer has a thickness comprised between 3 nm and 30 nm.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- providing a first donor substrate,
- forming a weakened zone in said first donor substrate, so as to delineate an intermediate first semiconductor layer,
- transferring said intermediate first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form an intermediate structure comprising the carrier substrate, the first electrically insulating layer and the transferred intermediate first semiconductor layer,
- locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
- depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
- providing a second donor substrate,
- forming a weakened zone in said second donor substrate, so as to delineate an active second semiconductor layer,
- transferring said active second semiconductor layer to the intermediate structure, a second electrically insulating layer being at the interface between the second donor substrate and the intermediate structure,
- producing:
    - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and
    - at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- forming an intermediate structure by depositing an intermediate first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
- locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
- depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
- providing a donor substrate,
- forming a weakened zone in said donor substrate, so as to delineate an active second semiconductor layer,
- transferring said active second semiconductor layer to the said intermediate structure, a second electrically insulating layer being at the interface between the donor substrate and the said intermediate structure,
- producing:
    - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and
    - at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

According to example embodiments, the processes have the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the radiofrequency component is produced in the active second semiconductor layer;
- the local removal of a segment of the intermediate first semiconductor layer and the deposition of a third electrically insulating layer in the cavity are carried out after the transfer of the second semiconductor layer to the intermediate structure;
- the process furthermore comprises forming a charge-trapping layer on the carrier substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer;
- the local removal comprises depositing a mask by lithography and etching the intermediate first semiconductor layer through at least one aperture of said mask;
- the process furthermore comprises, before the transfer of said second semiconductor layer to the intermediate structure, treating the free surfaces of the intermediate first semiconductor layer and the third electrically insulating layer in order to decrease the roughness thereof.

The multilayer structure according to embodiments of the invention can serve as carrier for the fabrication of transistors, in particular MOSFETs. MOSFETs are semiconductor devices comprising three active electrodes, namely an input electrode called the

drain, and a third electrode called the source. These transistors allow a voltage (or a current) output on the drain to be controlled by virtue of the gate.

In the present text, the term “on”, when it relates to the position of a first layer with respect to a second layer, or the position of a component with respect to a layer, does not necessarily imply that the first layer makes direct contact with the second or that the component makes direct contact with the layer. Unless otherwise specified, this term does not exclude one or more other layers being intermediate between the first layer and the second layer, or between the component and the layer.

The expression “plumb with”, which relates to the position of a component with respect to a layer within a structure, means that the component and the layer face each other in the direction of the thickness of the structure. In other words, any axis that extends through the thickness of the structure and that intercepts the component, also intercepts the layer plumb with this component.

DESCRIPTION OF THE FIGURES

Other advantages and features of the invention will become apparent upon reading the following description given by way of illustrative and non-limiting example, with reference to the following appended figures:

Figure 1 is a schematic of one embodiment of a multilayer structure according to invention, comprising two FD-SOI regions and one RF-SOI region;

Figure 2 is a schematic of one of the FD-SOI regions of the structure illustrated in Figure 1;

Figure 3 is a schematic of the RF-SOI region of the structure illustrated in Figure 1;

Figure 4 is a schematic of an intermediate structure, comprising an intermediate first semiconductor layer on a carrier substrate that has been covered beforehand with a first electrically insulating layer;

Figure 5 is a schematic of the intermediate structure of Figure 4, in which a cavity has been produced;

Figure 6 is a schematic of the intermediate structure of Figure 5, in which a cavity has been filled with an electrically insulating layer;

Figure 7 is a schematic of a multilayer structure;

Figure 8 is a schematic of the multilayer structure of Figure 7, in which a trench has been produced;

Figure 9 is a schematic of the multilayer structure of Figure 8, in which a lateral cavity has been produced;

Figure 10 is a schematic of the multilayer structure of Figure 9, in which the cavity has been filled with an electrically insulating layer.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

A first subject of the invention relates to a semiconductor-on-insulator multilayer structure that is usable both for digital applications and for radiofrequency applications.

Figure 1 illustrates one embodiment of such a multilayer structure 1 according to the invention.

With reference to Figure 1, the multilayer structure 1 comprises in succession, from a back side to a front side of the structure, a semiconductor carrier substrate 2, a first electrically insulating layer 3, an intermediate layer I, a second electrically insulating layer 5, and an active semiconductor layer 6.

The semiconductor carrier substrate 2 is a highly resistive substrate, i.e. it has a an electrical resistivity comprised between 500 Ω.cm and 30 kΩ.cm, and preferably comprised between 1 kΩ.cm and 10 kΩ.cm. A high resistivity gives the carrier substrate the ability to limit electrical losses and to improve the radiofrequency performance of the structure.

The first electrically insulating layer 3 allows the carrier substrate 2 to be insulated from the intermediate layer I and from the layers superjacent said intermediate layer.

The first electrically insulating layer 3 is preferably a layer of oxide. Since this layer is buried in the structure between the carrier substrate and the intermediate layer, it may also be called the “first BOX”. It is preferably a layer of silicon oxide.

The thickness of the first electrically insulating layer 3 is relatively large, and preferably comprised between 20 nm (nanometres) and 1000 nm. Specifically, too small a thickness, in particular one smaller than 20 nm, would run the risk of breakdown of the first electrically insulating layer. In particular, the first electrically insulating layer 3 preferably has a thickness larger than that of the active semiconductor layer 6.

Optionally, the structure 1 also comprises a charge-trapping layer 8, which is preferably made of polysilicon or of porous silicon, arranged between the carrier substrate 2 and the first electrically insulating layer 3. This charge-trapping layer allows the electrical charge that accumulates under the first electrically insulating layer 3 to be trapped.

The second electrically insulating layer 5 allows the active semiconductor layer 6 to be insulated from the intermediate layer I and from the layers subjacent the intermediate layer.

The second electrically insulating layer 5 is preferably a layer of oxide, and preferably a layer of silicon oxide. Since this layer is buried in the structure between the intermediate layer and the active semiconductor layer, it may be called the “second BOX”.

The second electrically insulating layer 5 has a thickness that is relatively small, and smaller than that of the first electrically insulating layer 3. This small thickness makes it possible to be able to control the threshold voltage of the transistor via suitable biasing (back bias voltage) of the subjacent intermediate layer. A thickness of the second

electrically insulating layer 5 preferably comprised between 10 nm and 100 nm is selected to this end.

The active semiconductor layer 6 is intended for the production both of digital components 11 and optionally of radiofrequency components 12, the components produced depending on the digital and radiofrequency applications desired for the structure.

The active semiconductor layer 6 is preferably a layer of single-crystal silicon.

The thickness of the active semiconductor layer 6 is preferably comprised between 3 nm and 30 nm, and more preferably between 5 nm and 20 nm. It is preferable for the thickness of the active semiconductor layer to be uniform over all the extent of the material, i.e. for its thickness to vary by 1 nm or less, in order to optimize the operation of the FD-SOI regions, in a fully depleted mode. The FD-SOI regions are described in detail below in the present text.

The multilayer structure 1 comprises a plurality of regions intended for different applications, including at least one FD-SOI region for digital applications and at least one RF-SOI region for radiofrequency applications.

In order to be able to combine an FD-SOI region and an RF-SOI region in one and the same structure, the intermediate layer I is arranged between the first and second electrically insulating layers 3, 5, and the nature of this intermediate layer I is different depending on whether it is in an FD-SOI region or in an RF-SOI region.

One of the two FD-SOI regions of the structure of Figure 1 is shown in Figure 2.

In an FD-SOI region, the intermediate layer I is a semiconductor layer 4.

The intermediate semiconductor layer 4 is advantageously made of a crystalline material or of an amorphous material, which may optionally be doped. This material is chosen so that the semiconductor layer may be biased in order to control the threshold voltage of the transistor.

The material of the intermediate semiconductor layer 4 is advantageously a semiconductor preferably chosen from: single-crystal silicon, polysilicon, and an alloy of Si and Ge.

The FD-SOI region comprises at least one digital component 11 in the active semiconductor layer 6. In Figure 1, the digital component is thus positioned plumb with the semiconductor layer.

The RF-SOI region of the structure of Figure 1 is shown in Figure 3.

In an RF-SOI region, the intermediate layer 1 is an electrically insulating layer 7, called the third electrically insulating layer.

The third electrically insulating layer 7 allows the active semiconductor layer 6 to be better isolated from the carrier substrate 2, i.e. the front gate to be electrically isolated from the back gate of the transistor.

The third electrically insulating layer 7 is preferably a layer of oxide. Since this layer is buried in the structure between the first and second electrically insulating layers, it may be called the “third BOX”. It is preferably a layer of silicon oxide.

The RF-SOI region comprises at least one radiofrequency component 12 plumb with the third electrically insulating layer 7, in particular in the active semiconductor layer 6. The radiofrequency component 12 may also be formed in one of the electrically insulating layers 5, 7 or 3, and preferably on the electrically insulating layer 5, in order to benefit from the effect of a BOX composed of three electrically insulating layers 5, 7 and 3. In Figure 3, the radiofrequency component is thus positioned plumb with the third electrically insulating layer.

According to one preferred embodiment, the sum of the thicknesses of the first electrically insulating layer 3, of the second electrically insulating layer 5, and of the third electrically insulating layer 7 is comprised between 50 nm and 1500 nm. The thickness of each of the three electrically insulating layers is therefore adjusted to obtain the described total thickness. Such a thickness allows the breakdown voltage to be optimized for the radiofrequency components.

Three embodiments of a process for fabricating a multilayer structure 1 such as described above will now be described.

According to a first embodiment, a first donor substrate is initially provided.

A weakened zone is formed in the substrate, so as to delineate an intermediate first semiconductor layer. The weakened zone is formed in the donor substrate at a predefined depth that corresponds substantially to the thickness of the semiconductor layer to be transferred. Preferably, the weakened zone is created by implanting hydrogen and/or helium atoms into the donor substrate.

The intermediate first semiconductor layer is then transferred to a semiconductor carrier substrate, which is a receiver substrate, by bonding the donor substrate to the carrier substrate via the first electrically insulating layer then by detaching the donor substrate along the weakened zone (Smart Cut™ process).

Alternatively, the transfer may be achieved by thinning the donor substrate from the side thereof opposite the side bonded to the carrier substrate, until the thickness desired for the intermediate first semiconductor layer is obtained.

Optionally, before the bonding step, a charge-trapping layer is formed on the carrier substrate, between the carrier substrate and the first electrically insulating layer.

As illustrated in Figure 4, an intermediate structure comprising the carrier substrate 2, the charge-trapping layer 8 when present, the first electrically insulating layer 3 and the transferred intermediate first semiconductor layer I is then obtained.

With reference to Figure 5, one segment of the intermediate first semiconductor layer is then removed down to the first electrically insulating layer in order to form a cavity 9. In

Figure 5, the cavity 9 is bounded in the thickness of the structure by the first electrically insulating layer 3, and laterally by two segments of the intermediate first semiconductor layer 4.

The local removal may advantageously be carried out by etching. To this end, a lithography mask is deposited on the intermediate first semiconductor layer 4. The mask is provided with at least one aperture. The intermediate first semiconductor layer is then etched through the aperture of the mask in order to form the cavity 9. Any known etching technique suitable for this purpose may be used, such as for example dry etching.

With reference to Figure 6, the third electrically insulating layer 7 is then deposited in the cavity 9, in order to fill the cavity. After this deposition, the upper surface of the third electrically insulating layer lies flush with the upper surface of the semiconductor layer.

Moreover, a second donor substrate is provided.

A weakened zone is formed in the substrate, so as to delineate a second semiconductor layer 6. The weakened zone may be formed in the same way used to delineate the intermediate first semiconductor layer.

The second semiconductor layer 6 is then transferred to the intermediate structure, by bonding the second donor substrate to the intermediate structure via the second electrically insulating layer 5 (formed either on the intermediate structure or on said donor substrate) then by detaching the donor substrate along the weakened zone (Smart Cut™ process).

Alternatively, the transfer may be achieved by thinning the second donor substrate from the side thereof opposite the side bonded to the intermediate structure, until the thickness desired for the second semiconductor layer 6 is obtained.

Optionally, before the transferring step, it is possible to carry out a treatment of the free surfaces of the intermediate first semiconductor layer and of the third electrically insulating layer, in order to decrease the roughness thereof. This surface treatment improves the bonding of the second electrically insulating layer to the intermediate first semiconductor layer and third electrically insulating layer.

Next, one or more digital components 11 are produced on the second semiconductor layer 6, which is the active semiconductor layer. The digital components are produced plumb with the intermediate first semiconductor layer, i.e. facing the intermediate first semiconductor layer in the direction of the thickness of the structure. This allows an FD-SOI region to be obtained.

One or more radiofrequency components 12 are also produced on the active semiconductor layer, plumb with the third electrically insulating layer 7. This allows an RF-SOI region to be obtained.

The first embodiment that has just been described comprises two steps of delineating and transferring a semiconductor layer. This is most particularly advantageous in the case

where the intermediate first semiconductor layer is crystalline. The transfer of such a layer from a donor substrate allows its crystal quality to be preserved on the final structure.

When an optimization of the crystal quality of the intermediate first semiconductor layer is not required, for example when the latter is amorphous, it is possible to form the intermediate first semiconductor layer by deposition on the first electrically insulating layer. This process then employs only a single transferring step, i.e. the step of transferring the active semiconductor layer, and is therefore more economical.

This method corresponds to a second embodiment that will now be described.

According to a second embodiment, an intermediate structure, as illustrated in Figure 4, is formed by depositing an intermediate first semiconductor layer 4 on a carrier substrate 2 covered beforehand with a first electrically insulating layer 3.

The intermediate first semiconductor layer 4 may be formed by epitaxy on the carrier substrate covered with a first electrically insulating layer, or alternatively deposited on said carrier substrate in particular by chemical vapour deposition (CVD).

Optionally, before the deposition of the intermediate first semiconductor layer, a charge-trapping layer 8 is formed on the carrier substrate 2, between the carrier substrate and the first electrically insulating layer 3.

With reference to Figure 5, one segment of the intermediate first semiconductor layer 4 is then removed down to the first electrically insulating layer 3 in order to form a cavity 9. In Figure 5, the cavity 9 is bounded in the thickness of the structure by the first electrically insulating layer 3, and laterally by two segments of the intermediate first semiconductor layer 4.

The local removal may advantageously be carried out by etching, similarly to the first embodiment.

With reference to Figure 6, an electrically insulating layer 5 called the third electrically insulating layer, is then deposited in the cavity 9, in order to fill the cavity. After this deposition, the upper surface of the third electrically insulating layer 7 lies flush with the upper surface of the intermediate semiconductor layer 4.

Moreover, a donor substrate is provided.

A weakened zone is formed in the substrate, so as to delineate a second semiconductor layer 6. The weakened zone may be formed in the same way used for the first embodiment.

The second semiconductor layer 6 is then transferred to the intermediate structure, by bonding the donor substrate to the intermediate structure via the second electrically insulating layer 5 then by detaching the donor substrate along the weakened zone (Smart Cut™ process).

Alternatively, the transfer may be achieved by thinning the donor substrate from the side thereof opposite the side bonded to the intermediate structure, until the thickness desired for the second semiconductor layer 6 is obtained.

Optionally, before the transferring step, it is possible to carry out a treatment of the free surfaces of the intermediate first semiconductor layer 4 and of the third electrically insulating layer 7, in order to decrease the roughness thereof. This surface treatment improves the bonding of the second electrically insulating layer to the intermediate first semiconductor layer and third electrically insulating layer.

Next, one or more digital components 11 are produced on the second semiconductor layer 6, which is the active semiconductor layer. The digital components 11 are produced plumb with the intermediate first semiconductor layer 4. This allows an FD-SOI region to be obtained.

One or more radiofrequency components 12 are also produced on the active semiconductor layer, plumb with the third electrically insulating layer 7. This allows an RF-SOI region to be obtained.

According to a third embodiment, the fabricating process comprises the same steps as those of the first embodiment or those of the second embodiment. However, contrary to the latter embodiments, in which the local removal of a segment of the intermediate first semiconductor layer 4 and the deposition of the third electrically insulating layer 7 in the cavity 9 are carried out before the transfer of the second semiconductor layer 6 to the intermediate structure, the removing and depositing steps are carried out after the transferring step.

In particular, the removing and depositing steps according to the third embodiment could be carried out on a structure in which a third electrically insulating layer 7 has been formed beforehand, according to the first or second embodiment described above.

The removing and depositing steps of the third electrically insulating layer 7 may be carried out before the digital and radiofrequency components 11, 12 are produced, or indeed after the digital and radiofrequency components are produced, i.e. during the fabrication of the transistor. It may in particular be a question of MOS transistor, such as a CMOS transistor.

According to this third embodiment, with reference to Figures 7 and 8, a trench 10 is dug at a defined distance from the edge of the structure, so that the trench extends from the free surface of the active semiconductor layer 6, through the second electrically insulating layer 5 and the intermediate first semiconductor layer 4, down at least to the first electrically insulating layer 3. This allows the lateral segment delineated by the trench 10 to be physically isolated from the rest of the structure.

With reference to Figure 9, the intermediate first semiconductor layer 4 in the lateral segment is then locally removed in order to form a cavity 9.

As shown in Figure 9, said cavity 9 is a lateral cavity, located on the edge of the useful zone, and opens onto the exterior of the structure. It is bounded in the thickness of the structure by the first electrically insulating layer 3 and the second electrically insulating layer 5, and laterally by the one or more trenches 10.

With reference to Figure 10, the third electrically insulating layer 7 is then deposited in the cavity 9, in order to fill the cavity.

One or more radiofrequency components 12 may then be produced on the active semiconductor layer 6, plumb with the third electrically insulating layer 7. An RF-SOI region is then obtained on the structure edge.

The advantage of producing the third electrically insulating layer during the process for fabricating the transistor is that it makes it possible to use the etch masks of this process, and therefore to benefit from an optimal alignment of the various layers of the structure.

CLAIMS

1. Semiconductor-on-insulator multilayer structure, comprising in succession from a back side to a front side of the structure:
   - a semiconductor carrier substrate having an electrical resistivity comprised between 500 Ω.cm and 30 kΩ.cm,
   - a first electrically insulating layer,
   - an intermediate layer,
   - a second electrically insulating layer, which has a thickness smaller than that of the first electrically insulating layer,
   - an active semiconductor layer,

   the multilayer structure being characterized in that it comprises:
   - at least one FD-SOI region, in which the intermediate layer is a semiconductor layer,
   - at least one RF-SOI region, adjacent to the FD-SOI region, in which the intermediate layer is a third electrically insulating layer, said RF-SOI region comprising at least one radiofrequency component plumb with the third electrically insulating layer.

2. Structure according to Claim 1, wherein the sum of the thicknesses of the first electrically insulating layer, of the second electrically insulating layer, and of the third electrically insulating layer is comprised between 50 nm and 1500 nm.

3. Structure according to Claim 1 or Claim 2, furthermore comprising a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer.

4. Structure according to Claim 3, wherein the charge-trapping layer is made of polysilicon or of porous silicon.

5. Structure according to one of Claims 1 to 4, wherein the intermediate semiconductor layer is made of crystalline or polycrystalline material.

6. Structure according to one of Claims 1 to 4, wherein the intermediate semiconductor layer is made of amorphous material.

7. Structure according to one of the preceding claims, wherein the first electrically insulating layer is a layer of silicon oxide.

8. Structure according to one of the preceding claims, wherein the second electrically insulating layer is a layer of silicon oxide.

9. Structure according to one of the preceding claims, wherein the third electrically insulating layer is a layer of silicon oxide.

10. Structure according to one of the preceding claims, wherein the first electrically insulating layer has a thickness comprised between 20 nm and 1000 nm.

11. Structure according to one of the preceding claims, wherein the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm.

12. Structure according to one of the preceding claims, wherein the active semiconductor layer has a thickness comprised between 3 nm and 30 nm.

13. Process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:
    - providing a first donor substrate,
    - forming a weakened zone in said first donor substrate, so as to delineate an intermediate first semiconductor layer,
    - transferring said intermediate first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form an intermediate structure comprising the carrier substrate, the first electrically insulating layer and the transferred intermediate first semiconductor layer,
    - locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
    - depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
    - providing a second donor substrate,
    - forming a weakened zone in said second donor substrate, so as to delineate an active second semiconductor layer,
    - transferring said active second semiconductor layer to the intermediate structure, a second electrically insulating layer being at the interface between the second donor substrate and the intermediate structure,
    - producing:
        - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and

- at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

14. Process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:
    - forming an intermediate structure by depositing an intermediate first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
    - locally removing one segment of the intermediate first semiconductor layer down to the first electrically insulating layer in order to form a cavity,
    - depositing an electrically insulating layer, called the third electrically insulating layer, in the cavity,
    - providing a donor substrate,
    - forming a weakened zone in said donor substrate, so as to delineate an active second semiconductor layer,
    - transferring said active second semiconductor layer to the intermediate structure, a second electrically insulating layer being at the interface between the donor substrate and the intermediate structure,
    - producing:
        - at least one digital component in the active second semiconductor layer plumb with the intermediate first semiconductor layer, in order to form an FD-SOI region, and
        - at least one radiofrequency component plumb with the third electrically insulating layer, in order to form an RF-SOI region.

15. Process according to Claim 13 or Claim 14, wherein the local removal of a segment of the intermediate first semiconductor layer and the deposition of a third electrically insulating layer in the cavity are carried out after the transfer of the active second semiconductor layer to the intermediate structure.

16. Process according to one of Claims 13 to 15, furthermore comprising forming a charge-trapping layer on the carrier substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer.

17. Process according to one of Claims 13 to 15, wherein the local removal comprises depositing a mask by lithography and etching the intermediate first semiconductor layer through at least one aperture of said mask.

18. Process according to one of Claims 13 to 15, furthermore comprising, before the transfer of said active second semiconductor layer to the intermediate structure,

treating the free surfaces of the intermediate first semiconductor layer and the third electrically insulating layer in order to decrease the roughness thereof.