# ASYMMETRICAL TRANSISTOR DEVICE AND METHOD OF FABRICATION

## CROSS-REFERENCES TO RELATED APPLICATIONS

**[0001]** This application is a divisional application of co-pending U.S. Patent Application Serial No. 12/550,407 filed August 31, 2009. The application is hereby incorporated by reference in their entireties.

## FIELD OF THE INVENTION

**[0002]** The present invention relates to a semiconductor device and to a method of fabricating the same. More particularly, the invention relates to a semiconductor device having a buried insulating layer and a method of fabricating the same.

## DESCRIPTION OF THE RELATED ART

**[0003]** Semiconductor integrated circuits typically comprise a large number of MOS transistor devices. As the feature size of devices continues to decrease, a variety of phenomena can limit a performance of the devices, such as a value of a switching speed, a leakage current or any other suitable performance parameter.

**[0004]** FIG. 1 is a schematic illustration of a known MOS device 5. The device 5 has a source region 10, a drain region 30 and a channel region 20 between the source and drain regions 10, 30. A source side depletion region 12 is formed at a junction between the source region 10 and adjacent semiconductor material including the channel region 20. A drain side depletion region 32 is formed at a junction between the drain portion 30 and adjacent semiconductor material including the channel region 20.

**[0005]** The presence of the depletion regions 12, 32 introduces a capacitance between the source and channel regions 10, 20 and between the drain and channel regions 30, 20 known as a

'junction capacitance'. The junction capacitance can limit the performance of the transistor device.

**[0006]** In the course of normal operation of the MOS device, junctions between the source and channel regions 10, 20 and between the drain and channel regions 30, 20 are reverse biased. A size of the depletion regions 12, 32 increases as the magnitude of the respective reverse bias potentials increases, thereby decreasing the junction capacitance.

**[0007]** The source side depletion region 12 is typically narrower than the drain side depletion region 32. Thus capacitance introduced by the source side depletion region 12 typically dominates the junction capacitance.

## SUMMARY OF THE INVENTION

**[0008]** Embodiments of the invention seek to mitigate at least some of the above mentioned problems.

**[0009]** Some embodiments of the invention provide a MOS transistor device structure having a decreased junction capacitance between the source and drain regions.

**[0010]** Some embodiments of the invention provide a MOS transistor having a reduced short channel effect.

**[0011]** In accordance with an embodiment of the invention there is provided a semiconductor device comprising: a semiconductor substrate; a source region, a drain region and a channel region, the channel region being provided between the source and drain regions, the source, drain and channel regions being provided in the substrate, the device having a layer of a buried insulating medium provided below the source region and not below the drain region, the layer of buried insulating medium below the source region being provided in abutment with a lower surface of the source region.

**[0012]** This has the advantage that a magnitude of a junction capacitance of the device associated with the source region may be reduced.

**[0013]** Furthermore, since the buried insulating medium does not extend under the drain region a thermal conductivity between the drain region and surrounding material is enhanced. This is at least in part because the buried insulating medium portion of the substrate has a lower thermal conductivity than semiconducting portions of the substrate. Thus, heat generated by current flow in the source, channel and drain regions may be dissipated more readily in structures according to embodiments of the invention than a structure in which the BOX layer extends under the source, channel and drain regions.

**[0014]** Optionally, the layer of insulating medium extends below the channel region. This has the advantage that a reduction in the junction capacitance under the gate electrode ($C_{jswg}$) may be achieved.

**[0015]** It is to be understood that a semiconductor device according to embodiments of the invention may be considered to have an asymmetrical structure since the buried insulating medium is provided below the source region but does not extend under the drain region.

**[0016]** In a second aspect of the invention there is provided a method of fabricating a semiconductor device comprising: providing a semiconductor substrate; forming a source region, a drain region and a channel region in the substrate, the channel region being provided between the source and drain regions, and providing a layer of a buried insulator material below the source region and not below the drain region, the buried insulator material being provided in abutment with a lower surface of the source region.

**[0017]** Some embodiments of the invention have the advantage that a magnitude of a junction capacitance between the source and drain regions of the transistor device may be reduced relative to known transistor devices.

**[0018]** In a third aspect of the invention there is provided a semiconductor device comprising: a semiconductor substrate comprising an upper semiconductor portion formed from silicon and a lower semiconductor portion formed from silicon, the upper and lower portions being separated by a layer of a buried oxide (BOX) medium; a source region, a drain region and a channel region provided in the upper semiconductor portion, the channel region being provided between the source and drain regions, wherein the BOX medium is provided below the source region and the channel region and not below the drain region, the BOX medium being provided in abutment with a lower surface of the source region.

**[0019]** In an aspect of the invention there is provided a method of fabricating a semiconductor device comprising: providing a semiconductor substrate; forming a source region, a drain region and a channel region in the substrate, the channel region being provided between the source and drain regions, a junction between the source and channel regions having a source junction capacitance; and providing a layer of a buried insulator material below the source region and not below the drain region thereby to reduce a value of the source junction capacitance, the buried insulator material being provided in abutment with a lower surface of the source region.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** Embodiments of the present invention will now be described hereinafter, by way of example only with reference to the accompanying drawings, in which:

**[0021]** FIGURE 1 is a schematic illustration of a prior art MOS device.

**[0022]** FIGURES 2 to 10 are schematic illustrations of a process of fabricating a MOS device according to embodiments of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

**[0023]** FIG. 2 shows a structure in which a substrate 101 is provided having a buried oxide (BOX) layer 103. The BOX layer 103 divides the substrate 101 into an upper semiconductor region 102 and a lower semiconductor region 104.

**[0024]** A gate stack is provided above the upper semiconductor region 102 of the substrate 101, the gate stack comprising a gate dielectric layer 141 and a gate electrode layer 142.

**[0025]** The gate dielectric layer 141 is formed from silicon oxide. Other materials are also useful such as silicon nitride, silicon oxynitride and any other suitable dielectric material.

**[0026]** The gate electrode layer 142 is formed from silicon. Other materials are also useful including other semiconductor materials or metallic materials.

**[0027]** A hardmask layer 153 has been formed over the substrate 101 and gate stack. The hardmask layer 153 has been patterned to expose a surface of a portion of the upper semiconductor region 102 of the substrate 101 where a drain region of the MOS device is to be formed. A gate stack spacer 151 has been formed over a sidewall of the gate stack on the side of the gate stack at which the drain region is to be formed.

**[0028]** FIG. 3 shows the structure of FIG. 2 following an etching process in which etching of the substrate 101 is performed in order to remove the exposed portion of the upper semiconductor region 102 and expose a portion of the underlying BOX layer 103. Portions of the upper semiconductor region 102 below the gate stack spacer 151 and hardmask layer 153 remain following the etching process.

**[0029]** FIG. 4 shows the structure of FIG. 3 following an isotropic etching process in which etching of the exposed potion of the BOX layer 103 is performed in order to remove a portion of the BOX layer 103. Because the etching process is isotropic a portion of the BOX layer underlying the gate stack spacer 151 is also removed. This phenomenon may be referred to as 'necking'. The purpose of removing this portion of the BOX layer 103 is to reduce a problem of

current crowding as current flows from the channel region to the drain region of the structure (see below).

**[0030]** FIG. 5 shows the structure of FIG. 4 following an anisotropic (directional) etching process in which a remainder of the BOX layer 103 not underlying the hardmask layer 153 or gate stack spacer 151 is removed. A portion of the lower semiconductor region 104 of the substrate 101 is thereby exposed.

**[0031]** FIG. 6 shows the structure of FIG. 5 following re-growth of semiconductor material over the lower semiconductor region 104. Re-growth of semiconductor material is performed to a level of remaining portions of the upper semiconductor region 102.

**[0032]** FIG. 7 shows the structure of FIG. 6 following removal of the hardmask layer 153 and gate stack spacer 151. The gate dielectric layer 141 and gate electrode layer 142 remain above the upper semiconductor region 102.

**[0033]** FIG. 8 shows the structure of FIG. 7 following a process of forming source and drain extension regions 114, 134 respectively, gate stack sidewall spacers 153 and source and drain regions 110, 130 respectively thereby to form a transistor structure 100. The drain region 130 of the embodiment of FIG. 8 has been formed to a depth below a level of the BOX layer 103 and may be referred to as a deep drain region 130.

**[0034]** In the embodiment of FIG. 8 the source and drain extension regions 114, 134 and source and drain regions 110, 130 are formed by implantation of dopant into the substrate 101. Other methods of introducing dopant into the substrate are also useful.

**[0035]** The extension regions 114, 134 may be of a different dopant concentration to the source and drain regions 110, 130 respectively. The extension regions 114, 134 may be lightly doped regions. The drain extension region may be a lightly doped drain (LDD) region.

**[0036]** FIG. 9 shows a transistor structure 200 similar to that of FIG. 8 except that the portion of the BOX layer 203 below drain extension region 234 has not been etched to form a necked structure.

**[0037]** FIG. 10 shows a transistor structure 300 similar to that of FIG. 9 except that the drain region 330 of the structure of FIG. 10 does not extend below a depth of the BOX layer 303. In the embodiment of FIG. 10 the drain region 330 extends to a depth below an upper surface of the BOX layer 303 but above a lower surface of the BOX layer 303. It is to be understood that the depth to which the drain region 330 extends is dependent at least in part on a depth to which dopant ions are provided.

**[0038]** Other structures are also useful.

**[0039]** FIG. 11 shows a transistor structure 400 similar to that of FIG. 8. Like features are provided with like reference numerals prefixed with the numeral 4 instead of the numeral 1.

**[0040]** The structure of FIG. 11 is provided with a drain stressor portion 432. The drain stressor portion 432 is arranged to induce a strain in the channel region 420 thereby to enhance a performance of the transistor structure 400.

**[0041]** The drain stressor portion 432 may be formed by performing a further etching process to form a drain stressor recess following the step of re-growth of semiconductor material illustrated in FIG. 6 and described above. Drain stressor material may subsequently be formed in the drain stressor recess thereby to form the drain stressor 432.

**[0042]** Embodiments of the present invention have the advantage that a value of junction capacitance of a transistor device may be reduced whilst maintaining a heat dissipative path from the device to a portion of the substrate away from the upper semiconductor layer. This allows a self heating effect associated with devices formed in relatively thin semiconductor layers such as devices formed on silicon on insulator (SOI) structures to be suppressed.

**[0043]** Embodiments of the invention having a necked buried insulator layer such as that shown in FIG. 8 and FIG. 11 have the advantage that current crowding may be reduced thereby enhancing device performance. Provision of the necked portion increases a cross-sectional area of a flow path available for current flowing from the channel region to the drain region thereby decreasing an external series resistance of the device. The feature of a necked buried insulator layer is particularly useful in ultra thin body SOI transistor devices.

**[0044]** Embodiments of the invention having a buried insulator layer extending below the channel region provide a fully depleted SOI structure and have the advantage that short channel effects may be suppressed. This allows elimination of the use of halo/pocket implant structures. Furthermore, a reduction in the junction capacitance under the gate electrode ($C_{jswg}$) may be achieved. $C_{jswg}$ is understood to be a major contributor to parasitic capacitance in advanced CMOS technologies.

**[0045]** Throughout the description and claims of this specification, the words "comprise" and "contain" and variations of the words, for example "comprising" and "comprises", means "including but not limited to", and is not intended to (and does not) exclude other moieties, additives, components, integers or steps.

**[0046]** Throughout the description and claims of this specification, the singular encompasses the plural unless the context otherwise requires. In particular, where the indefinite article is used, the specification is to be understood as contemplating plurality as well as singularity, unless the context requires otherwise.

**[0047]** Features, integers, characteristics, compounds, chemical moieties or groups described in conjunction with a particular aspect, embodiment or example of the invention are to be understood to be applicable to any other aspect, embodiment or example described herein unless incompatible therewith.

What is claimed is:

## CLAIMS

1. A device comprising:

a substrate having an asymmetrical transistor, wherein the asymmetrical transistor comprises

a gate disposed on the substrate having first and second sides,

a source disposed in the substrate on the first side of the gate, and

a drain disposed in the substrate on the second side of the gate, wherein the source and drain are asymmetrical.

2. The device in claim 1 wherein the source and drain comprise different source and drain depths.

3. The device in claim 2 wherein the substrate comprises a buried insulator layer, an upper portion of the substrate is above a top surface of the buried insulator layer and a lower portion is below a bottom surface of the buried insulator layer.

4. The device in claim 3 wherein the source depth of the source is about the top surface of the buried insulator layer and the drain depth of the drain is below the top surface of the buried insulator layer.

5. The device in claim 4 wherein the buried insulator layer comprises an edge being about aligned with the edge of a gate sidewall spacer on the second side of the gate.

6. The device in claim 5 wherein the drain depth of the drain is in the lower portion of the substrate below the bottom surface of the buried insulator layer.

7. The device in claim 6 wherein the edge of the buried insulator layer comprises a recess underlying the gate sidewall spacer on the second side of the gate.

8. The device in claim 5 wherein the edge of the buried insulator layer comprises a recess underlying the gate sidewall spacer on the second side of the gate.

9. The device in claim 8 wherein the drain comprises a stressor.

10. The device in claim 9 wherein the stressor comprises a top stressor surface above a top surface of the substrate.

11. A device comprising:

a substrate having an asymmetrical transistor, wherein the asymmetrical transistor comprises

a gate disposed in the substrate having first and second sides,

a first doped region disposed in the substrate on the first side of the gate, and a second doped region disposed in the substrate on the second side of the gate, wherein the first and second doped regions are asymmetrical.

12. The device in claim 11 wherein the first and second doped regions comprise different depths.

13. The device in claim 12 wherein the first doped region comprises a source of the transistor and the second doped region comprises a drain of the transistor.

14. The device in claim 12 wherein the substrate comprises a first substrate region and a second substrate region separated by a channel region.

15. The device in claim 14 wherein the substrate comprises a buried insulator layer, an upper portion of the substrate is above a top surface of the buried insulator layer and a lower portion of the substrate is below a bottom surface of the buried insulator layer.

16. The device in claim 15 wherein the second substrate region includes a semiconductor material and extends from a top surface of the substrate through the buried insulator layer to a depth below the bottom surface of the buried insulator layer.

17. The device in claim 16 wherein the buried insulator layer is disposed below the first doped region and channel region and not in the second doped region.

18. The device in claim 14 wherein the second substrate region comprises a stressor.

19. The device in claim 14 wherein the stressor comprises a top stressor surface above the substrate.

20. A device comprising:

a substrate having an asymmetrical transistor, wherein the asymmetrical transistor comprises

a gate disposed in the substrate having first and second sides,

a first doped region disposed in the substrate on the first side of the gate, and a second doped region disposed in the substrate on the second side of the gate, wherein the first and second doped regions comprise different depths.