FIG. 1

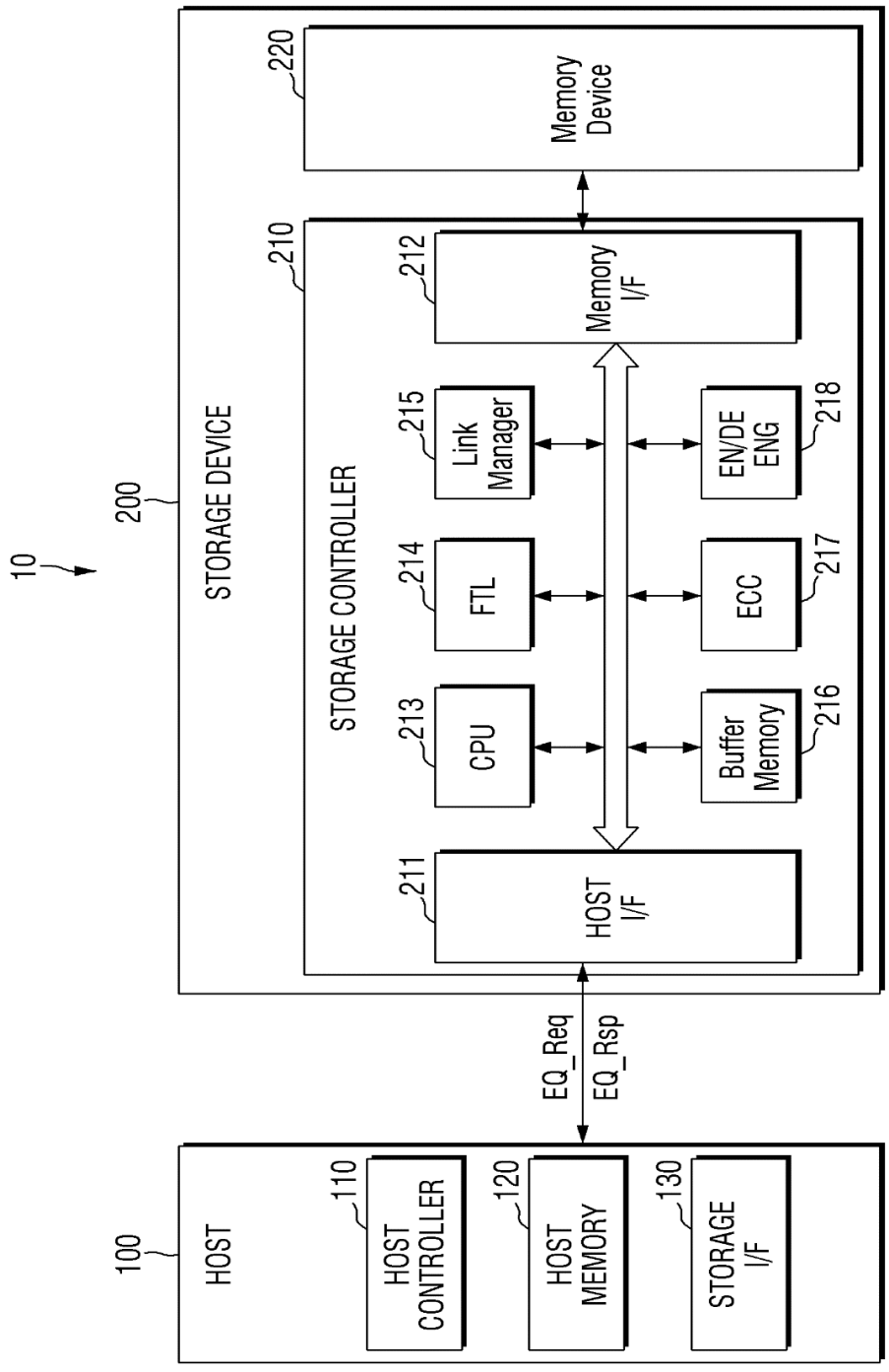

10
100
HOST
110
HOST CONTROLLER
120
HOST MEMORY
130
STORAGE I/F
EQ_Req
EQ_Rsp
200
STORAGE DEVICE
210
STORAGE CONTROLLER
211
HOST I/F
212
Memory I/F
213
CPU
214
FTL
215
Link Manager
216
Buffer Memory
217
ECC
218
EN/DE ENG
220
Memory Device

FIG. 2

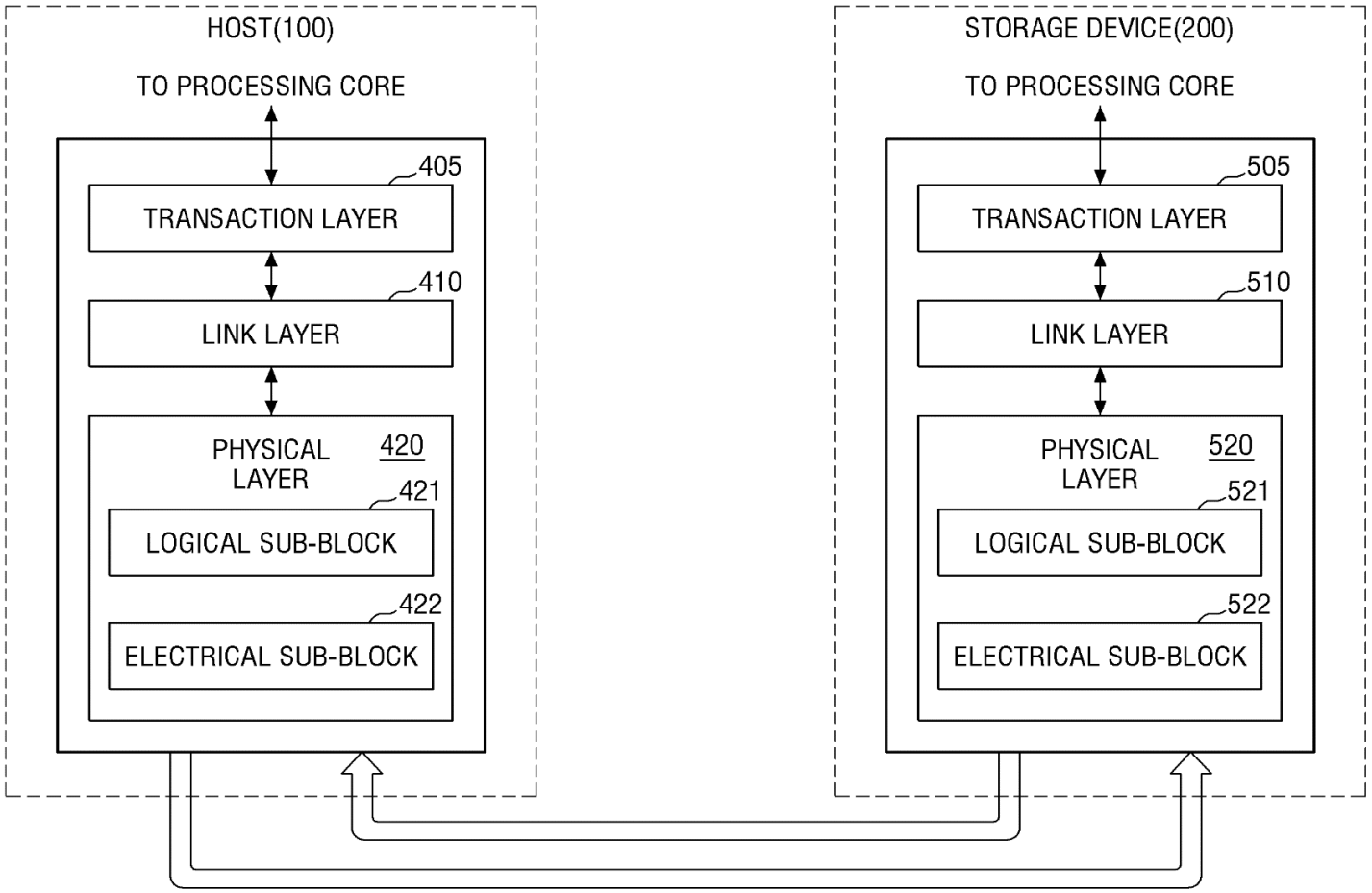

HOST(100)
TO PROCESSING CORE
405
TRANSACTION LAYER
410
LINK LAYER
PHYSICAL LAYER
420
421
LOGICAL SUB-BLOCK
422
ELECTRICAL SUB-BLOCK
STORAGE DEVICE(200)
TO PROCESSING CORE
505
TRANSACTION LAYER
510
LINK LAYER
PHYSICAL LAYER
520
521
LOGICAL SUB-BLOCK
522
ELECTRICAL SUB-BLOCK

FIG. 3

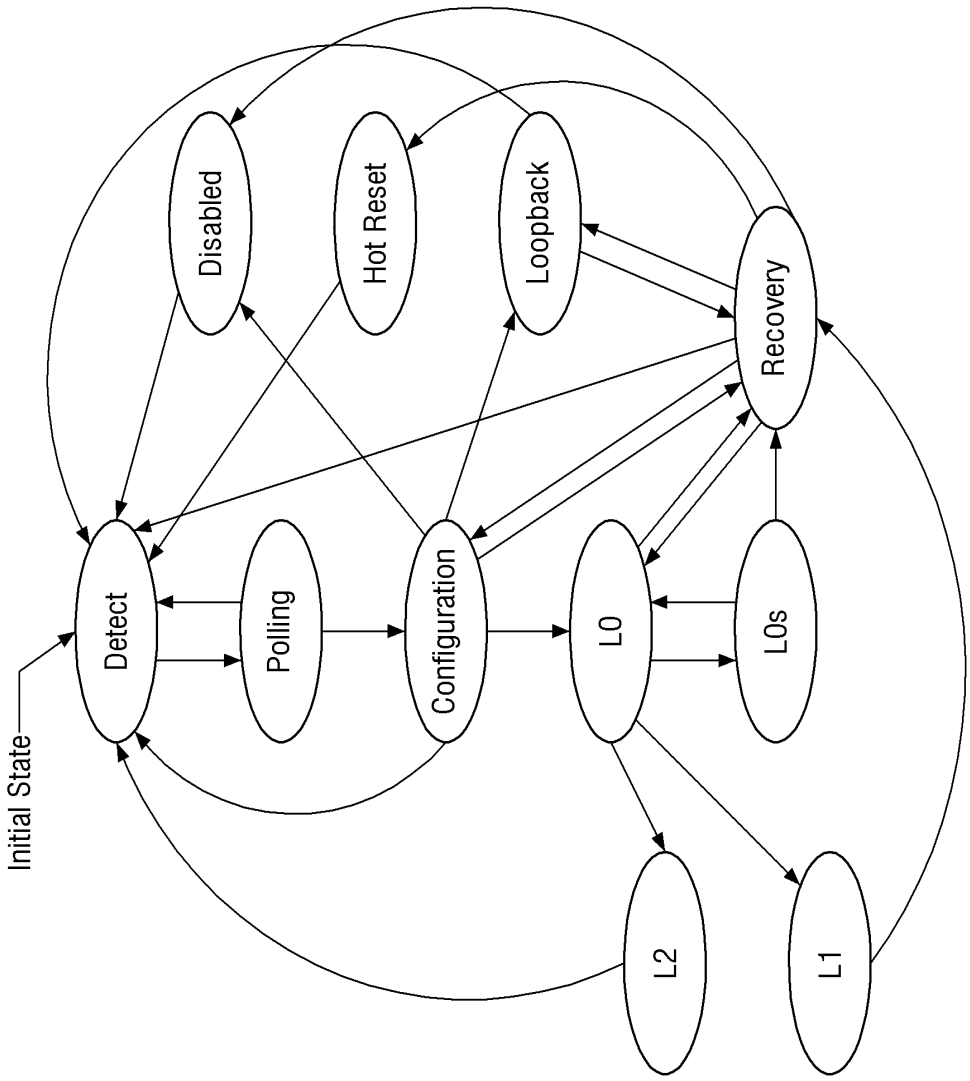

Initial State
Detect
Polling
Configuration
L0
L0s
L1
L2
Recovery
Loopback
Hot Reset
Disabled

FIG. 4

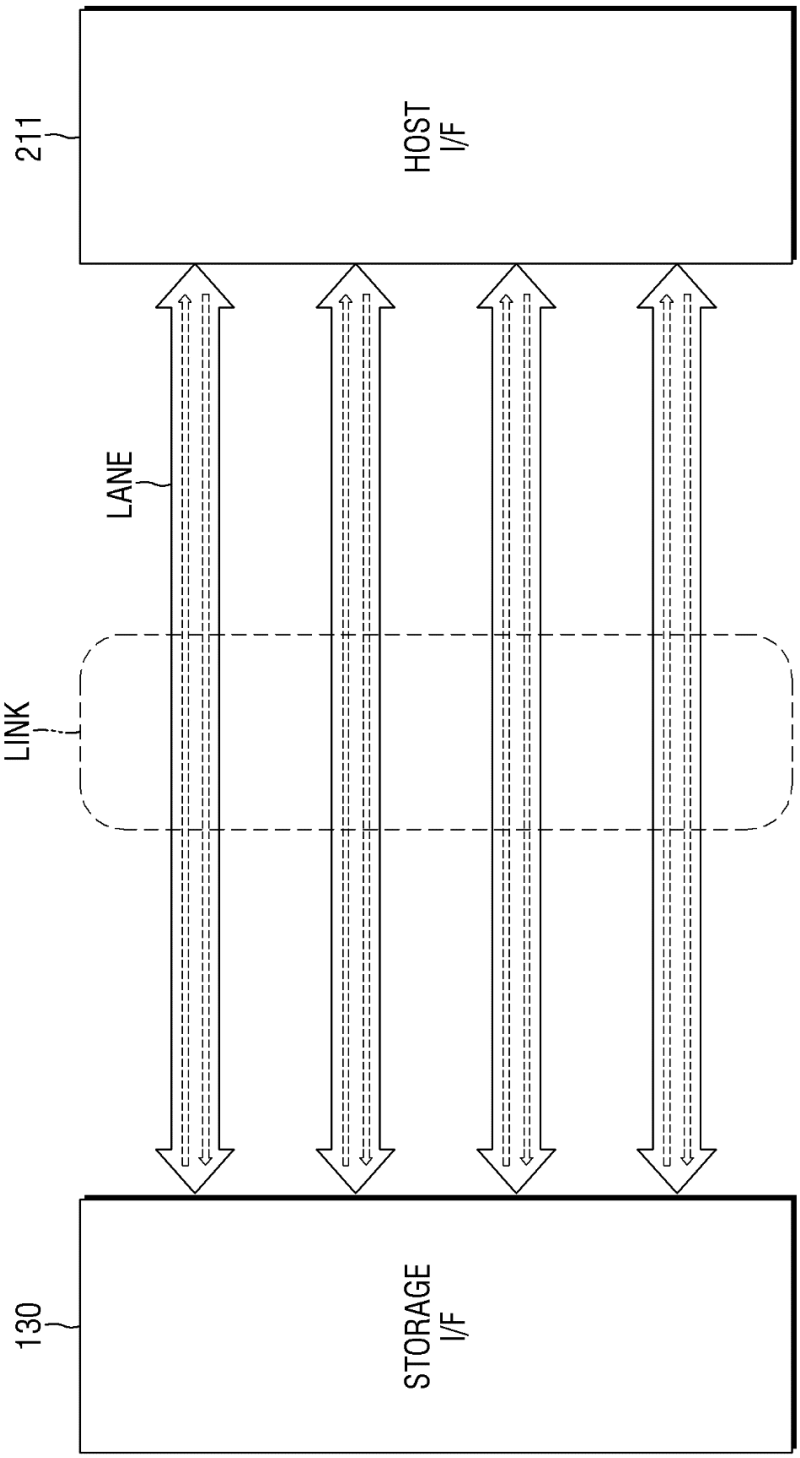


FIG. 5

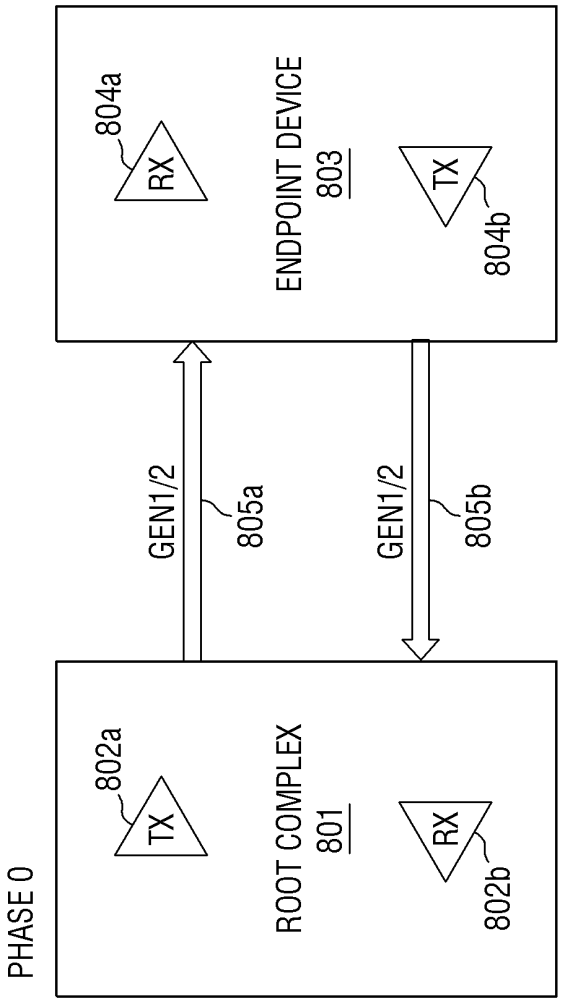

PHASE 0
ROOT COMPLEX
801
802a
TX
802b
RX
GEN1/2
805a
GEN1/2
805b
ENDPOINT DEVICE
803
804a
RX
804b
TX

FIG. 6

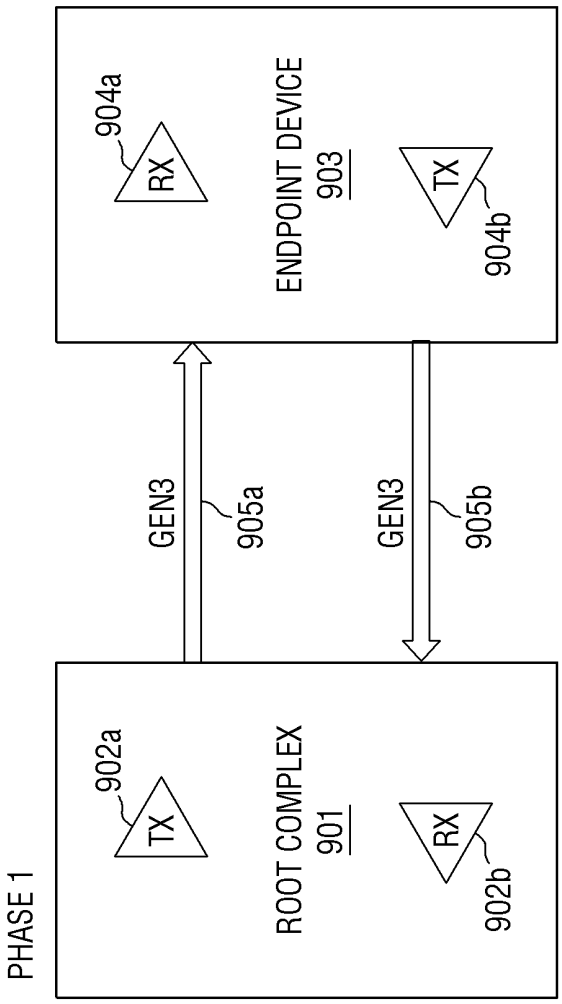

PHASE 1
ROOT COMPLEX
901
902a
TX
902b
RX
GEN3
905a
GEN3
905b
ENDPOINT DEVICE
903
904a
RX
904b
TX

FIG. 7

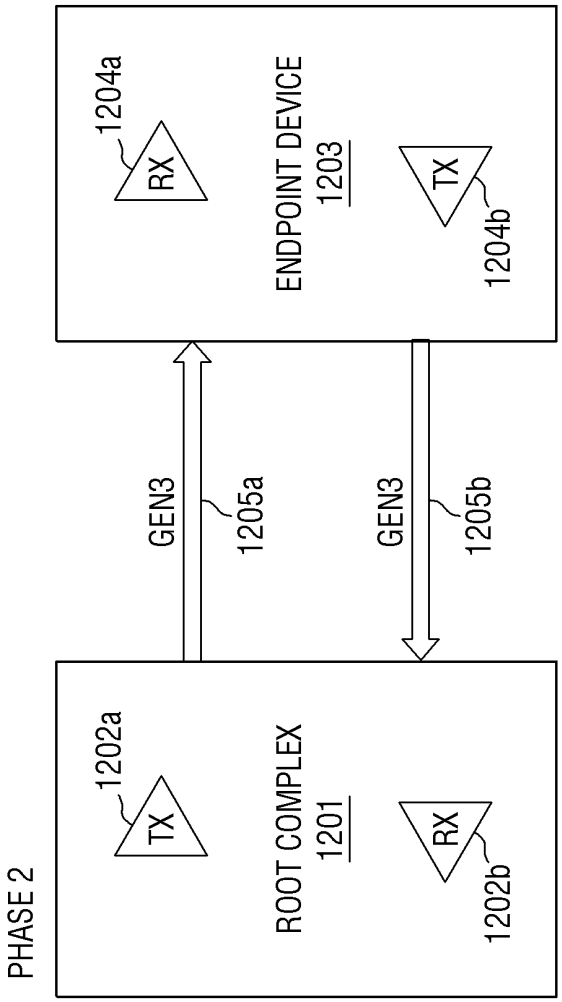

PHASE 2
ROOT COMPLEX
1201
1202a
TX
1202b
RX
GEN3
1205a
GEN3
1205b
ENDPOINT DEVICE
1203
1204a
RX
1204b
TX

FIG. 8

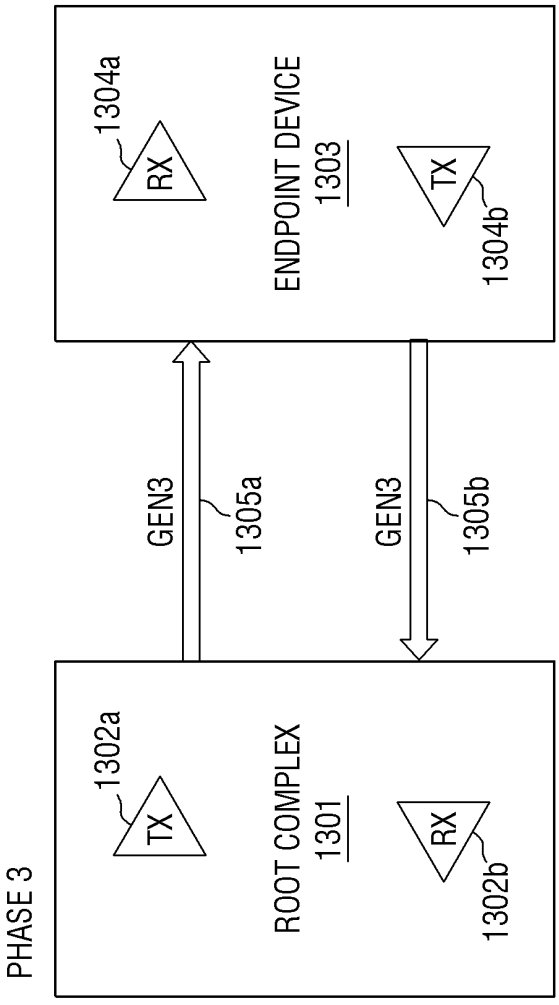

PHASE 3
ROOT COMPLEX
1301
1302a
TX
1302b
RX
GEN3
1305a
GEN3
1305b
ENDPOINT DEVICE
1303
1304a
RX
1304b
TX

FIG. 9

PATH	PORT	LANE	SPEED	HIGH	LOW	RIGHT	PH3_PRECURSOR	PH3_POSTCURSOR
Rx	5	0	Gen3	101	-106	79	1	0
Rx	5	1	Gen3	101	-99	74	1	0
Rx	5	2	Gen3	94	-99	69	1	0
Rx	5	3	Gen3	98	-98	76	2	0
Rx	5	0	Gen3	103	-106	81	1	0
Rx	5	1	Gen3	99	-105	69	1	0
Rx	5	2	Gen3	97	-105	71	1	0
Rx	5	3	Gen3	96	-100	78	2	0
Rx	5	0	Gen3	99	-106	77	1	0
Rx	5	1	Gen3	98	-102	76	1	0
Rx	5	2	Gen3	99	102	70	1	0
Rx	5	3	Gen3	96	-96	79	2	0
Rx	5	0	Gen3	78	-79	50	3	4
Rx	5	1	Gen3	99	-104	72	1	0
Rx	5	2	Gen3	94	-101	74	1	0
Rx	5	3	Gen3	93	-97	80	2	0
• • •								
Rx	5	0	Gen3	81	-82	56	3	4
Rx	5	1	Gen3	95	-104	70	1	0
Rx	5	2	Gen3	98	-99	72	1	0
Rx	5	3	Gen3	95	-98	80	2	0

FIG. 10

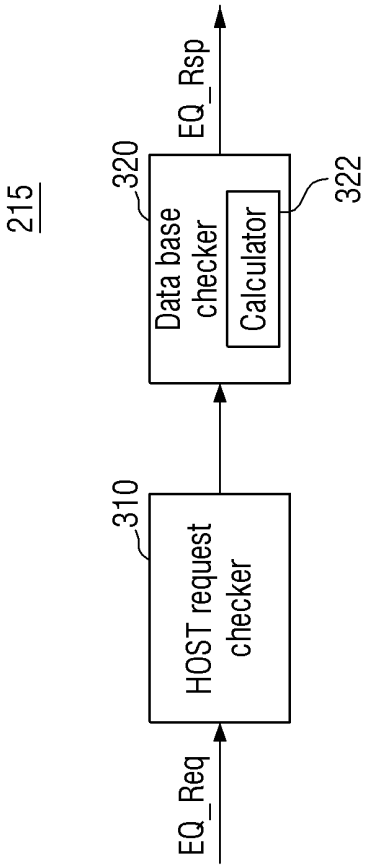

215
EQ_Req
310
HOST request checker
320
Data base checker
Calculator
322
EQ_Rsp

FIG. 11

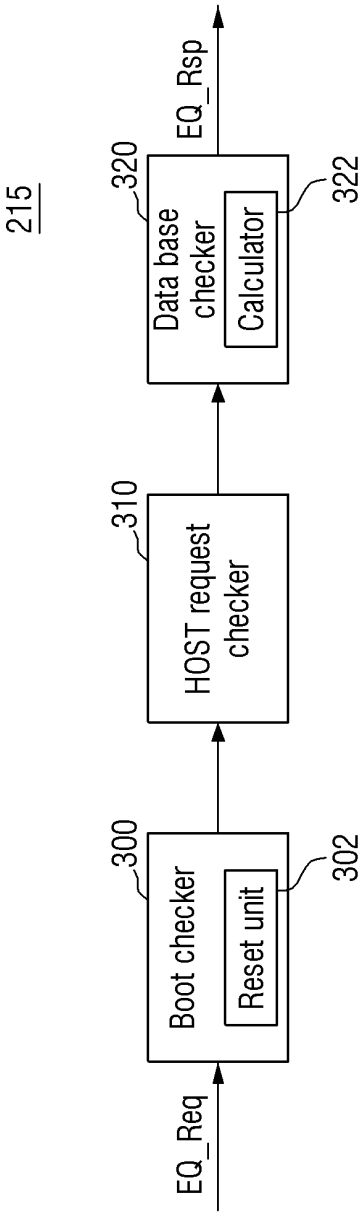

215
EQ_Req
300
Boot checker
Reset unit
302
310
HOST request checker
320
Data base checker
Calculator
322
EQ_Rsp

FIG. 12

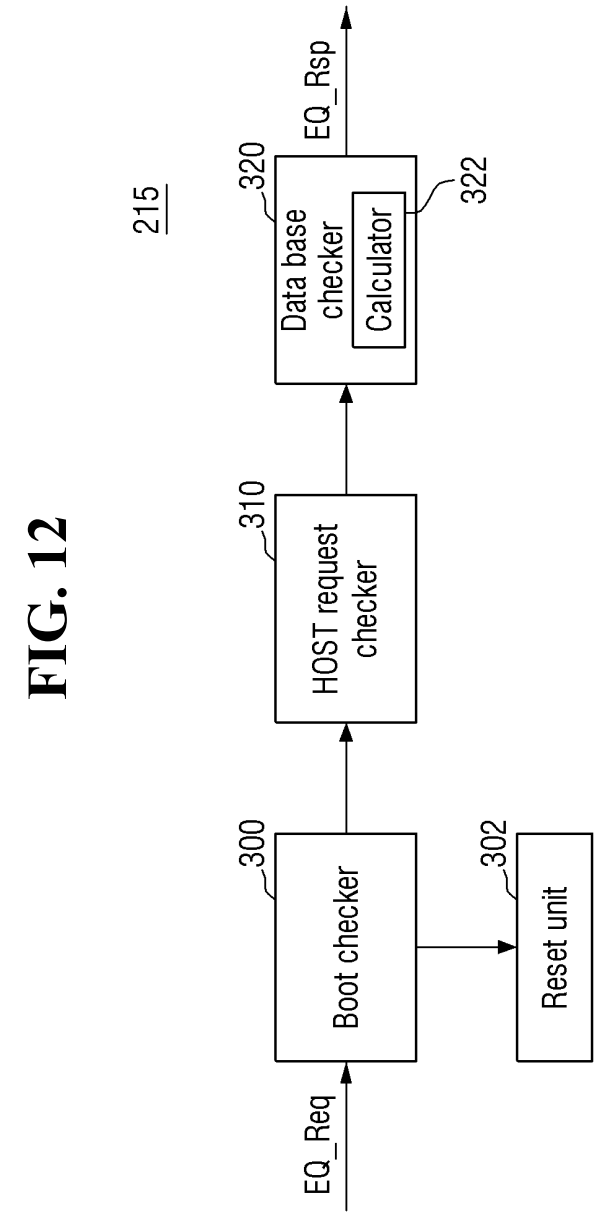

215
EQ_Req
300
Boot checker
302
Reset unit
310
HOST request checker
320
Data base checker
Calculator
322
EQ_Rsp

FIG. 13

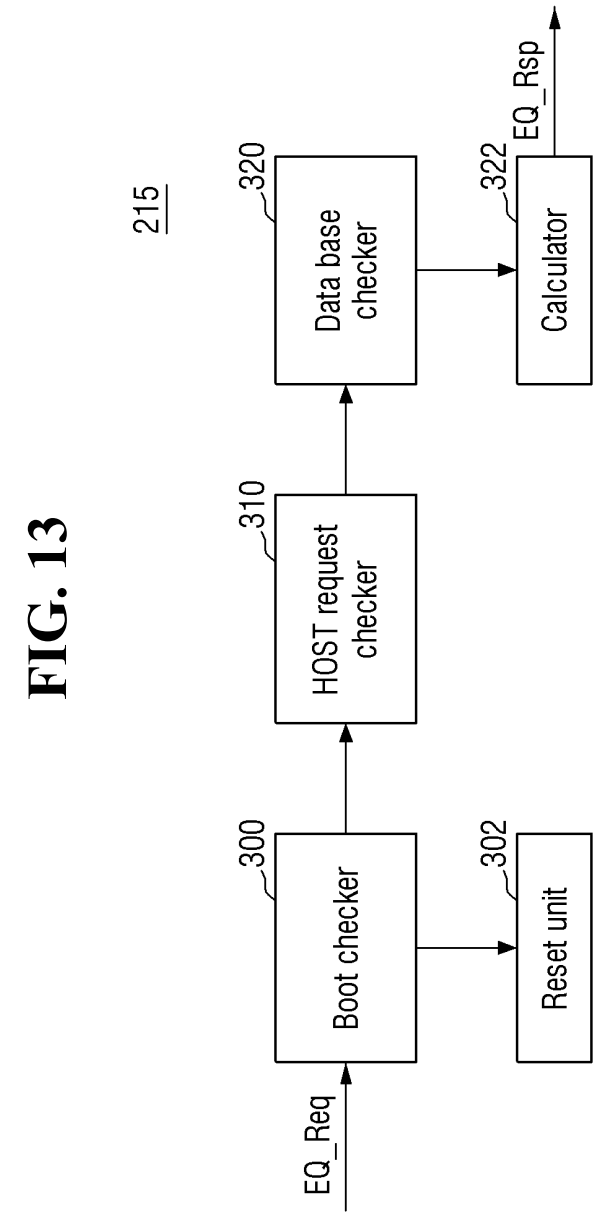

215
EQ_Req
300
Boot checker
302
Reset unit
310
HOST request checker
320
Data base checker
322
Calculator
EQ_Rsp

FIG. 14

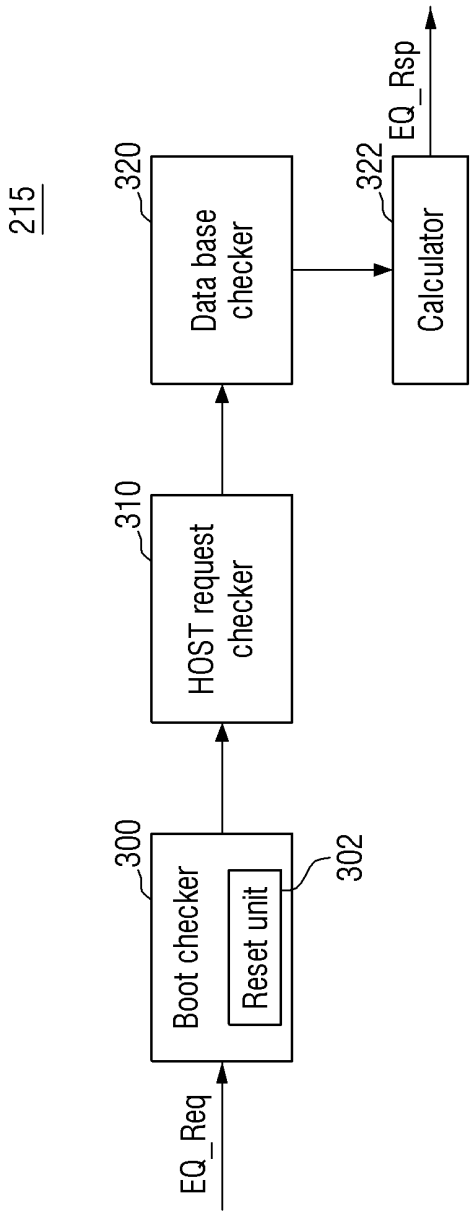

215
EQ_Req
300
Boot checker
Reset unit
302
310
HOST request checker
320
Data base checker
322
Calculator
EQ_Rsp

FIG. 15

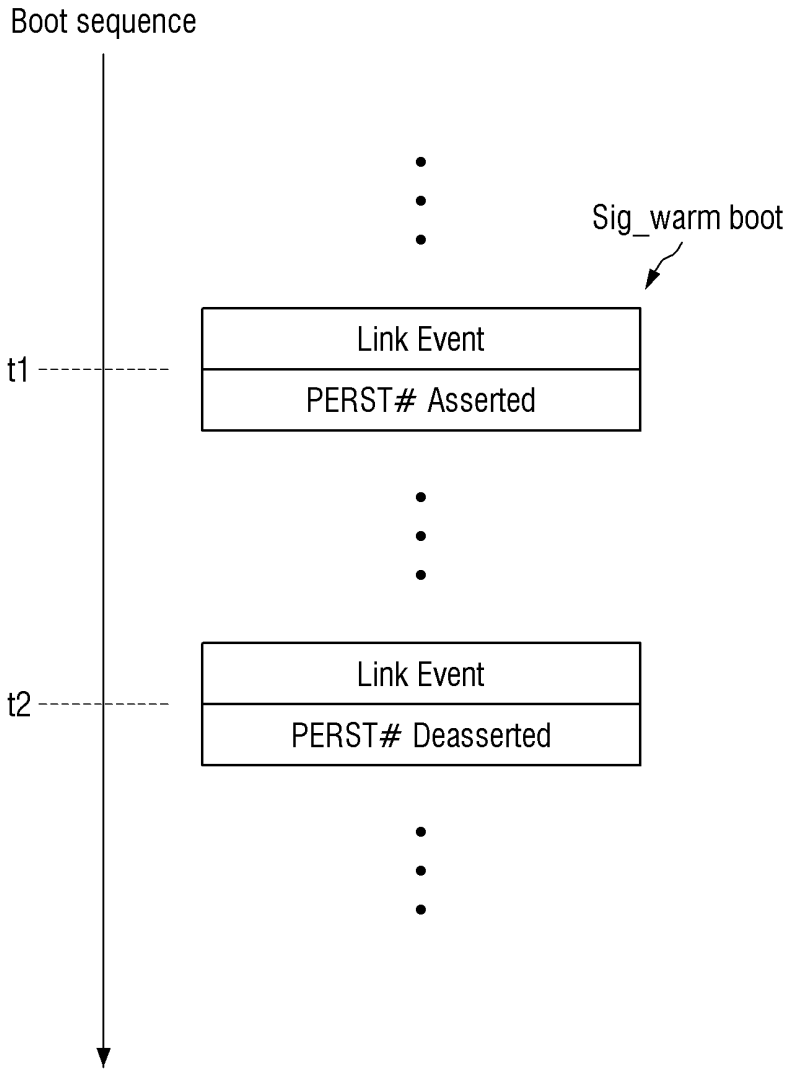

Boot sequence
Sig_warm boot
t1
Link Event
PERST# Asserted
t2
Link Event
PERST# Deasserted

FIG. 16

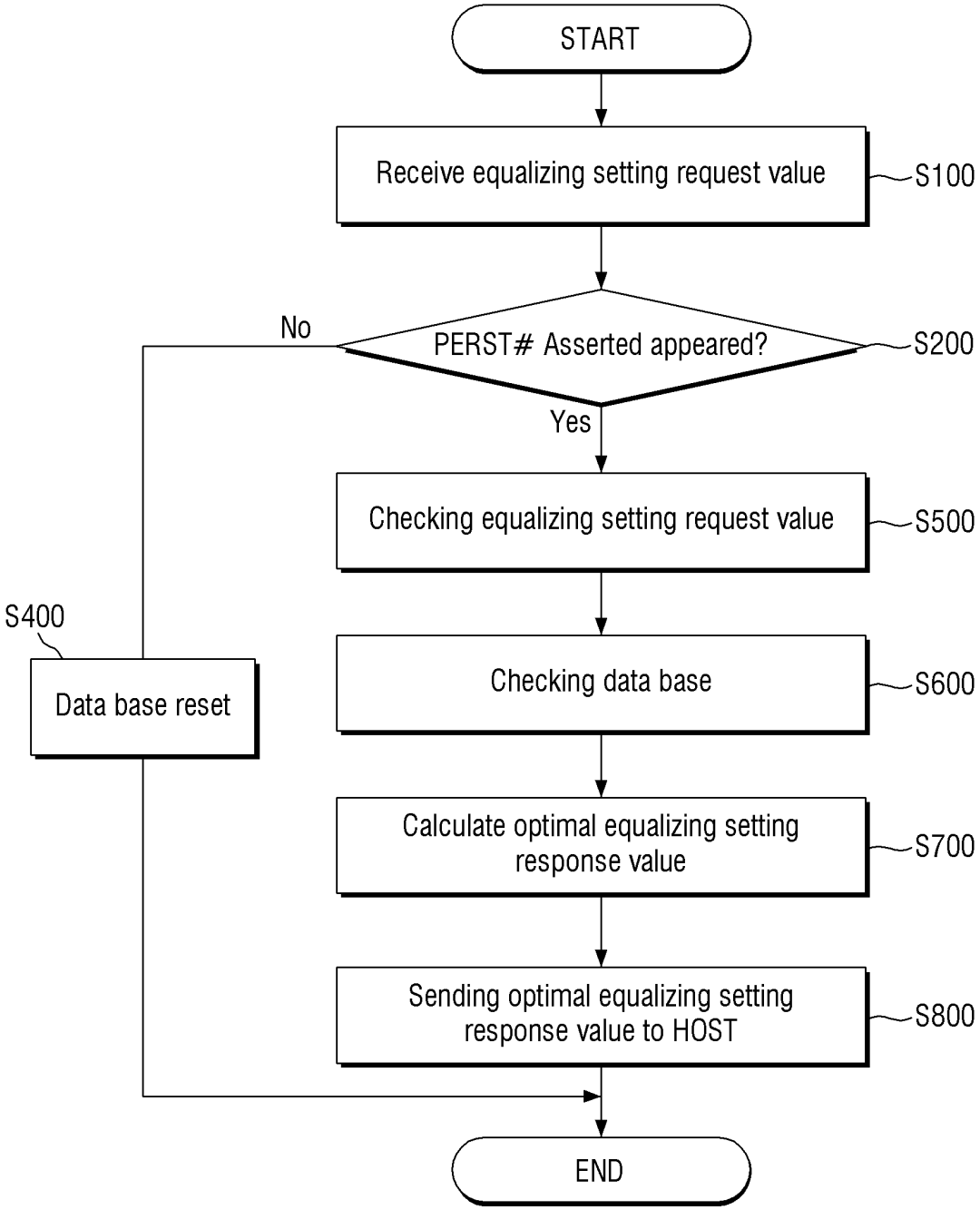

START
Receive equalizing setting request value
S100
No
PERST# Asserted appeared?
S200
Yes
Checking equalizing setting request value
S500
S400
Data base reset
Checking data base
S600
Calculate optimal equalizing setting response value
S700
Sending optimal equalizing setting response value to HOST
S800
END

FIG. 17

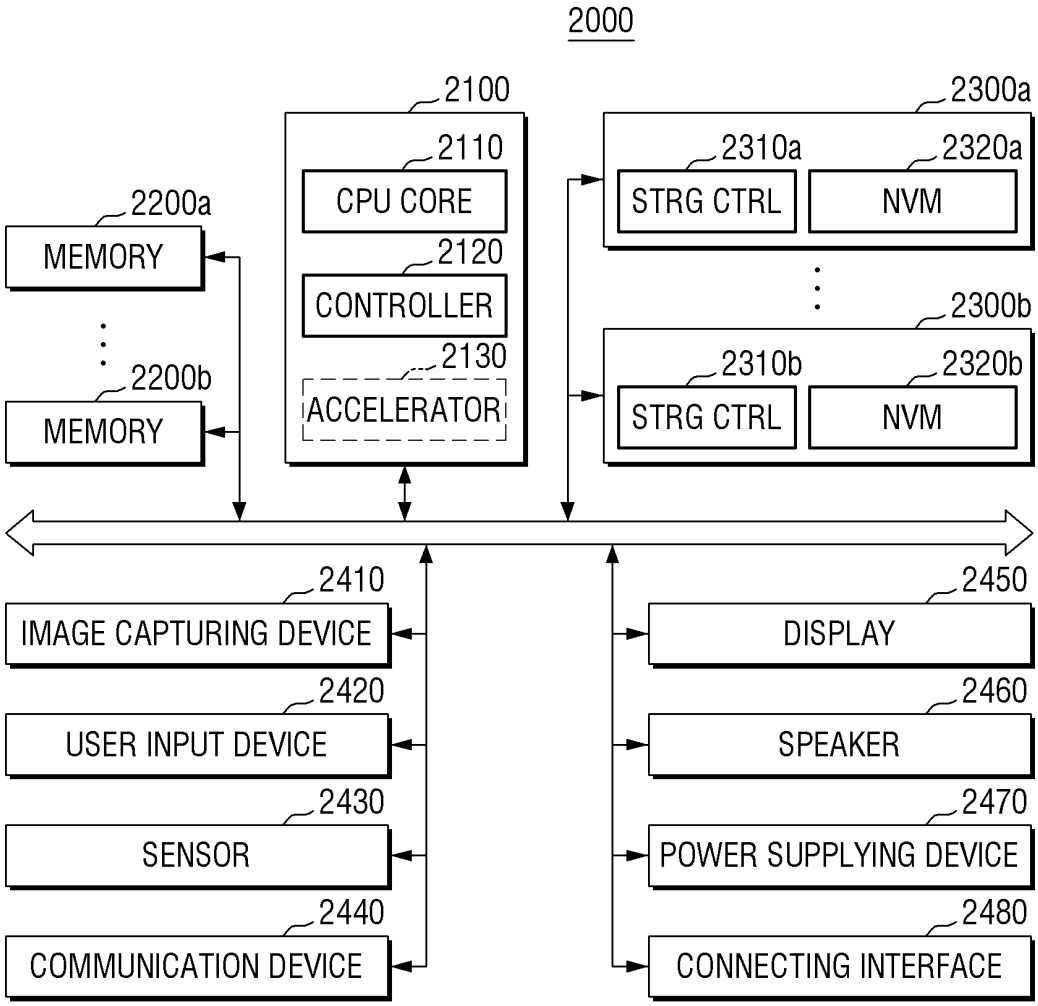
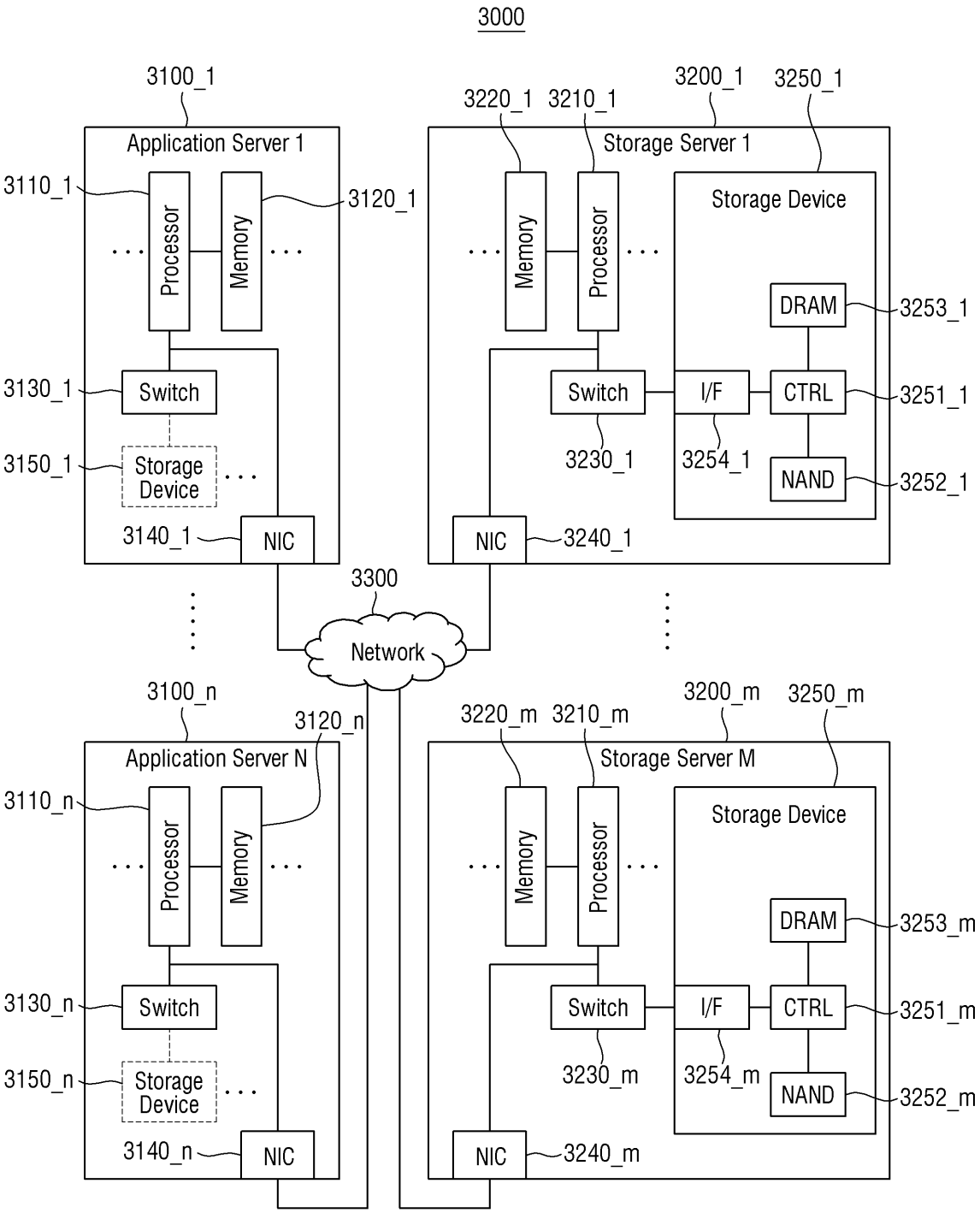

2000
2100
2110
CPU CORE
2120
CONTROLLER
2130
ACCELERATOR
2200a
MEMORY
2200b
MEMORY
2300a
2310a
STRG CTRL
2320a
NVM
2300b
2310b
STRG CTRL
2320b
NVM
2410
IMAGE CAPTURING DEVICE
2420
USER INPUT DEVICE
2430
SENSOR
2440
COMMUNICATION DEVICE
2450
DISPLAY
2460
SPEAKER
2470
POWER SUPPLYING DEVICE
2480
CONNECTING INTERFACE

FIG. 18


3000
3100_1
Application Server 1
3110_1
Processor
Memory
3120_1
3130_1
Switch
3150_1
Storage Device
3140_1
NIC
3220_1
3210_1
3200_1
3250_1
Storage Server 1
Memory
Processor
Storage Device
DRAM
3253_1
Switch
I/F
CTRL
3251_1
3230_1
3254_1
NAND
3252_1
NIC
3240_1
3300
Network
3100_n
Application Server N
3110_n
Processor
Memory
3120_n
3130_n
Switch
3150_n
Storage Device
3140_n
NIC
3220_m
3210_m
3200_m
3250_m
Storage Server M
Memory
Processor
Storage Device
DRAM
3253_m
Switch
I/F
CTRL
3251_m
3230_m
3254_m
NAND
3252_m
NIC
3240_m