TRIPLE-LAYERED LOW DIELECTRIC CONSTANT DIELECTRIC DUAL DAMASCENE APPROACH

ABSTRACT

A triple layered low dielectric constant material dual damascene metallization process is described. Metal lines are provided covered by an insulating layer overlying a semiconductor substrate. A first dielectric layer of a first type is deposited overlying the insulating layer. A second dielectric layer of a second type is deposited overlying the first dielectric layer. A via pattern is etched into the second dielectric layer. Thereafter, a third dielectric layer of the first type is deposited overlying the patterned second dielectric layer. Simultaneously, a trench pattern is etched into the third dielectric layer and the via pattern is etched into the first dielectric layer to complete the formation of dual damascene openings in the fabrication of an integrated circuit device. If the first type is a low dielectric constant organic material, the second type will be a low dielectric constant inorganic material. If the first type is a low dielectric constant inorganic material, the second type will be a low dielectric constant organic material.

Figure 8