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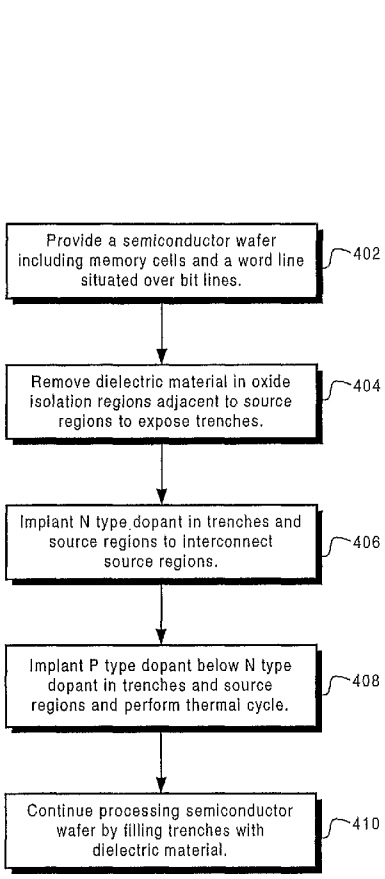
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(54) Title: METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE



(57) Abstract: According to one exemplary embodiment, a method for fabricating a floating gate memory array comprises a step of removing (404) a dielectric material from an isolation region (110) situated in a substrate (258,358) to expose a trench (128,228), where the trench (128,228) is situated between a first source region (116,216,316) and a second source region (118,218), where the trench (128,228) defines sidewalls (150,250) in the substrate (258,358,). The method further comprises implanting (406) an N type dopant in the first source region (116,216,316), the second source region (118,218,318), and the sidewalls (150,250) of the trench (128,228), where the N type dopant forms an N+ type region (252,352). The method further comprises implanting (408) a P type dopant in the first source region (116,216,316), the second source region (118,218), and the sidewalls (150,250) of the trench (128,228), where the P type dopant forms a P type region (256,356), and where the P type region (256,356) is situated underneath the N+ type region (252,352).

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