

SEMICONDUCTOR EQUIPMENT

TECHNICAL FIELD

The present disclosure belongs to the field of semiconductor processing equipment, and particularly relates to semiconductor equipment.

BACKGROUND

A capacitor, as one of the most essential components in a circuit, plays a crucial role in an entire electronic device. With the development of the semiconductor technology, film deposition technology allows nanoscale manufacturing process of electronic components, and becomes a main means for miniaturization and integration of capacitors. The prepared miniaturized capacitors are generally called micro-capacitors.

The micro-capacitor typically includes a planar capacitor and a trench capacitor. FIG. 1a shows a planar capacitor; and FIG. 1b shows a trench capacitor. As can be seen from FIGs. 1a and 1b, each of the planar capacitor and the trench capacitor is mainly composed of an upper electrode 10, a lower electrode 20, and a dielectric layer 30 located between the upper electrode 10 and the lower electrode 20. FIG. 1c is a schematic diagram of a specific structure of a trench capacitor. As shown in FIG. 1c, the upper electrode 10 of the trench capacitor includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode 20; the lower electrode 20 includes a TiN film layer, a W film layer, and a TiN film layer that are sequentially stacked in a direction approaching the upper electrode 10; and the dielectric layer 30 is an Al_2O_3 film layer.

The trench capacitor shown in FIG. 1c is prepared by a method including: CVD TiN $\rightarrow$ CVD W $\rightarrow$ CVD TiN $\rightarrow$ ALD Al_2O_3 $\rightarrow$ CVD TiN $\rightarrow$ CVD W. CVD TiN and CVD W refer to the preparation of the TiN film layer and the W film layer by a chemical vapor deposition (CVD) process, which needs to be performed in a CVD chamber; and ALD Al_2O_3 refers to the preparation of the Al_2O_3 film layer by an atomic layer deposition (ALD) process, which needs to be performed in an ALD

chamber.

Currently, devices for CVD W, CVD TiN and ALD Al_2O_3 in the market are independent devices and cannot be integrated into the same transport platform, which may cause the following problems.

First, multiple independent devices for CVD and ALD are used for preparing the capacitor, leading to high costs.

Second, after the process in each independent device is completed, the substrate needs to be transported to another independent device corresponding to the next process. Since the transport of the substrate between two independent devices makes the substrate exposed to air, the substrate will be exposed to air five times during the entire fabrication process of the trench capacitor, which will inevitably cause contamination on a surface of the deposited film.

Third, the electrode deposited by the CVD process has a high resistivity, thereby affecting performance of the capacitor.

SUMMARY

To solve at least one of the problems in the related art, the present disclosure provides semiconductor equipment that can protect the substrate from being exposed to air during the transport process, improve performance of the prepared capacitor and reduce the device costs.

To solve one of the above problems, the present disclosure provides semiconductor equipment, including: a physical vapor deposition chamber, an atomic layer deposition chamber and a transport platform; wherein

the physical vapor deposition chamber is configured to prepare an upper electrode and a lower electrode of a capacitor;

the atomic layer deposition chamber is configured to prepare a dielectric layer of the capacitor; and

the transport platform is respectively connected to the physical vapor deposition chamber and the atomic layer deposition chamber and configured to transport a substrate.

Optionally, the equipment further includes a degas chamber configured to degas and anneal the substrate; and the degas chamber is connected to the transport platform.

Optionally, the equipment further includes a preclean chamber configured to remove impurities on a surface of the substrate; and the preclean chamber is connected to the transport platform.

Optionally, the equipment includes a plurality of physical vapor deposition chambers, and the plurality of physical vapor deposition chambers are respectively configured to deposit films of different materials.

Optionally, both the upper electrode and the lower electrode of the capacitor include at least one W film layer and at least one TiN film layer; a number of the plurality of physical vapor deposition chambers is two; and the two physical vapor deposition chambers are respectively configured to deposit the W film layer and the TiN film layer.

Optionally, the upper electrode of the capacitor includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode; and

the lower electrode includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the upper electrode.

Optionally, the upper electrode of the capacitor includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode;

the lower electrode includes a TiN film layer, a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the upper electrode; and

the dielectric layer is an Al_2O_3 film.

Optionally, the dielectric layer includes an Al_2O_3 film layer; and the atomic layer deposition chamber is configured to deposit the Al_2O_3 film.

Optionally, the capacitor is a planar capacitor.

Optionally, the capacitor is a trench capacitor.

The present disclosure has the following beneficial effects:

the semiconductor equipment of the present disclosure uses a physical vapor deposition chamber to prepare an upper electrode and a lower electrode of a capacitor, which, compared with the case of using chemical vapor deposition, forms a film with better compactness and lower resistivity, so that the metal electrode performance of the upper electrode and the lower electrode can be improved and thus the performance of the capacitor is improved; meanwhile, the semiconductor equipment of the present disclosure integrates the physical vapor deposition chamber and the atomic layer deposition chamber with the same transport platform to form a single cluster device system, which reduces the device costs, protects the substrate from being exposed to the air during the transport process, and thus prevents the film surface from being contaminated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a is a schematic structural diagram of a planar capacitor;

FIG. 1b is a schematic structural diagram of a trench capacitor;

FIG. 1c is a schematic structural diagram of a specific trench capacitor;

FIG. 2 is a schematic structural diagram of semiconductor equipment according to an embodiment of the present disclosure;

FIG. 3a is a schematic structural diagram of a planar capacitor according to an embodiment of the present disclosure;

FIG. 3b is a schematic structural diagram of a trench capacitor according to an embodiment of the present disclosure;

FIG. 4 is a schematic structural diagram of a typical magnetron sputtering chamber;

FIG. 5 is a schematic structural diagram of a degas chamber; and

FIG. 6 is a schematic structural diagram of a preclean chamber.

DETAILED DESCRIPTION

To enable those skilled in the art to better understand the technical solution of the present disclosure, the semiconductor equipment of the present disclosure will be

described in detail below in conjunction with the accompanying drawings.

First embodiment

The semiconductor equipment in the embodiment of the disclosure may be used for preparing a capacitor. FIG. 2 is a schematic structural diagram of semiconductor equipment according to an embodiment of the present disclosure. Referring to FIG. 2, the semiconductor equipment includes: a physical vapor deposition (PVD) chamber 40, an atomic layer deposition (ALD) chamber 50, and a transport platform 60. The PVD chamber 40 is configured to prepare an upper electrode and a lower electrode of a capacitor; the ALD chamber 50 is configured to prepare a dielectric layer of the capacitor; and the transport platform 60 is respectively connected to the PVD chamber 40 and the ALD chamber 50 and configured to transport a substrate. Specifically, the transport platform 60 mainly includes a transport chamber and a loading/unloading station, the transport chamber is a vacuum chamber and a manipulator is disposed in the transport chamber. The PVD chamber 40 and the ALD chamber 50 surround and communicate with the transport chamber to form a cluster device system.

After being loaded to the loading station of the transport platform 60, a substrate is taken out of the loading station by the manipulator and transported to the PVD chamber 40 and the ALD chamber 50 in a process order, and after preparation of the capacitor is completed, the processed substrate is transported to the unloading station.

The semiconductor equipment in the embodiment of the present disclosure uses a PVD chamber to prepare an upper electrode and a lower electrode of a capacitor, which, compared with the case of using chemical vapor deposition, forms a film with better compactness and lower resistivity, so that the metal electrode performance of the upper electrode and the lower electrode can be improved, and thus the performance of the capacitor is improved; meanwhile, the semiconductor equipment of the present disclosure integrates the PVD chamber and the ALD chamber with the same transport platform to form a single cluster device system, which reduces the device costs, protects the substrate from being exposed to the air during the transport process, and thus prevents the film surface from being contaminated.

Optionally, the equipment includes a plurality of PVD chambers, and the

plurality of PVD chambers are respectively configured to deposit films of different materials. Thus, a single cluster device system can accomplish deposition of films of different materials without using multiple independent devices, thereby reducing the device costs while protecting the substrate from being exposed to the air during the transport process.

For example, the capacitor may be a planar capacitor or a trench capacitor. Both the upper electrode and the lower electrode of the capacitor may include at least one W film layer and at least one TiN film layer. In this case, the equipment may include two PVD chambers; and the two PVD chambers are respectively configured to deposit the W film layer and the TiN film layer. Optionally, the dielectric layer includes an Al₂O₃ film layer; and the ALD chamber is configured to deposit a Al₂O₃ film.

In the embodiment, FIG. 3a shows a planar capacitor, and FIG. 3b shows a trench capacitor, each of which include an upper electrode 10, a lower electrode 20 and a dielectric layer 30 therebetween. The upper electrode 10 includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode 20; the lower electrode 20 includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the upper electrode 10; and the dielectric layer 30 is an Al₂O₃ film layer.

The planar capacitor and the trench capacitor are prepared by a method including: PVD W→PVD TiN→ALD Al₂O₃→PVD TiN→PVD W. PVD TiN and PVD W refer to the preparation of the TiN film layer and the W film layer by a physical vapor deposition process, and are performed in two PVD chambers, respectively. ALD Al₂O₃ refers to the preparation of the Al₂O₃ film layer by an atomic layer deposition process, and needs to be performed in an ALD chamber.

It should be noted that, in practical applications, the upper electrode and the lower electrode of the capacitor may also adopt other structures. For example, as shown in FIG. 1c, the upper electrode 10 of the capacitor includes a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode 20; and the lower electrode 20 includes a TiN film layer, a W film layer, and

a TiN film layer that are sequentially stacked in a direction approaching the upper electrode 10. Obviously, the number of film layers and the types of materials used in the upper electrode and the lower electrode of the capacitor may be specifically set as required. Further, the number of the PVD chambers and the number of the ALD chambers should correspond to the total number of material types of the film layers used in the upper electrode and the lower electrode.

Optionally, the PVD chamber is a magnetron sputtering chamber. FIG. 4 is a schematic structural diagram of a typical magnetron sputtering chamber. As shown in FIG. 4, the magnetron sputtering chamber includes a cavity 8, a process kit, etc. A base 9 is provided in the cavity 8 and configured to carry a substrate; and a target 3 is provided at the top of the cavity 8. The process kit includes a shield 2, a shelter ring 11 and a deposition ring 14. The shield 2 is circumferentially provided on an inner side of a sidewall of the cavity 8 and configured to protect the sidewall of the cavity 8. The deposition ring 14 is circumferentially disposed around an edge region of the base 9, and the shelter ring 11 is disposed on the shield 2 and the deposition ring 14 and configured to shelter a gap between the shield 2 and the deposition ring 14 to prevent plasma from entering a space below the base 9. Further, a magnetron 6 is provided above the target 3 and driven by a motor 5 to rotate around a central axis. A cooling cavity 7 for containing deionized water is further provided above the target 3 and configured to cool the target; and the magnetron 6 is located in the cooling cavity 7. In addition, a vacuum system 13 is provided at the bottom of the cavity 8 and configured to vacuumize the chamber.

As shown in FIG. 2, the semiconductor equipment in the embodiment of the present disclosure further includes a degas chamber 70 for degassing and annealing the substrate. Further, the degas chamber 70 is connected to the transport platform 60, and forms a cluster device system with other chambers.

Specifically, FIG. 5 is a schematic structural diagram of a degas chamber. Referring to FIG. 5, the degas chamber 70 includes a cavity in which a quartz window 71 dividing the cavity into a vacuum cavity 72 and an atmospheric cavity 73 is provided, the vacuum cavity 72 is provided therein with a base 74 for carrying a

substrate 76; and a heater wire assembly 75 is provided in the base 74 and configured to uniformly heat the substrate 76. A heating bulb 77 is provided in the atmospheric cavity 73 and irradiates heat to the substrate 76 through the quartz window 71. The heating bulb 77 is mounted on a mounting plate 79 through a bulb base 78, and a reflective plate 792 is superposed on a surface of the mounting plate 79 facing the heating bulb 77. A lower surface of the reflective plate 792 is smoothed to better reflect heat from the heating bulb 77 toward the quartz window 71, thereby improving the heating efficiency. Further, a cooling water pipe 791 is provided on the mounting plate 79 and configured to cool the reflective plate 792. A shield 793 is circumferentially provided on an inner side of a sidewall of the cavity, and a cooling water pipe 794 is provided in the shield 793 and configured to cool the sidewall of the cavity, so as to prevent the sidewall of the cavity from being overheated.

By heating the substrate 76 using both the heating bulb 77 and the heater wire assembly 75, not only the heating efficiency is improved, but also rapid and uniform heating of the substrate 76 can be achieved because the heater wire assembly 75 can uniformly heat the substrate 76.

As shown in FIG. 2, the semiconductor equipment in the embodiment of the present disclosure further includes a preclean chamber 80 for removing impurities on the surface of the substrate. Further, the preclean chamber 80 is connected to the transport platform 60, and forms a cluster device system with other chambers.

Specifically, FIG. 6 is a schematic structural diagram of a preclean chamber. Referring to FIG. 6, the preclean chamber 80 includes a chamber lid 801, an insulating chamber wall 802, an annular metal component 803, etc., and a base 804 for carrying a substrate is provided in the preclean chamber 80. Further, a solenoid coil 805 is wound around an outer side of the insulating chamber wall 802, and a shield case 806 is provided around the solenoid coil 805 and configured to prevent magnetic induction lines generated by the solenoid coil 805 from radiating to the outside. In addition, the solenoid coil 805 is connected to a first radio frequency (RF) power source 807 through an adapter, and the first RF power source 807 is configured to apply RF power onto the solenoid coil 805 to ionize gas in the chamber to generate plasma; and

a second RF power source 808 is connected to a base 804 through an adapter, and is configured to generate and apply a negative bias voltage onto the substrate and attract the plasma to bombard the substrate so as to remove impurities on the surface of the substrate , and thus the surface of the substrate can be pre-processed.

It should be noted that FIGs. 4 to 6 show the typical PVD chamber, degas chamber 70 and preclean chamber 80, respectively, but the disclosure is not limited thereto, and in practical applications, PVD chambers, degas chambers 70 and preclean chambers 80 of other structures may also be used. In addition, the ALD chamber employs a chamber structure commonly used in the related art, which will not be described in detail herein.

It will be appreciated that the above implementations are merely exemplary implementations for the purpose of illustrating the principle of the disclosure, and the disclosure is not limited thereto. Various modifications and improvements can be made by a person having ordinary skill in the art without departing from the spirit and essence of the disclosure. Accordingly, all of the modifications and improvements also fall into the protection scope of the disclosure.

What is claimed is:

1. Semiconductor equipment, characterized by comprising: a physical vapor deposition chamber, an atomic layer deposition chamber and a transport platform; wherein

the physical vapor deposition chamber is configured to prepare an upper electrode and a lower electrode of a capacitor;

the atomic layer deposition chamber is configured to prepare a dielectric layer of the capacitor; and

the transport platform is respectively connected to the physical vapor deposition chamber and the atomic layer deposition chamber and configured to transport a substrate.

2. The semiconductor equipment according to claim 1, characterized by further comprising a degas chamber configured to degas and anneal the substrate; wherein the degas chamber is connected to the transport platform.

3. The semiconductor equipment according to claim 1, characterized by further comprising a preclean chamber configured to remove an impurity on a surface of the substrate; wherein the preclean chamber is connected to the transport platform.

4. The semiconductor equipment according to claim 1, characterized in that, the semiconductor equipment comprises a plurality of physical vapor deposition chambers, and the plurality of physical vapor deposition chambers are respectively configured to deposit films of different materials.

5. The semiconductor equipment according to claim 4, characterized in that, both the upper electrode and the lower electrode of the capacitor comprise at least one W film layer and at least one TiN film layer; a number of the plurality of physical vapor deposition chambers is two; and the two physical vapor deposition chambers are

respectively configured to deposit the W film layer and the TiN film layer.

6. The semiconductor equipment according to claim 5, characterized in that, the upper electrode of the capacitor comprises a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode; and

the lower electrode comprises a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the upper electrode.

7. The semiconductor equipment according to claim 5, characterized in that, the upper electrode of the capacitor comprises a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the lower electrode;

the lower electrode comprises a TiN film layer, a W film layer and a TiN film layer that are sequentially stacked in a direction approaching the upper electrode; and the dielectric layer is an Al_2O_3 film.

8. The semiconductor equipment according to any one of claims 1 to 7, characterized in that, the dielectric layer comprises an Al_2O_3 film layer; and the atomic layer deposition chamber is configured to deposit the Al_2O_3 film.

9. The semiconductor equipment according to claim 1, characterized in that, the capacitor is a planar capacitor.

10. The semiconductor equipment according to claim 1, characterized in that, the capacitor is a trench capacitor.