

SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

[0001] The present invention relates to a semiconductor device and a control method of the same.

2. Description of Related Art

10 [0002] A reverse conducting insulated gate bipolar transistor (RC-IGBT) module is known in a power electronics technology that controls drive of a motor mounted on a hybrid vehicle (HV) or an electric vehicle (EV). The RC-IGBT may be regarded as a diode-built-in IGBT.

[0003] For example, Japanese Patent Application Publication No. 2010-4728 (JP
15 2010-4728 A) discloses a power converter in which a diode sense element disposed to a freewheeling diode (FWD) unit and an IGBT sense element disposed to an IGBT unit are connected to one end of a sense resistor, and a control circuit detects an abnormality by determining a polarity of a current that flows to the resistor.

[0004] ~~According to the technology of JP 2010-4728 A, a large potential~~
20 difference generated between a collector and an emitter is directly measured. Therefore, a device having a high withstand voltage is necessary.

SUMMARY OF THE INVENTION

[0005] The present invention provides a semiconductor device and a control
25 method of the same.

[0006] A semiconductor device according to a first aspect of the present invention includes a transistor, a diode, a first detection circuit, a second detection circuit, a calculation circuit and a determination circuit. The diode is connected in reverse parallel with the transistor. The first detection circuit is configured to detect a change

rate of a gate voltage of the transistor with respect to time. The second detection circuit is configured to detect a gate current of the transistor. The calculation circuit is configured to calculate a gate capacitance based on the change rate of the gate voltage with respect to time, and the gate current. The determination circuit is configured to
5 determine, based on a determination result of the gate capacitance at a time when a charge is injected to a gate of the transistor, whether a current flows to the diode or to the transistor.

[0007] A control method of a semiconductor device according to a second embodiment of the present invention is a control method of a semiconductor device that
10 includes a transistor and a diode connected in inverse parallel with the transistor. The control method includes: detecting a change rate of a gate voltage of the transistor with respect to time; detecting a gate current of the transistor; calculating a gate capacitance based on the change rate of the gate voltage with respect to time, and the gate current; and determining, based on a determination result of the gate capacitance when a charge is
15 injected to a gate of the transistor, whether a current flows to the diode or to the transistor.

[0008] According to the aspects described above, a polarity of the current can be determined without using a device having a high withstand voltage.

~~BRIEF DESCRIPTION OF THE DRAWINGS~~

20 [0009] Features, advantages, and technical and industrial significance of exemplary embodiments of the invention will be described below with reference to the accompanying drawings, in which like numerals denote like elements, and wherein:

FIG. 1 is a diagram that illustrates a constitution of a semiconductor device according to a first embodiment of the present invention;

25 FIG. 2 is a graph that illustrates a relationship between an input capacitance and a feedback capacitance versus a collector voltage;

FIG. 3 is a graph that illustrates a relationship between a gate capacitance and a collector voltage;

FIG. 4 is a diagram that illustrates a constitution of an IGBT according to the first embodiment;

FIG. 5 is a diagram that illustrates the constitution of the IGBT according to the first embodiment;

5 FIG. 6 is a diagram that illustrates an operation of the semiconductor device according to the first embodiment when the IGBT is energized;

FIG. 7 is a diagram that illustrates the operation of the semiconductor device according to the first embodiment when a diode is energized;

10 FIG. 8 is a diagram that illustrates a constitution of a semiconductor device according to a second embodiment of the present invention;

FIG. 9 is a diagram that illustrates the operation of the semiconductor device according to the second embodiment when the IGBT is energized; and

FIG. 10 is a diagram that illustrates the operation of the semiconductor device according to the second embodiment when the diode is energized.

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DETAILED DESCRIPTION OF EMBODIMENTS

[0010] Hereinafter, an embodiment for carrying out the invention will be described with reference to the drawings. In the respective drawings, the same constituents will be identified by the same reference numerals and duplicated descriptions thereof will be omitted in some cases.

20 [0011] FIG. 1 is a diagram that illustrates an example of a constitution of a semiconductor device according to the first embodiment of the present invention. A semiconductor device 100 includes an RC-IGBT 110, an RC-IGBT 120, a load 130, a microcomputer 140, a control circuit 150, a control circuit 160 and a power potential unit 170. The RC-IGBT 110 includes an IGBT 111 and a diode 112. The RC-IGBT 120 includes an IGBT 121 and a diode 122.

25 [0012] The control circuit 150 includes a voltage detection circuit 151, a gate voltage gradient calculation circuit 152, a current detection circuit 153, a capacitance calculation circuit 154, a capacitance determination circuit 155, an on-off determination

circuit 156, a drive circuit 157, and a resistor 158.

[0013] The IGBT 111 and the IGBT 121 are connected in series. The diode 112 is disposed corresponding to the IGBT 111. The diode 122 is disposed corresponding to the IGBT 121. The IGBT 111 and the diode 112 are connected in reverse parallel, and the IGBT 121 and the diode 122 are connected in reverse parallel. The diode 122 and the IGBTs 111 and 121 are preferably disposed on the same substrate.

[0014] The IGBT 111 and the IGBT 121 are switching elements that perform an on-off operation. Therefore, without particularly restricting to the IGBT, also a power transistor element such as a MOSFET can be used. In the present embodiment, a case where, as an example of the switching element, the IGBT is used will be described. However, when, for example, the MOSFET is used, it is possible to read by replacing a "collector" into a "drain" and an "emitter" into a "source".

[0015] The control circuit 160 is disposed between the microcomputer 140 and the RC-IGBT 110. The control circuit 150 is disposed between the microcomputer 140 and the RC-IGBT 120. The load 130 is disposed between the RC-IGBT 110 and the RC-IGBT 120.

[0016] In the RC-IGBT 110, an anode of the diode 112 and an emitter of the IGBT 111 are connected, and a cathode of the diode 112 and a collector of the IGBT 111 are connected. ~~The collector is connected with the power potential unit 170, and, for~~ example, a potential V_H (high potential) is supplied thereto. A gate of the IGBT 111 is controlled by a drive signal ($SinH$) 141a output from the microcomputer 140 via the control circuit 160 connected to the gate.

[0017] In the RC-IGBT 120, an anode of the diode 122 and an emitter of the IGBT 121 are connected, and a cathode of the diode 122 and a collector of the IGBT 121 are connected. The emitter is set to, for example, GND (low potential). A gate of the IGBT 121 is controlled by a drive signal ($SinL$) 141b output from the microcomputer 140 via the control circuit 150 connected to the gate.

[0018] The microcomputer 140 outputs a drive signal to a control circuit. For example, the microcomputer 140 inputs the drive signal 141b to the control circuit 150.

and inputs the drive signal 141a to the control circuit 160. Since the drive signal 141a and the drive signal 141b are phase-reversed signals, the control circuit 150 and the control circuit 160 drive in corresponding ways. As the drive signal, for example, signals that turn on (off) the IGBTs 111 and 121, and signals that turn on (off) the diodes 112 and 122 can be used. As the microcomputer 140, for example, a Micro Controller Unit (MCU), a Micro Processing Unit (MPU), an Electronic Control Unit (ECU), and a Central Processing Unit (CPU) can be used.

[0019] The control circuit 150 inputs an appropriate signal to the gate of the IGBT 121 based on the drive signal 141b from the microcomputer 140. Thus, an amount of charges injected to the gate of the IGBT is controlled. As will hereinafter be described in detail, the control circuit 150 monitors a gate capacitance of the IGBT 121 at the time of turn-on and estimates, from the gate capacitance, a potential difference (hereinafter, referred to as a collector voltage) generated between the collector and the emitter of the IGBT 121. When the gate capacitance is smaller than a threshold, the collector voltage is determined to be high, and the control circuit 150 turns on the IGBT 121. When the gate capacitance is larger than the threshold, the collector voltage is determined to be low, and the control circuit 150 turns off the IGBT 121.

[0020] Hereinafter, the respective constituents contained in the control circuit 150 will be described more specifically.

[0021] The voltage detection circuit 151 detects a potential difference (hereinafter referred to as a gate voltage V_{ge}) generated between the gate and the emitter of the IGBT 121 and outputs a detection result to the gate voltage gradient calculation circuit 152. The gate voltage changes based on, for example, an on signal or an off signal output from the microcomputer 140. For example, when the off signal is output from the microcomputer 140, the gate voltage becomes a low level.

[0022] The gate voltage gradient calculation circuit (first detection circuit) 152 includes, for example, a change rate calculation unit and calculates a change rate of the gate voltage with respect to time at the change rate calculation unit based on a signal input from the voltage detection circuit 151. Thereafter, a calculation result is output to

the capacitance calculation circuit 154. As the change rate calculation unit, for example, a differentiation circuit that differentiates the gate voltage V_{ge} with respect to a time t and outputs a value obtained by differentiating with respect to the time (a derivative dV_{ge}/dt) as an output signal can be used. Here, the dV_{ge} denotes a change of the gate voltage, and the dt denotes a change of the time.

[0023] The current detection circuit (second detection circuit) 153 makes use of the resistor 158, detects a gate current I_g of the IGBT 121, and outputs a detection result to the capacitance calculation circuit 154. Also the gate current changes, in the same manner as the gate voltage, based on, for example, the drive signal output from the microcomputer 140 (it changes also based on the current injected from a current injection circuit in a constitution of Embodiment 2).

[0024] The capacitance calculation circuit 154 calculates a gate capacitance C_g based on the signal output from the gate voltage gradient calculation circuit 152 (calculation result of the change rate of the gate voltage with respect to time) and a signal output from the current detection circuit 153 (detection result of the gate current). Thereafter, the calculation result is output to the capacitance determination circuit 155. The gate capacitance is represented by the following formula.

Gate capacitance

$$\begin{aligned}
 &= \text{input capacitance} + \text{feedback capacitance} \\
 &= \text{gate current/change rate of gate voltage with respect to time} \\
 &= C_{ies} + C_{res} = I_g / \{dV_{ge}/dt\} \\
 &= C_g
 \end{aligned}$$

[0025] FIG. 2 shows a relationship between the input capacitance and the feedback capacitance versus the collector voltage. FIG. 3 shows a relationship between the gate capacitance and the collector voltage. As shown in FIG. 2, while a feedback capacitance C_{res} 601 decreases as the collector voltage becomes higher, an input capacitance C_{ies} 602 does not nearly depend on the collector voltage. Therefore, as shown in FIG. 3, a gate capacitance C_g 603 that is a sum of the input capacitance C_{ies} 602 and the feedback capacitance C_{res} 601 depends on the collector voltage. Further, as

shown in FIG. 3, a rate of decrease when the gate capacitance is a threshold Cth 604 or more is larger than the rate of decrease when the gate capacitance is the threshold Cth 604 or less. That is, the rate of decrease of the gate capacitance accompanying an increase of the collector voltage changes based on the threshold Cth 604.

5 [0026] The feedback capacitance Cres when the collector voltage is high is represented by the following formula.

Feedback capacitance

$$\begin{aligned}
 &= \{(\text{capacitance of insulating film between substrate and gate}) \times (\text{junction capacitance between substrate and gate})\} / \{(\text{capacitance of insulating film between} \\
 10 &\text{ substrate and gate}) + (\text{junction capacitance between substrate and gate})\} \\
 &= (C_{gd} \times C_{pn}) / (C_{gd} + C_{pn}) \\
 &= C_{res}
 \end{aligned}$$

[0027] When the collector voltage is high as shown in FIG. 4, a potential on a collector side becomes high in an N layer of a center of the substrate because a part
 15 between a P layer on the collector side and the N layer of the center of the substrate is a forward direction of a PN junction. On the other hand, a reverse bias is applied to a PN junction between a P layer on an emitter side and the N layer of the center of the substrate because the P layer on the emitter side is low in the potential. Therefore, a depleted layer is formed and a junction capacitance Cpn is formed thereby (see X part).

20 [0028] On the other hand, the feedback capacitance Cres when the collector voltage is low is represented by the following formula.

Feedback capacitance

$$\begin{aligned}
 &= (\text{capacitance of insulating film between substrate and gate}) \\
 &= C_{gd} \\
 25 &= C_{res}
 \end{aligned}$$

[0029] When the collector voltage is low as shown in FIG. 5, the potential on the collector side becomes low in the N layer of the center of the substrate because the part between the P layer on the collector side and the N layer of the center of the substrate is the forward direction of the PN junction. The reverse bias is not applied to the PN

junction between the P layer on the emitter side and the N layer of the center of the substrate because also the P layer on the emitter side is low in the potential. Therefore, the junction capacitance C_{pn} is not formed because the depleted layer is not formed.

[0030] That is, whether the junction capacitance C_{pn} is formed or not depends on whether the collector voltage is high or low. It can be estimated that the feedback capacitance C_{res} is small and the collector voltage is high when the junction capacitance C_{pn} is formed. Further, it can be estimated that the feedback capacitance C_{res} is large and the collector voltage is low when the junction capacitance C_{pn} is not formed.

[0031] Furthermore, there is the following relationship between the feedback capacitance C_{res} (V_{ce} : large) when the collector voltage is high and the feedback capacitance C_{res} (V_{ce} : small) when the collector voltage is low.

$$\begin{aligned} \text{Feedback capacitance } C_{res} (V_{ce}: \text{small}) &> \text{Feedback capacitance } C_{res} (V_{ce}: \text{large}) \\ &= C_{gd} > \{(C_{gd} \times C_{pn}) / (C_{gd} + C_{pn})\} \end{aligned}$$

That is, as the collector voltage becomes higher, the feedback capacitance (C_{res}) approaches $\{(C_{gd} \times C_{pn}) / (C_{gd} + C_{pn})\}$ from C_{gd} and becomes smaller.

[0032] The capacitance determination circuit 155 determines whether the gate capacitance C_g is larger than the threshold C_{th} or smaller than the threshold C_{th} based on a signal output from the capacitance calculation circuit 154 and outputs a determination result to the on-off determination circuit 156.

[0033] The on-off determination circuit 156 determines whether to turn on the IGBT 121 based on the signal output from the capacitance determination circuit 155 and the drive signal 141b output from the microcomputer 140 and outputs a determination result to the drive circuit 157.

[0034] For example, when the gate capacitance C_g is smaller than the threshold C_{th} , the feedback capacitance C_{res} can be estimated to be large and the collector voltage V_{ce} can be estimated to be high.

[0035] In this case, since the IGBT 121 is necessary to be energized, the on-off determination circuit 156 determines to turn on the IGBT 121 (gate on determination).

Further, the on-off determination circuit 156 outputs a signal for turning on the IGBT 121 (raising the gate voltage) to the drive circuit 157.

[0036] For example, when the gate capacitance C_g is larger than the threshold C_{th} , the feedback capacitance C_{res} can be estimated to be small and the collector voltage V_{ce} can be estimated to be low.

[0037] In this case, the on-off determination circuit 156 determines to turn off the IGBT 121 (gate-off determination) because the IGBT 121 is not necessary to be energized (the diode 122 is being energized). Further, the on-off determination circuit 156 outputs a signal for turning off the IGBT 121 (decreasing the gate voltage) to the drive circuit 157.

[0038] This is estimated based on the gate capacitance after a start of charge injection. Further, the on-off control of the IGBT 121 is performed based on the determination result of the on-off determination circuit 156 obtained by comparing the gate capacitance and the threshold. A time after the start of charge injection includes a monitoring period of the gate capacitance C_g . The monitoring period of the gate capacitance denotes a small period from a time when an on-signal (here, the on-signal is a drive start instruction signal from the microcomputer) is input to the gate of the IGBT 121 to a time when the IGBT 121 is turned on. That is, charges in such an amount that ~~can turn on the IGBT 121 are injected to the gate of the IGBT 121. The on-off~~ determination circuit 156 can determine whether the energization to the IGBT 121 is necessary during a small period when the IGBT 121 is switched from off to on. At an end of the monitoring period of the gate capacitance, the gate voltage does not change. For example, the gate voltage reaches a limiting value.

[0039] The drive circuit 157 outputs a control signal to the gate of the IGBT 121 based on the signal output from the on-off determination circuit 156. The IGBT 121 is turned on (or off) based on the control signal.

[0040] The control circuit 160 is driven responding to the control circuit 150. Since a constitution of the control circuit 160 is the same as that of the control circuit 150, a detailed description thereof will be omitted. The control circuit 160 outputs a control

signal to the gate of the IGBT 111 based on the drive signal 141a from the microcomputer 140 in the same manner as in the control circuit 150.

[0041] The power potential unit 170 supplies an appropriate potential, for example, V_H to the collector of the IGBT 111 and the cathode of the diode 112.

5 [0042] According to the semiconductor device 100 of the present embodiment, the control circuit 150 can determine a polarity of the current based on the gate capacitance after the start of charge injection of the IGBT 121. The polarity of the current can be determined by a method that makes use of the result of the monitoring of the gate capacitance without using a device having a high withstand voltage.

10 [0043] Next, an example of operations at the time of turn-on of the semiconductor device 100 will be described.

[0044] Firstly, an operation when the IGBT 121 is energized will be described in detail with reference to FIG. 6. An operation when the on-off determination circuit 156 monitors the gate capacitance at the time of turn-on of the IGBT 121 will be described.

15 A case where a switching waveform in each of the signals becomes "High" is abbreviated as "H", and a case where the switching waveform becomes "Low" is abbreviated as "L".

[0045] Until a time $t1\alpha$ is reached, the $SinL$ (drive signal) is "L" because the IGBT 121 is off. The feedback capacitance C_{res} is small because a V_{ceL} (collector voltage) is "H". A V_{geL} (gate voltage) and a dV_{geL}/dt (change rate of the gate voltage with respect to time) are "L" because the gate current does not flow. Therefore, also a CML (a monitored value of the gate capacitance C_g) is "L". An I_{cL} (collector current) and an I_{diL} (diode current) are also "L". Here, the diode 112 in the RC-IGBT 110 is energized and a current flows in the diode 112.

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[0046] At the time $t1\alpha$, the $SinL$ changes from "L" to "H". Thus, an on-signal is input to the gate of the IGBT121 (start to monitor the gate capacitance C_g). The V_{ceL} is "H". The gate current flows accompanying the turn-on of the IGBT121. Therefore, the V_{geL} starts an increase and also the dV_{geL}/dt starts an increase. Also the CML starts an increase because the monitoring of the gate capacitance C_g is started. The I_{cL} and the I_{diL} are "L".

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[0047] The SinL and the VceL maintain "H" from the time $t1\alpha$ to the time $t2\alpha$ (monitoring period of the gate capacitance C_g). The VgeL increases in proportion to the time. The dV_{geL}/dt increases rapidly in the proximity of the time $t1\alpha$, passes a maximum value, and decreases rapidly in the proximity of the time $t2\alpha$. The dV_{geL}/dt changes such that it has the maximum value at a time in the center between the time $t1\alpha$ and the time $t2\alpha$ (a shape of a waveform becomes a shape like a bisymmetrical parabola). The on-off determination circuit 156 performs the gate on determination of the IGBT121 because the CML does not exceed the threshold C_{th} . Although the IcL maintains a state of "L" for a while, as the gate capacitance C_g increases, it increases in proportion to the time. The IdL maintains "L".

[0048] At the time $t2\alpha$, the SinL is "H". The VceL starts a decrease based on the determination result of the on-off determination circuit 156 that the CML is smaller than the threshold C_{th} (start of a mirror period). The VgeL is a value that increased during from the time $t1\alpha$ to the time $t2\alpha$. The dV_{geL}/dt is "L". The CML increases rapidly and becomes larger than the threshold C_{th} (end of monitoring of the gate capacitance C_g). The IcL is a value that increased during from the time $t1\alpha$ to the time $t2\alpha$. The IdL is "L".

[0049] During from the time $t2\alpha$ to a time $t3\alpha$, the SinL maintains "H". The VceL decreases rapidly in proportion to the time and maintains "L". The VgeL becomes flat and maintains a value at the time $t2\alpha$. The dV_{geL}/dt maintains "L". The CML maintains a value that increased at the time $t2\alpha$. The IcL decreases rapidly and, after that, increases gradually in proportion to the time. The IdL maintains "L".

[0050] At the time $t3\alpha$, the SinL is "H". The VceL is a value that decreased during from the time $t2\alpha$ to the time $t3\alpha$. The VgeL starts an increase (end of the mirror period) and also the dV_{geL}/dt starts an increase. The CML starts a decrease. The IcL and the IdL do not change. Since the VceL is "L" after the end of the mirror period, the feedback capacitance C_{res} becomes larger, and the on-off determination circuit 156 becomes incapable of determining an energization direction.

[0051] Here, the mirror period indicates a period during which due to the change of the collector voltage V_{ce} at the time of turn-on (or at the time of turn-off), the capacitance between the gate and the collector changes and the gate voltage becomes flat. A length of the mirror period depends on, for example, a product of a capacitance
 5 between the gate and the collector and a resistance of a resistor 158. Therefore, it is preferable that a loss increase be prevented from increasing by appropriately adjusting the length of the mirror period.

[0052] During from the time $t3\alpha$ to a time $t4\alpha$, the $SinL$ maintains "H". The V_{ceL} maintains a value at the time $t3\alpha$. The V_{geL} increases in proportion to the time.
 10 The dV_{geL}/dt increases rapidly in the proximity of the time $t3\alpha$, passes a maximum value, and decreases rapidly in the proximity of the time $t4\alpha$. The dV_{geL}/dt changes such that it has the maximum value at a time in the center of the time $t3\alpha$ and the time $t4\alpha$. Further, the maximum value of the dV_{geL}/dt during from the time $t3\alpha$ to the time $t4\alpha$ becomes smaller than the maximum value of the dV_{geL}/dt during from the time
 15 $t1\alpha$ to the time $t2\alpha$. The CML nearly maintains a value that decreased at the time $t3\alpha$. The I_{cL} continues a gradual increase in proportion to the time. The I_{diL} maintains "L".

[0053] At the time $t4\alpha$, the $SinL$ is "H", the V_{ceL} is a value at the time $t3\alpha$, and the V_{geL} is a value that increased during from the time $t3\alpha$ to the time $t4\alpha$. When the V_{geL} of the IGBT 121 has completed an increase (has reached a limit value), it maintains
 20 a constant value. The gate capacitance C_g cannot be monitored because the gate current does not flow. The dV_{geL}/dt is "L". The CML decreases rapidly and becomes smaller than the threshold C_{th} . The I_{cL} and the I_{diL} do not change.

[0054] After the time $t4\alpha$ is exceeded, the $SinL$ maintains "H". The V_{ceL} , the V_{geL} and the dV_{geL}/dt maintain values at the time $t4\alpha$. The CML maintains a value
 25 that is larger than a value until the time $t1\alpha$ is reached and smaller than a value during from the time $t1\alpha$ to the time $t2\alpha$. The I_{cL} continues a gradual increase in proportion to the time. The I_{diL} maintains "L".

[0055] Next, an operation when the diode 122 is energized will be described in detail with reference to FIG. 7. An operation in the case where the on-off determination

circuit 156 monitors the gate capacitance at the time of turn-on of the IGBT 121 will be described.

[0056] Until a time $t1\beta$ is reached, the SinL is "L" because the IGBT 121 is off. The feedback capacitance Cres is small because the VceL is "H". The VgeL and the
5 dVgeL/dt are "L" because the gate current does not flow. The CML is "L". The IdIL increases in proportion to the time because the diode 122 is energized. The IcL is "L".

[0057] At the time $t1\beta$, the SinL changes from "L" to "H". Thus, a signal is input to the gate of the IGBT121 (start of monitoring of the gate capacitance Cg). The VceL is "L". As the IGBT121 is turned on, the gate current flows. Therefore, the
10 VgeL starts an increase and also the dVgeL/dt starts an increase. Also the CML starts an increase because the monitoring of the gate capacitance Cg is started. The behaviors of the IcL and the IdIL do not change.

[0058] During from the time $t1\beta$ to a time $t2\beta$ (monitoring period of the gate capacitance Cg), the SinL maintains "H" and the VceL maintains "L". The VgeL
15 increases in proportion to the time accompanying turn on of the IGBT 121. The dVgeL/dt increases rapidly in the proximity of the time $t1\alpha$, passes a maximum value, and decreases rapidly in the proximity of the time $t2\alpha$. The dVgeL/dt changes such that it has the maximum value at a time in the center of the time $t1\alpha$ and the time $t2\alpha$. The
~~on-off determination circuit 156 performs the gate off determination of the IGBT121~~
20 based on the monitoring result because the CML exceeds the threshold Cth. The IdIL increases in proportion to the time. The IcL is "L".

[0059] At the time $t2\beta$, the SinL is "H". The VceL is "L". The VgeL starts a decrease based on the determination result of the on-off determination circuit 156 that the CML is larger than the threshold Cth. The dVgeL/dt is "L". The CML decreases
25 rapidly and becomes smaller than the threshold Cth (end of monitoring of the gate capacitance Cg). The behaviors of the IcL and the IdIL do not change.

[0060] After the time $t2\beta$ is exceeded, the SinL maintains "H" and the VceL maintains "L". The IGBT 121 is turned off because the VgeL decreases rapidly. The gate capacitance Cg cannot be monitored because the gate current does not flow. That is,

the on-off determination circuit 156 cannot determine the energization direction. The dV_{geL}/dt maintains "L". The CML maintains a value at the time $t2\beta$. The I_{diL} increases in proportion to the time. The I_{cL} is "L".

[0061] Therefore, according to the semiconductor device 100 of the present embodiment, the gate capacitance C_g is monitored at the time of turn-on of the IGBT 121 and whether it is larger or smaller than the threshold is determined. The control circuit 150 performs an appropriate control by determining whether to turn on the IGBT 121 without any change or to turn off the IGBT 121 by stopping the turn-on of the IGBT 121 based on the determination result of the gate capacitance C_g . Thus, a loss deterioration due to a V_F increase of the diode can be suppressed because the diode and the IGBT can be driven by avoiding an interference of the gate.

[0062] In the second embodiment, a semiconductor device 200 that is different from the first embodiment will be described. The semiconductor device 200 includes a current injection circuit and an off holding circuit in the control circuit, differing from the semiconductor device 100.

[0063] FIG. 8 is a diagram that illustrates an example of a constitution of a semiconductor device according to the present embodiment. The semiconductor device 200 includes the RC-IGBT 110, the RC-IGBT 120, the load 130, the microcomputer 140, ~~a control circuit 250, a control circuit 260, and the power potential unit 170.~~ The RC-IGBT 110 includes the IGBT 111 and the diode 112. The RC-IGBT 120 includes the IGBT 121 and the diode 122.

[0064] The semiconductor device 200 includes a current injection circuit 180 and an off holding circuit 190 in the control circuit 250 in addition to the constitution of the semiconductor device 100. Further, although also the control circuit 260 includes the current injection circuit and the off holding circuit, since the constitution of the control circuit 260 corresponds to the constitution of the control circuit 250, a detailed description thereof will be omitted.

[0065] As shown in FIG. 8, the control circuit 250 includes the voltage detection circuit 151, the gate voltage gradient calculation circuit 152, the current detection circuit

153, the capacitance calculation circuit 154, the capacitance determination circuit 155, the on-off determination circuit 156, the drive circuit 157, the resistor 158, the current injection circuit 180, and the off-holding circuit 190.

[0066] The current injection circuit 180 injects a current I_{g2} to the gate at the
5 time of turn-off of the IGBT 121. That is, the voltage detection circuit 151 detects a change of the gate voltage that changes based on the current I_{g2} that is injected from the current injection circuit 180. Further, in the same manner, the current detection circuit 153 detects a change of the gate current that changes based on the current I_{g2} that is injected from the current injection circuit 180. The control circuit 250 controls on-off of
10 the IGBT 121 based on the determination result of the gate capacitance (whether the gate capacitance is larger or smaller than the threshold) at the time of turn-off of the IGBT 121.

[0067] The off holding circuit 190 holds the gate voltage of the IGBT 121 such that it may not increase to a predetermined value or more (holds the gate voltage at a
15 predetermined value or less). The gate capacitance can be monitored even at the time of turn-off of the IGBT 121 by holding the gate voltage at the predetermined value or less by the off holding circuit 190.

[0068] That is, in the semiconductor device 100 according to the embodiment 1,
~~the control circuit 150 detects the change of the gate capacitance that changes based on~~
20 an on-signal output from the microcomputer 140. That is, the monitoring period of the gate capacitance is at the time of turn-on of the IGBT 121. On the other hand, in the semiconductor device 200 according to the embodiment 2, the control circuit 250 detects the change of the gate capacitance that changes based on the current I_{g2} that is injected from the current injection circuit 180. That is, the monitoring period of the gate
25 capacitance is at the time of turn-off of the IGBT 121.

[0069] According to the semiconductor device 200 of the present embodiment, the gate capacitance at the time of turn-off of the IGBT 121 can be monitored by making use of the current injection circuit 180 and the off holding circuit 190. That is, when the diode 122 is energized, it is possible that the IGBT 121 is not utterly turned on.

Therefore, superfluous loss can be omitted and the loss deterioration of the diode can be suppressed. Further, the direction of the current (energization direction) can be determined on a real-time basis at the time of turn-off of the IGBT 121.

[0070] Next, an example of an operation at the time of turn-off of the semiconductor device 200 will be described.

[0071] Firstly, an operation at the time of energization of the IGBT will be described in detail. An operation when the on-off determination circuit 156 monitors the gate capacitance at the time of turn-off of the IGBT will be described.

[0072] In FIG 9, a switching waveform at the time of turn-on is shown. As shown in FIG. 9, the drive signal is denoted with SinL , the collector voltage is denoted with VceL , the injection current is denoted with Ig2 , the gate voltage is denoted with VgeL , the change rate of the gate voltage with respect to time is denoted with $d\text{VgeL}/dt$, the monitoring value of the gate capacitance Cg is denoted with CML , the collector current is denoted with IcL , and the diode current is denoted with IdiL . Further, the case where a switching waveform in each of the signals becomes "High" is abbreviated as "H" and the case where the switching waveform becomes "Low" is abbreviated as "L".

[0073] Until the time $t1\alpha$ is reached (monitoring period of the gate capacitance Cg), the SinL is "L" because the IGBT 121 is off. The feedback capacitance Cres is small because the VceL is "H". ~~The Ig2 is a sine curve because the current is injected~~ from the current injection circuit 180 to the gate of the IGBT 121 (start of monitoring of the gate capacitance Cg). The waveform of the current Ig2 is not limited to the sine curve. Also the VgeL and the $d\text{VgeL}/dt$ are sine curves because these respond to the Ig2 . The CML is smaller than the threshold Cth . Therefore, the on-off determination circuit 156 performs a gate-on determination of the IGBT 121. The IcL and the IdiL are "L".

[0074] The SinL changes from "L" to "H" at the time $t1\alpha$. The VceL is "H". The microcomputer 140 inputs an on-signal to the gate of the IGBT 121 and the IGBT 121 is turned on thereby (end of monitoring of the gate capacitance Cg). The injection of the current to the gate is terminated accompanying the turn-on of the IGBT121 because the current injection circuit 180 injects the current to the gate at only the time of

turn-off of the IGBT121. Therefore, the I_{g2} changes from the sine curve to "L". The V_{geL} starts an increase and also the dV_{geL}/dt starts an increase. The CML and the I_{cL} do not change. The I_{diL} is "L" because the on-off determination circuit 156 performs the gate-on determination of the IGBT 121 (the diode 122 is off).

5 [0075] During from the time $t1\alpha$ to the time $t2\alpha$, the $SinL$ and the V_{ceL} maintain "H". The I_{g2} maintains "L". The V_{geL} increases in proportion to the time accompanying the turn-on of the IGBT 121. The dV_{geL}/dt increases rapidly in the proximity of the time $t1\alpha$, passes a maximum value, and decreases rapidly in the proximity of the time $t2\alpha$. The dV_{geL}/dt changes such that it has the maximum value
10 at a time in the center of the time $t1\alpha$ and the time $t2\alpha$. The CML, the I_{cL} and the I_{diL} do not change.

 [0076] At the time $t2\alpha$, the $SinL$ is "H". The V_{ceL} starts a decrease based on the determination result of the on-off determination circuit 156 that the CML is smaller than the threshold C_{th} (start of a mirror period). The I_{g2} does not change. The V_{geL}
15 is a value that increased during from the time $t1\alpha$ to the time $t2\alpha$. The dV_{geL}/dt decreases rapidly and is "L". The CML increases rapidly and becomes larger than the threshold C_{th} . The I_{cL} starts an increase. The I_{diL} is "L".

 [0077] During from the time $t2\alpha$ to the time $t3\alpha$, the $SinL$ maintains "H". The ~~V_{ceL} decreases rapidly in proportion to the time and maintains "L".~~ The ~~I_{g2} maintains~~
20 "L". The V_{geL} becomes flat and maintains a value at the time $t2\alpha$. The dV_{geL}/dt maintains "L". The CML maintains a value that increased at the time $t2\alpha$. The I_{cL} increases in proportion to the time and, after that, decreases in proportion to the time. The I_{diL} maintains "L".

 [0078] At the time $t3\alpha$, the $SinL$ is "H". The V_{ceL} is a value that decreased
25 during from the time $t2\alpha$ to the time $t3\alpha$. The I_{g2} does not change. The V_{geL} starts an increase (end of the mirror period) and also the dV_{geL}/dt starts an increase. The CML decreases rapidly but is larger than the threshold C_{th} . The I_{cL} is in the middle of the decrease and I_{diL} does not change. The gate capacitance C_g cannot be monitored after the end of the mirror period.

[0079] During from the time $t3\alpha$ to the time $t4\alpha$, the $SinL$ maintains "H". The $VceL$ maintains a value at the time $t3\alpha$. The $Ig2$ maintains "L". The $VgeL$ increases in proportion to the time. The $dVgeL/dt$ increases rapidly in the proximity of the time $t3\alpha$, passes a maximum value, and decreases rapidly in the proximity of the time $t4\alpha$.
 5 The $dVgeL/dt$ changes such that it has the maximum value at a time in the center of the time $t3\alpha$ and the time $t4\alpha$. Further, the maximum value of the $dVgeL/dt$ during from the time $t3\alpha$ to the time $t4\alpha$ becomes smaller compared with the maximum value of the $dVgeL/dt$ during from the time $t1\alpha$ to the time $t2\alpha$. The CML maintains nearly a value that decreased at the time $t3\alpha$. The IcL decreases in proportion to the time and, after
 10 that, increases in proportion to the time. The $IdiL$ maintains "L".

[0080] At the time $t4\alpha$, the $SinL$ is "H" and the $VceL$ is the value at the time $t3\alpha$. The $Ig2$ does not change. The $VgeL$ is a value that increased during from the time $t3\alpha$ to the time $t4\alpha$. When the $VgeL$ of the IGBT 121 completes an increase (upon reaching a limit value), it maintains a constant value. The gate capacitance Cg cannot
 15 be monitored because the gate current does not flow. The $dVgeL/dt$ is "L". The CML decreases rapidly and becomes smaller than the threshold Cth . The behaviors of the IcL and the $IdiL$ do not change.

[0081] After the time $t4\alpha$ is exceeded, the $SinL$ maintains "H". The $VceL$, the $Ig2$, the $VgeL$, and the $dVgeL/dt$ maintain values at the time $t4\alpha$. The CML maintains a
 20 value that is smaller than a value until the time $t1\alpha$ is reached. The IcL continues a gradual increase in proportion to the time. The $IdiL$ maintains "L".

[0082] Next, an operation at the time of energization of the diode 122 will be described in detail. An operation in the case where the on-off determination circuit 156 monitors the gate capacitance at the time of turn-off of the IGBT will be described.

25 [0083] In FIG. 10, a switching waveform at the time of turn-on is shown. As shown in FIG. 10, the drive signal is denoted with $SinL$, the collector voltage is denoted with $VceL$, the injection current is denoted with $Ig2$, the gate voltage is denoted with $VgeL$, the change rate of the gate voltage with respect to time is denoted with $dVgeL/dt$,

the monitoring value of the gate capacitance C_g is denoted with CML, the collector current is denoted with I_{cL} , and the diode current is denoted with I_{diL} .

[0084] Until the time $t1\beta$ is reached, the IGBT 121 is off. The $SinL$ changes from "L" to "H" on the way. The feedback capacitance C_{res} is small because the V_{ceL} is "H". The I_{g2} is a sine curve because the current is injected from the current injection circuit 180 to the gate of the IGBT 121 (start of monitoring of the gate capacitance C_g). Also the V_{geL} and the dV_{geL}/dt are sine curves because these respond to the I_{g2} . The CML is larger than the threshold C_{th} . Therefore, the on-off determination circuit 156 performs a gate-off determination of the IGBT 121. Although the diode 122 is energized, the I_{diL} decreases gradually in proportion to the time. The I_{cL} is "L".

[0085] The $SinL$ is "H" at the time $t1\beta$. The V_{ceL} is "L". The I_{g2} is the sine curve. The V_{geL} starts an increase because charges based on the on-signal from the microcomputer 140 are injected to the gate of the IGBT 121. Also the dV_{geL}/dt starts an increase. The CML decreases rapidly. The I_{diL} and the I_{cL} do not change.

[0086] During from the time $t1\beta$ to the time $t2\beta$, the $SinL$ maintains "H". The V_{ceL} maintains "L" for a while and, after that, increases. The I_{g2} is the sine curve. The V_{geL} increases in proportion to the time accompanying the turn-on of the IGBT 121. Also the dV_{geL}/dt increases accompanying the increase of the V_{geL} . The CML ~~maintains a value that decreased at the time $t1\beta$. The CML is smaller than the threshold~~ C_{th} . The I_{diL} is "L" (the diode 122 is off) because the on-off determination circuit 156 performs the gate-on determination of the IGBT 121. Here, a current direction is reversed. As the current direction is reversed, the I_{cL} increases gradually from "L" in proportion to the time.

[0087] At the time $t2\beta$, the $SinL$ is "H". The V_{ceL} passes a peak of an increase and starts a decrease. The current injection circuit 180 injects the current to the gate only the time of turn-off of the IGBT121. Therefore, the injection of the current to the gate is terminated accompanying the turn-on of the IGBT 121. Thus, the I_{g2} changes to "L" from the sine curve (end of monitoring of the gate capacitance C_g). The

VgeL starts an increase and also the dV_{geL}/dt starts an increase. The CML is smaller than the threshold Cth. The IcL and the IdiL do not change.

[0088] During from the time $t2\beta$ to the time $t3\beta$, the SinL maintains "H". The VceL decreases rapidly in proportion to the time and maintains "L". After the end of the mirror period, the feedback capacitance Cres becomes larger because the VceL is "L", and the on-off determination circuit 156 cannot monitor the gate capacitance Cg. The Ig2 maintains "L". The VgeL increases in proportion to the time, becomes flat at a certain value, and increases again in proportion to the time. The dV_{geL}/dt increases rapidly in the proximity of the time $t2\beta$, passes a maximum value, decreases rapidly ("L"), after that, increases again, passes a maximum value, and decreases ("L"). Here, the maximum value of the dV_{geL}/dt in the second increase becomes smaller compared with the maximum value of the dV_{geL}/dt in the first increase. The CML increases rapidly, becomes larger than the threshold Cth, after that, decreases rapidly and maintains a value larger than the threshold Cth. The IcL increases gradually in proportion to the time. The IdiL maintains "L".

[0089] At the time $t3\beta$, the SinL is "H". The VceL and the Ig2 are "L". The VgeL is a value at the time $t3\beta$. The dV_{geL}/dt is "L". The CML decreases rapidly (smaller than the threshold Cth). The behaviors of the IcL and the IdiL do not change.

~~[0090] After the time $t3\beta$ is exceeded, the SinL maintains "H" and the VceL and the Ig2 maintain "L".~~ The VgeL maintains a value at the time $t3\beta$. When the VgeL of the IGBT 121 completes an increase (reaches a limiting value), it maintains a constant value. The gate capacitance Cg cannot be monitored because the gate current does not flow. The dV_{geL}/dt maintains "L". The CML maintains a value at the time $t3\beta$. The IcL increases gradually in proportion to the time. The IdiL does not change.

[0091] Therefore, according to the semiconductor device 200 of the present embodiment, a technology that can determine a polarity of the current without using a device having a high withstand voltage can be provided.

[0092] In the above, although embodiments for carrying out the present invention have been described in detail, the present invention is not limited to such

specific embodiments. The present invention can be variously modified and altered within a range of a gist of the present invention.

CLAIMS

1. A semiconductor device characterized by comprising:
 - a transistor (121);
 - a diode (122) connected in reverse parallel with the transistor;
 - a first detection circuit (152) configured to detect a change rate of a gate voltage of the transistor with respect to time;
 - a second detection circuit (153) configured to detect a gate current of the transistor;
 - a calculation circuit (154) configured to calculate a gate capacitance based on the change rate of the gate voltage with respect to time, and the gate current; and
 - a determination circuit (155) configured to determine, based on a determination result of the gate capacitance at a time when a charge is injected to a gate of the transistor, whether a current flows to the diode or to the transistor.
2. The semiconductor device according to claim 1, wherein
 - on-off of the transistor is controlled based on the determination result of the gate capacitance at a time when the transistor is off.
- ~~3. The semiconductor device according to claim 1, further comprising~~
 - an on-off determination circuit (156) configured to determine whether to turn on the transistor based on the determination result of the gate capacitance at a time when the transistor is off.
4. The semiconductor device according to claim 3, wherein
 - the first detection circuit, the second detection circuit, the calculation circuit, the determination circuit, and the on-off determination circuit constitute a part of a control circuit; and
 - the control circuit is configured to control on-off of the transistor.

5. The semiconductor device according to claim 4, wherein
the control circuit includes a drive circuit (157); and
the drive circuit is configured to control the on-off of the transistor based on a signal output from the on-off determination circuit.

6. The semiconductor device according to any one of claims 1 to 5, further comprising:

a current injection circuit (180) configured to inject a charge to the gate at a time when the transistor is off; and

an off holding circuit (190) configured to hold the gate voltage at a predetermined value or less at the time when the transistor is off.

7. A control method of a semiconductor device that includes a transistor (121) and a diode (122) that is connected in reverse parallel with the transistor, the control method characterized by comprising:

detecting a change rate of a gate voltage of the transistor with respect to time;

detecting a gate current of the transistor;

calculating a gate capacitance based on the change rate of the gate voltage with respect to time, and the gate current; and

determining, based on a determination result of the gate capacitance when a charge is injected to a gate of the transistor, whether a current flows to the diode or to the transistor.