NICAM AUDIO SIGNAL RESAMPLER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims priority to U.S. Provisional Patent Application serial number 60/756,515, entitled "NICAM Decoder With Output Resampler," filed January 5, 2006, attorney docket number 056233-0287. The entire content of this provisional application is incorporated herein by reference.

BACKGROUND

[0002] *Technical Field*

[0003] This application relates to the extraction of digitally-sampled audio, such as NICAM (Near-Instantaneous Companded Audio Multiplex), from a broadcast carrier.

[0004] *Description of Related Art*

[0005] NICAM audio is typically sampled with a 32 kHz clock at the point of transmission. A local 32 kHz sample clock is typically generated to drive a digital-to-analog converter at the receiver as part of the demodulation process. This local sample clock, however, is usually not synchronous with the remote sample clock. Some decoders, moreover, use local sample clocks at a different frequency, such as at 48 kHz or 44.1 kHz.

[0006] This lack of synchronization between the remote sample clock and the local sample clock can create errors in processing, resulting in distortion in the audio. Eliminating this distortion can require a large number of computations to be quickly performed, increasing the cost and complexity of the decoder.

SUMMARY

[0007] A digital sample rate converter may include a digital up sampler configured to receive a first stream of digital samples of an analog signal at a first frequency and to generate a second stream of digital samples at a second frequency that is substantially higher than the first frequency and that substantially tracks the first stream of digital samples. The converter may also include a non-linear interpolator configured to interpolate between two sequential digital samples in the second stream of digital samples in a non-linear manner.

[0008] The non-linear interpolator may be configured to interpolate between the two sequential digital samples by determining a non-linear function that substantially fits three sequential digital samples in the second stream that include the two sequential digital samples. The non-linear function may be a parabolic function.

[0009] The digital sample rate converter may include a digital delay line configured to generate at least two versions of the second stream of digital samples, each delayed by a different amount of time with respect to the second stream of digital samples.

[0010] The non-linear interpolator may be configured to interpolate at points in time that are based on a phase difference between the first stream of digital samples and a local sample clock.

[0011] The digital sample rate converter may include a phase differential calculator configured to calculate the phase differential. The phase difference calculator may include a phased-lock loop.

[0012] The digital sample rate converter may include a synchronizer configured to synchronize interpolations made by the non-linear interpolator with the local sample clock. The synchronizer may include a 2-word FIFO.

[0013] The first stream of digital samples may be demodulated NICAM audio samples at a frequency of approximately 32 kHz.

[0014] The local sample clock may have a frequency of approximately 31.25 kHz, 32 kHz, 44.1 kHz, 46.875 kHz, or 48 kHz.

[0015] The second frequency may be between 128Khz to 1.024Mhz. The second frequency may be approximately 384 kHz.

[0016] The digital up sampler may include a sample interpolator configured to divide each digital sample in the first stream into an integer multiple of samples. The sample interpolator may be configured to divide each digital sample in the first stream into between 4 and 32 samples. The sample interpolator may be configured to divide each digital sample in the first stream into 12 samples.

[0017] One of the integer multiple of samples may be based on the digital sample in the first stream and the other integer multiple samples may be substantially zero.

[0018] The digital up sampler may include a digital low pass filter and the digital low pass filter may be configured to filter the integer multiple of samples.

[0019] A phase differential calculator may include a first phase accumulator configured to generate information indicative of the phase of a local sample clock at a first resolution. The phase differential calculator may include a clock generator configured to generate a generated clock and information indicative of the phase of the generated clock at a second resolution that is lower than the first resolution as a function of a phase comparison and in synchronism with a remote sample clock. The phase differential calculator may include a phase comparator configured to generate the phase comparison based on a phase difference between the information indicative of the phase of the local sample clock and the information indicative of the phase of the generated clock.

[0020] The clock generator may include an adder configured to repeatedly add an amount to a sum that is a function of the phase comparison and in synchronism with the remote sample clock. The sum may be configured to reset after a predetermined number of additions.

[0021] The generated clock may be based on the sum generated by the adder.

[0022] The clock generator may be configured to generate the second clock based on a filtering of the phase comparison by a second order phase-locked loop filter.

[0023] The clock generator may be configured to update the information indicative of the phase of the generated clock at a frequency that is an integer multiple of the remote sample clock.

[0024] A NICAM audio signal re-sampler may include a non-linear interpolator configured to interpolate in a non-linear manner between sequential digital samples that are based on a stream of demodulated NICAM audio samples.

[0025] The NICAM audio signal re-sampler may include a local sample clock and a synchronizer configured to synchronize an interpolated stream of demodulated NICAM audio samples with the local sample clock.

[0026] The NICAM audio signal re-sampler may include a phase comparator configured to generate a measurement of phase difference between a signal that is

synchronous with the stream of demodulated NICAM audio samples and a signal that is synchronous with the local sample clock.

[0027] These, as well as other components, steps, features, objects, benefits, and advantages, will now become clear from a review of the following detailed description of illustrative embodiments, the accompanying drawings, and the claims.

BRIEF DESCRIPTION OF DRAWINGS

[0028] The drawings disclose illustrative embodiments. They do not set forth all embodiments. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective illustration. When the same numeral appears in different drawings, it is intended to refer to the same or like components or steps.

[0029] FIG. 1 is a block diagram of a resampler for one audio channel of a NICAM signal.

[0030] FIG. 2 is a block diagram a NICAM processor that includes the NICAM resampler illustrated in FIG. 1.

[0031] FIG. 3 is a block diagram of a prior art FM/DQPSK demodulator that may be used to generate signals used by the NICAM processor illustrated in FIG. 2.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0032] Illustrative embodiments are now discussed. Other embodiments may be used in addition or instead. Details that may be apparent or unnecessary may be omitted to save space or for more effective presentation.

[0033] FIG. 1 is a block diagram of a resampler for one audio channel of a NICAM signal. As shown in FIG. 1, an up-sampler 101 may receive demodulated audio samples and a remote sample clock.

[0034] The demodulated audio samples may be any type of audio samples. For example, they may be one channel of digital audio samples that have been demodulated from a NICAM signal.

[0035] The demodulated audio samples may be at any frequency or resolution. For example, they may be at a frequency of 32 kHz and have a 14 bit resolution.

[0036] The remote sample clock may be a clock that is synchronous with the demodulated audio samples. For example, the remote sample clock may be a 32 kHz NICAM enable signal that has been decoded from a NICAM decoder.

[0037] The up-sampler 101 may include a clock multiplier 103. The clock multiplier 103 may be configured to produce a multiplied remote sample clock that represents the remote sample clock multiplied in frequency by an integer value. The integer may be selected to be high enough so as provide a desired degree of resolution, but not so high as to require a costly system to quickly process a large number of calculations. In one embodiment, the clock multiplier 103 may multiply the remote sample clock frequency by between 4 and 32 times, such as by 12 times.

[0038] When the remote sample clock is a 32 kHz NICAM enable signal, and when the integer multiplier is 12, the clock multiplier 103 may generate a multiplied remote sample clock at a frequency of approximately 384 kHz.

[0039] To accomplish this multiplication, the clock multiplier 103 may be driven with a high frequency local clock having a frequency that is approximately the frequency of the desired multiplied remote sample clock. In the example given, this may be a frequency of approximately 384 kHz. The high frequency local clock may be derived from a high frequency local system clock, such as a local system clock that may operate at approximately 35.804 mHz.

[0040] The clock multiplier 103 may be configured to use a periodic edge in the remote sample clock, such as a periodic rising or falling edge, as the first edge in the multiplied remote sample clock. The clock multiplier 103 may be configured to inject the remaining needed pulses before the next periodic edge of the remote sample clock from the high frequency local clock. If 12 is used as the multiplier for the clock multiplier 103, for example, the clock multiplier 103 may therefore pass the first pulse from the remote sample clock and follow this with 11 pulses from the high frequency local clock, following which this cycle of 1 pulse from the remote sample clock and 11 pulses from the high frequency local clock may repeat.

[0041] The up-sampler 101 may include an interpolator 105. The interpolator105 may be configured to interpolate between samples of the demodulated audio samples. The interpolator 105 may be configured to do so at the frequency of the

multiplied remote sample clock generated by the clock multiplier 103 and in synchronism with it. In this configuration, the interpolator 105 may be configured to output the current value of the demodulated audio sample as a first value. During the next 11 cycles of the multiplied remote sample clock, the interpolator 105 may be configured to output a value representative of zero.

[0042] The up-sampler 101 may include a low pass filter 107. The interpolated samples from the interpolator 105 may pass through the low pass filter 107. The low pass filter may be configured to smoothen the interpolated samples from the interpolator 105. The low pass filter 107 may be a digital low pass filter and may provide filtered values at the frequency of the multiplied remote sample clock. The effect of the low pass filter 107, therefore, may be to create interpolated values at the frequency of the multiplied remote sample clock between each of the varying values of the demodulated audio samples which may be at a far lower frequency.

[0043] The output of the up-sampler 101 may be delivered to a digital delay line 109. The digital delay line 109 may be configured to generate at least three versions of the up-sampled demodulated audio samples, two of which are successively delayed with respect to the up-sampled demodulated audio samples. As reflected in FIG. 1, the multiplied remote sample clock may be used to clock the digital delay line 109. The digital delay line 109 may therefore simultaneously output three sequential samples of the up-sampled demodulated audio samples.

[0044] A parabolic interpolator 111 may be configured to interpolate between any two of these samples at a point that is based on interpolator phase information received from a phase differential calculator 115 (discussed below). The parabolic interpolator 111 may be configured to do so by fitting a parabolic function to a set of three sequential points that contain the two sequential points between which an interpolation is desired. The parabolic interpolator 111 may use this fitted parabolic function to calculate the desired interpolated value.

[0045] As is well known, a parabolic function is a non-linear function. The interpolator 111 may instead be configured to fit a non-linear function to the three points that is not a parabolic function. The interpolator 111 may instead be configured to fit a linear function to the two consecutive points between which an interpolation is desired.

[0046] The output of the parabolic interpolator 111 may be directed into a synchronizer, such as into a 2-word FIFO (first in first out) 113. The 2-word FIFO 113 may be configured to load the interpolated value from the parabolic interpolator 111 into the first word of the FIFO upon command of a generated clock (discussed below). It may be configured to shift that loaded value into the second word of the FIFO upon command of a local sample clock (discussed below). The net effect of this operation of the 2-word FIFO 113 may be to cause the interpolated values provided by the parabolic interpolator 111 to be synchronized to the local sample clock. A different form of synchronizer may be used instead.

[0047] The local sample clock may be a local clock that the NICAM decoder extracts from the high frequency local system clock and which the NICAM decoder uses to drive a local digital-to-analog converter to convert the remote demodulated audio samples from their digital to analog format. However, the remote demodulated audio samples may not be synchronized to the local sample clock. Indeed, the local sample clock may even be at a different frequency. When operating with NICAM signals, for example, the local sample clock may have a frequency of approximately 31.25 kHz, 32 kHz, 44.1 kHz, 46.875 kHz, 48 kHz, or any other amount.

[0048] The function of the phase differential calculator 115 may be to calculate a difference in phase between the local sample clock and a signal that is based upon the remote sample clock, such as the multiplied remote sample clock. Information relating to this phase difference may be used by the parabolic interpolator 111 to direct the parabolic interpolator 111 to the location between two of the points from the digital delay line 109 at which an interpolated value is desired.

[0049] The phase differential calculator 115 may include a phase accumulator 117. The phase accumulator 117 may be configured to generate information indicative of the phase of the local sample clock.

[0050] The phase accumulator 117 may use any approach for accomplishing this. For example, the phase accumulator may use the local sample clock as a gate to a counter that counts local system clock pulses, such as pulses that may be at a frequency of 36.804 mHz. The count might begin on each periodic edge of the local sample clock, such as upon each rising or falling edge, and recycle on the next

periodic edge. The value of this count may therefore be representative of the phase of the local sample clock.

[0051] The phase differential calculator 115 may include a clock generator 119 that may include an adder 120. The clock generator 119 may be configured to add the value of a filtered phase error (discussed below) using the adder 120 during each cycle of the multiplied remote sample clock. The adder 120 may be configured to reset after a predetermined number of the multiplied remote sample clock pulses so as to result in the stream of added values having a cycling frequency, referred to in FIG. 1 as the generated clock, that is substantially the same as the frequency of the local sample clock.

[0052] For example, if the remote sample clock and the local sample clock are both operating at approximately 32 kHz, and if the multiplied remote sample clock has a frequency of approximately 384 kHz, the clock generator 119 may be configured to add the filtered phase error to the count 12 times before recycling the count. The values of the added count may thus be representative of the phase of the generated clock, but adjusted based on the filtered phase error.

[0053] The phase differential calculator may include a phase comparator 121. The phase comparator 121 may be configured to compare the information from the phase accumulator 117 that is indicative of the phase of the local sample clock with the information from the clock generator 119 that is indicative of the phase of the generated clock, i.e., with the value provided by the adder 120. The phase comparator 121 may generate a phase error indicative of the result of this comparison. The phase differential calculator 115 may include a filter 123 that is configured to filter this phase error and to deliver the filtered phase error back to the clock generator 119. The filter 123 may provide any type of filtering function. For example, the filter 123 may be a second order phase-locked loop filter. The filter 123 may be scaled to allow for a fixed amount of jitter before allowing the phase-locked loop phase error to influence the output.

[0054] The output of the filter 123 may serve as the value which is added by the adder 120 during each cycle of the multiplied remote sample clock, until the adder resets. The net effect may be to create a phase-locked loop that generates a generated clock that is substantially locked in phase to the local sample clock by comparing information indicative of the phase of the generated clock with

information indicative of the phase of the local sample clock. The count that is indicative of the phase of the generated clock may be updated at a frequency that is lower than the frequency at which the count that is indicative of the phase of the local sample clock is updated. Thus, the information that is indicative of the phase of the generated clock may be at a lower resolution than the information that is indicative of the phase of the local sample clock.

[0055] The output of the phase comparator 121 may be used by the parabolic interpolator 109 to signify the location between two of the points in the digital delay line 109 at which an interpolation is needed, as discussed above.

[0056] FIG. 2 is a block diagram of a NICAM processor that includes the NICAM resampler illustrated in FIG. 1. FIG. 2 follows a standard signal naming convention in which a prefix indicates the direction and bit width of the named signal: "i" for input; "w" for a wire; and "ow" for an output wire. The type prefix is followed by a numeric indication of the bit width of the signal.

[0057] The NICAM resampler that is illustrated in FIG. 1 may be part of a resampler 201 in FIG. 2 and used to resample one of the two NICAM channels of demodulated audio samples, indicated in FIG. 2 as w14NCAMRight. A duplicate of the resampler that is illustrated in FIG. 1 may be another part of the resampler 201 and used to resample the other NICAM channel of demodulated audio samples, indicated in FIG. 2 as w14NICAMLeft. The signal w1RightLeftEn to the resampler 201 may be the remote sample clock referred to in FIG. 1 and discussed above.

[0058] The remaining portions of the NICAM processor shown in FIG. 2 may be the same as in a standard NICAM 728 processor.

[0059] Prior to modulation in the transmitting system, the NICAM 32 kHz sampled audio data stream may have been compressed, framed, interleaved, scrambled, and assigned parity bits with embedded compounding information to facilitate expansion at the receiving equipment. The other functions depicted in FIG. 2 may take the serial dibits from a DQOSK demodulator (i2QPSKData) and enable (i2QPSKDataEn) signals and reverse all of this pre-modulation processing. First, frame synchronization may be achieved. Next, the data in each frame may be descrambled. After descrambling, the data may be de-interleaved. Finally, parity bits may be checked and the audio samples may be expanded.

[0060] Each NICAM frame may have a length of 1 msec (defined at the point of transmission) and may deliver, after expansion, thirty-two 14 bit samples for each stereo channel (w14NICAMRight, w14NICAMLeft). Each 1 msec interval may be defined as 364 of the recovered i1QPSKDataEn pulses. These pulses may be generated by a symbol timing recovery algorithm in a DQPSK demodulator. The 32 samples may be delivered to the resampler shown in FIG. 1 at a rate of 32 kHz (32 per each 1 msec interval), along with an accompanying enable (w1RightLeftEn) pulse.

[0061] FIG. 3 is a block diagram of a prior art FM/DQPSK demodulator that may be used to generate signals used by the NICAM processor illustrated in FIG. 2. The digital audio input at some intermediate frequency (IF Data) may first be down converted to baseband by a downconverter 301. Next, the undesired mixing product may be removed via a low pass filter in a down-sampler 302, which also may meet the NICAM root raised cosine pulse shaping requirement. After filtering, the data may be sub-sampled by 16 up-samples in the down-sampler 302. At this point, a baseband quadrature signal may be available for a DQPSK demodulator 303. The DQPSK demodulator 303 may recover the symbol clock and make a decision on each symbol point. The decided two-bit data may be output along with a data enable, which may occur at a rate determined by the symbol clock of the transmitting system.

[0062] The various functions that are illustrated in FIGS. 1-3 and that have been described above may be implemented by hardware, software, or by a combination of hardware and software, all in accordance with well-known techniques. For example, Hardware Description Language (HDL) coding may be written from which an integrated hardware implementation may be created, again, all in accordance with well-known techniques. An example of such HDL coding is set forth in United States Provisional Application Serial No. 60/756,515, entitled "NICAM Decoder With Output Resampler," filed January 5, 2006, attorney docket no. 56233-287, the entire content of which is incorporated herein by reference.

[0063] The components, steps, features, objects, benefits and advantages that have been discussed are merely illustrative. None of them, nor the discussions relating to them, are intended to limit the scope of protection in any way. Numerous other embodiments are also contemplated, including embodiments that have fewer,

additional, and/or different components, steps, features, objects, benefits and advantages. The components and steps may also be arranged and ordered differently.

[0064] For example, the resampler illustrated in FIG. 1 and discussed above may be used in connection with audio signals other than NICAM signals, such as MP2, MP3 or MP4 audio. Indeed, the resampler may be to change the sample rate of any type of unsynchronized sample stream.

[0065] Although having been primarily discussed in connection with a local sample clock frequency of 32 kHz, the resamplers that have been discussed may also advantageously be used in connection with local sample clocks of other frequencies, such as approximately 31.25 kHz, 44.1 kHz, 46.875 kHz, and/or 48 kHz.

[0066] The phrase "means for" when used in a claim embraces the corresponding structures and materials that have been described and their equivalents. Similarly, the phrase "step for" when used in a claim embraces the corresponding acts that have been described and their equivalents. The absence of these phrases means that the claim is not limited to any of the corresponding structures, materials, or acts or to their equivalents.

[0067] Nothing that has been stated or illustrated is intended to cause a dedication of any component, step, feature, object, benefit, advantage, or equivalent to the public, regardless of whether it is recited in the claims.

[0068] In short, the scope of protection is limited solely by the claims that now follow. That scope is intended to be as broad as is reasonably consistent with the language that is used in the claims and to encompass all structural and functional equivalents.

CLAIMS:

1. A digital sample rate converter comprising:

a digital up sampler configured to receive a first stream of digital samples of an analog signal at a first frequency and to generate a second stream of digital samples at a second frequency that is substantially higher than the first frequency and that substantially tracks the first stream of digital samples; and

a non-linear interpolator configured to interpolate between two sequential digital samples in the second stream of digital samples in a non-linear manner, wherein the non-linear interpolator is configured to interpolate at points in time that are based on a phase difference between the first stream of digital samples and a local sample clock.

2. The digital sample rate converter of claim 1 wherein the non-linear interpolator is configured to interpolate between the two sequential digital samples by determining a non-linear function that substantially fits three sequential digital samples in the second stream that include the two sequential digital samples.

3. The digital sample rate converter of claim 2 wherein the non-linear function is a parabolic function.

4. The digital sample rate converter of claim 2 further including a digital delay line configured to generate at least two versions of the second stream of digital samples, each delayed by a different amount of time with respect to the second stream of digital samples.

5. The digital sample rate converter of claim 4 further comprising a phase differential calculator configured to calculate the phase differential, said phase difference calculator including a phased-lock loop.

6. The digital sample rate converter of claim 4 further comprising a synchronizer configured to synchronize interpolations made by the non-linear interpolator with the local sample clock.

7. The digital sample rate converter of claim 5 wherein the synchronizer includes a 2-word FIFO.

8. The digital sample rate converter of claim 4 wherein the first stream of digital samples are demodulated NICAM audio samples at a frequency of approximately 32 kHz.

9. The digital sample rate converter of claim 7 wherein the local sample clock has a frequency of approximately 31.25 kHz.

10. The digital sample rate converter of claim 7 wherein the local sample clock has a frequency of approximately 32 kHz.

11. The digital sample rate converter of claim 7 wherein the local sample clock has a frequency of approximately 44.1 kHz.

12. The digital sample rate converter of claim 7 wherein the local sample clock has a frequency of approximately 46.875 kHz.

13. The digital sample rate converter of claim 7 wherein the local sample clock has a frequency of approximately 48 kHz.

14. The digital sample rate converter of claim 7 wherein the second frequency is between 128 Khz to 1.024 Mhz.

15. The digital sample rate converter of claim 13 wherein the second frequency is approximately 384 kHz.

16. The digital sample rate converter of claim 1 wherein the digital up sampler includes a sample interpolator configured to divide each digital sample in the first stream into an integer multiple of samples.

17. The digital sample rate converter of claim 15 wherein the sample interpolator is configured to divide each digital sample in the first stream into between 4 and 32 samples.

18. The digital sample rate converter of claim 16 wherein the sample interpolator is configured to divide each digital sample in the first stream into 12 samples.

19. The digital sample rate converter of claim 15 wherein the sample interpolator is configured such that one of the integer multiple of samples is based on the digital sample in the first stream and the other integer multiple samples are substantially zero.

20. The digital sample rate converter of claim 18 wherein the digital up sampler includes a digital low pass filter and wherein the digital low pass filter is configured to filter the integer multiple of samples.