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(54) SEMICONDUCTOR MEMORY DEVICE

(71) We, TOKYO SHIBAURA ELECTRIC COMPANY LIMITED, a Japanese corporation, of 72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to a semiconductor memory device.

Presently, as a semiconductor memory device a memory device based on the use of static memory cells formed of CMOS FET's may be used. In this type of semiconductor memory device, high density integration, and shortening of the access time, of the semiconductor elements constituting the device are a great problem.

20 Conventionally, in order to accomplish the high density integration of the semiconductor elements, so-called silicon gate field effect transistors are favorably employed. This is because, in a semiconductor memory device using silicon gate field effect transistors, a silicon polycrystalline layer having diffused impurities can be advantageously used for wiring. In a conventional semiconductor memory device, however, since the conventional semiconductor memory device is so constructed that data reading is effected serially through a switching element composed of an IG FET whose source electrode is not connected to the substrate and whose source potential is varied, a back gate bias effect occurs in the IGFET's constituting the switching element when the data reading is carried out, thereby delaying the switching operation of the switching element and greatly prolonging the access time.

An object of the invention is to provide a

semiconductor memory device whose access time is shortened. 45

According to the invention there is provided a semiconductor memory device comprising a pair of complementary data input lines, a plurality of pairs of complementary data lines, a plurality of memory cells disposed in the form of a matrix, the memory cells of each column being connected between the corresponding pair of complementary data lines, a respective switching circuit for each column having a first drive terminal for receiving a column selection signal and two switching elements each connected between the respective one of said pair of complementary data lines in the corresponding column and the corresponding complementary data input line and responsive to said column selection signal to connect each of said pair of complementary data lines in the corresponding column to each of said pair of complementary data input lines, respective, and a respective data detection circuit separately from the respective switching circuit for each column having a second drive terminal for receiving a signal corresponding to said column selection signal and directly connected to at least one of said pair of complementary data lines in the corresponding column and adapted, upon receipt of said signal corresponding to said column selection signal, to provide a signal corresponding to a data signal from said at least one complementary data line. 80

An embodiment of this invention will now be described with reference to the accompanying drawings in which:

Figure 1 is a circuit diagram showing part of a semiconductor memory device according to the invention; 85

Figures 2 and 3 show graphs illustrating the access time for each memory cell of the device partly shown in Figure 1 together

with that for an equivalent conventional device in the cases where aluminum gate type IG FETs and polycrystalline silicon gate type IG FETs are used, respectively; and

Figures 4 to 7 each show a modified form of a data detection circuit used in the device partly shown in the Figure 1.

Figure 1 shows part of a semiconductor memory device having memory cells arranged in the form of a matrix and a respective data detection circuit disposed for each column. Though in Figure 1, for a better understanding of the device, only one memory cell 10 is shown, memory cells similar to the memory cell 10 are actually disposed in matrix form and a respective data detection circuit similar to the data detection circuit 20 is arranged for each column.

The memory cell 10 has a p channel type IG FET 11 and an n channel type IG FET 12 connected in series between a power source terminal V_{DD} and ground, and a p channel type IG FET 13 and an n channel type IG FET 14 similarly connected in series therebetween. The connection point p1 between the IG FETs 11 and 12 is connected to respective gate electrodes of the IG FETs 13 and 14, and the connection point p2 between the IG FETs 13 and 14 is connected to respective gate electrodes of the IG FETs 11 and 12, thereby to constitute a flip-flop. The memory cell 10 further has an n channel type IG FET 15 connected between a data line 41 and the connection point p1 and an n channel type IG FET 16 connected between a data line 42 and the connection point p2. Respective gate electrodes of the IG FETs 15 and 16 are connected to a row selection line 43.

A switching circuit 30 has n channel type IG FETs 31 and 32 for connecting the data lines 41 and 42 to data input lines 44 and 45, respectively, and a drive terminal 33 for receiving a column selection signal S from a column selection circuit (not shown). Respective gate electrodes of the IG FETs 31 and 32 are connected to the drive terminal 33. The data input lines 44 and 45 are adapted to transmit a data signal and an inverted signal of this data signal from a data source (not shown), respectively.

The data detection circuit 20 has p channel type IG FETs 21 and 22 and n channel type IG FETs 23 and 24 connected in series between a power source terminal V_{DD} and ground, p channel type IG FETs 25 and 26 and n channel type IG FETs 27 and 28 connected in series between the power source terminal V_{DD} and ground, and a drive terminal 29 for receiving an inverted signal S of the column selection signal from the column selection circuit. The drive terminal 29 is connected to respective gate

electrodes of the IG FETs 21 and 25, and the respective gate electrodes of the IG FETs 24 and 28 are connected to the drive terminal 33. While respective gate electrodes of the IG FETs 22, 23 and respective gate electrodes of the IG FETs 26, 27 are connected to the data lines 41 and 42, respectively, the connection point between the IG FETs 22 and 23 and the connection point between the IG FETs 26 and 27 are connected to data output lines 46 and 47, respectively.

Hereinafter, the operation of the semiconductor memory device will be explained in accordance with positive logic operation.

In the case of writing information into the memory cell 10, the row selection line 43 is excited by a row selection circuit (not shown) and simultaneously the column selection signal S is supplied from the column selection circuit (not shown) to the drive terminal 33. Upon receipt of this column selection signal, the IG FETs 31 and 32 are rendered conducting, so that data signals on the data input lines 44 and 45 are transmitted onto the data lines 41 and 42, respectively. The IG FETs 15 and 16 of the memory cell 10 are rendered conducting by the excited row selection line 43. Assume now that the data signal on the data line 41 has a "1" level and the data signal on the data line 42 has a "0" level. Then, the "1" level signal on the data line 41 is applied to the respective gate electrodes of the IG FETs 13 and 14 through the conducting IG FET 15, thereby rendering the IG FET 14 conducting and the IG FET 13 nonconducting, while the "0" level signal on the data line 42 is applied to the respective gate electrodes of the IG FETs 11 and 12 through the conducting IG FET 16, thereby rendering the IG FET 11 conducting and the IG FET 12 nonconducting. Thus, the point p1 is kept at a "1" level, while the point p2 is kept at a "0" level.

During the above writing operation, the column selection signal is applied to the respective gate electrodes of the IG FETs 24 and 28 of the data detection circuit 20 through the drive terminal 33 of the switching circuit 30, thereby rendering the IG FETs 24 and 28 conducting, while the inverted signal of the column selection signal is applied to the respective gate electrodes of the IG FETs 21 and 25 through the drive terminal 29 of the detection circuit 20, thereby rendering the IG FETs 21 and 25 conducting. In the case where the data signal on the data line 41 has a "1" level, the IG FET 22 is kept nonconducting and the IG FET 23 is rendered conducting. Simultaneously, upon receipt of the "0" level signal from the data

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line 42, the IG FET 26 is rendered conducting and the IG FET 27 is kept non-conducting. As a result, inverted signals of the data signal on the data input lines 44 and 45 are transmitted onto the data output lines 46 and 47, respectively.

In the case of reading information from the memory cell 10, as in the case of the writing operation, the row selection line 43 is excited, and simultaneously the column selection signal and the inverted signal of the column selection signal are applied to the drive terminals 33 and 29, respectively. As a result, the data signal from the point p1 of the memory cell 10 which has a logical level of, for example, "1" is applied to the gate electrode of the IG FET 23 through the IG FET 15 and the data line 41 to render the IG FET 23 conducting, and simultaneously the data signal from the point p2 which has a logical level of "0" is applied to the gate electrode of the IG FET 26 through the IG FET 16 and the data line 42 to render the IG FET 26 conducting. Thus, a "0" level signal and a "1" level signal are transmitted onto the data output lines 46 and 47, respectively.

Since, each data signal read from the memory cell 10 is transmitted without being passed serially through an IG FET, it is free from a back gate bias effect unlike the conventional case, so that access time is decreased largely.

Figures 2 and 3 show by solid lines, the variations in voltages on a data in reading a "0" level signal from the memory cell 10 in the case of constructing the semiconductor memory device shown in Figure 1 by using IG FETs each having an aluminum gate and each having a polycrystalline silicon gate respectively. The broken lines indicate the variations in the voltages on the data line of a conventional equivalent semiconductor memory device. At the points of time when the information-reading and -writing cycles commence respectively, the data lines 41 and 42 are so excited as to each have a "1" level signal thereon. Therefore, in the case where a data signal having a "0" level is read from the memory cell 10, some length of time is required until data detection circuit 20 reads this data signal as a "0" level data signal, namely until the "1" level signal on the appropriate data line is reduced to a specified level.

In the case of using IG FETs each having an aluminum gate in the device, as shown in Figure 2, at a point of time t0 after completion of the address designating operation, the "0" level data signal from the memory cell 10 is connected to the appropriate data line, and the signal level on this data line gradually decreases and at

a point of time t1 the data detection circuit 20 reads the data signal on this data line as a data signal having a logical level of "0". Conventionally, much time was required from the start of the address designating operation until the content of the memory cell was coupled to the data detection circuit and at a point of time t2 the content of the memory cell was read by the data detection circuit. When comparing a conventional semiconductor memory device having an access time of, for example, 1 microsecond with the equivalent semiconductor memory device according to the invention, the access time of the latter device was shortened by about 300 nanoseconds.

Also, in the case of using IG FETs each having a polycrystalline silicon gate, the access time t1 of the present device is made much shorter than the access time t2 of the conventional one.

Figures 4 to 7 show respectively modified forms of the data detection circuit of the semiconductor memory device shown in Figure 1.

The data detection circuit shown in Figure 4 includes p channel type IG FETs 121 and 122 connected in series between a power source terminal V_{D3} and the data output line 46, and p channel type IG FETs 123 and 124 connected in series between the power source terminal V_{D3} and the data output line 47. Respective gate electrodes of the IG FETs 121 and 123 are connected to a drive terminal 129 for receiving the column selection signal S, while respective gate electrodes of the IG FETs 122 and 124 are connected to the data lines 41 and 42, respectively. The data detection circuit further includes n channel type IG FETs 126 and 125 respectively. The data detection circuit further includes n channel type IG FETs 126 and 125 respectively connected between the data output lines 46, 47 and ground so as to maintain the data output lines 46 and 47 usually at a logical level of "0. Respective gate electrodes of the IG FETs 125 and 126 are supplied with an inverted signal $\bar{C}$ of a chip selection signal C through a drive terminal 130 and, during a period in which a chip selecting operation is not performed, the IG FETs 125 and 126 are rendered conducting thereby to set the potential of the data output lines 46, 47 at a logical level of "0". Connected in parallel to the IG FETs 125 and 126 are n channel type IG FETs 127 and 128 having a small mutual conductance, respectively. The IG FETs 127 and 128 are supplied with a voltage through a power source terminal V_{D4} at their respective gate electrodes and rendered always conducting to compensate that portion of the charge in the data output

lines 46 and 47 which has leaked during the dip selecting operation.

When the inverted signal F of the column selection signal S is applied to the drive terminal 129, the IG FETs 121 and 123 are rendered conducting. Where, under this condition, for example "1" and "0" level data signals appear on the data lines 41 and 42, respectively, the IG FET 122 is not rendered conducting and accordingly the signal level on the data output line 46 remains at a "0" level. On the other hand, the IG FET 124 is rendered conducting upon receipt of the "0" level data signal from the data line 42, so that the signal level on the data output line 47 is altered to a "1" level by the power source terminal V_{DS} . Thus, the "1" and "0" level data signals on the data lines 41 and 42 are read onto the output lines 46 and 47 as "0" and "1" level data signals, respectively.

The data detection circuit shown in Figure 4 is constituted by elements fewer in number than those constituting the data detection circuit of Figure 1. Namely, in the data detection circuit of Figure 1, $n \times 8$ elements are required for the memory cells arranged in the form of a matrix having n columns, whereas in the data detection circuit of Figure 4 only $(n \times 4 + 4)$ elements are required for the memory cells arranged in the form of a n -column matrix.

The data detection circuit shown in Figure 5 which is constructed by making interchanges between the IG FETs 121 and 122 and between the IG FETs 123 and 124, of the data detection circuit shown in Figure 4, performs the same functions as in the case of the data detection circuit of Figure 4.

Note that in the data detection circuits of Figures 4 and 5 the data output lines are usually kept at a "0" level, whereas the data detection circuit of Figure 6 is so constructed that the data output lines are so excited as to normally have a potential corresponding to "1" level. In Figure 6, n channel type IG FETs 221 and 222 and n channel type IG FETs 223 and 224 are connected in series between the data output lines 46, 47 and ground, respectively. Respective gate electrodes of the IG FETs 221 and 223 are connected to the data lines 41 and 42, respectively, and respective gate electrodes of the IG FETs 222 and 224 are connected to a drive terminal 229 for receiving the column selection signal. The data detection circuit shown in Figure 6 further includes p channel type IG FETs 225 and 226 respectively connected between a power source terminal V_{DS} and the data output lines 46, 47. Respective gate electrodes of the IG FETs 225 and 226 are supplied with the chip selection signal C through a drive

terminal 230, and during a period in which a chip selecting operation is not carried out the IG FETs 225 and 226 are rendered conducting, so that the data output lines 46 and 47 are so excited through the power source terminal V_{DS} as to have a potential corresponding to a "1" level. Connected in parallel with the IG FETs 225 and 226 are p channel type IG FETs 227 and 228 having a small mutual conductance, respectively. The IG FETs 227 and 228 have their respective gate electrodes kept at ground potential and are rendered always conducting to compensate that portion of the charge in the data output lines 46 and 47 which has leaked during the chip selecting operation.

The data detection circuit shown in Figure 6 operates in accordance with a similar principle, and has a similar function and effect, as in the case of the data detection circuit shown in Figure 4. When an inverted signal S is applied to the drive terminal 229, the IG FETs 222 and 224 are rendered conductive. Where, under this condition, for example, "1" and "0" level data signals appear on the data lines 41 and 42, respectively, the IGFET 223 is not rendered conductive, and accordingly the signal on the data output line 47 remains at "1" level. On the other hand, the IGFET 221 is rendered conductive, and the signal level on the data output line 46 is changed to "0" level or ground level. Further, the data detection circuit shown in Figure 7 which is constructed by making interchanges between the IGFETs 221 and 222 and between the IGFETs 223 and 224, of the data detection circuit of Figure 6, functions in the same manner as in the case of the data detection circuit of Figure 6.

This invention has above been explained by describing five embodiments, but is not limited thereto. For instance, with regard to the data detection circuit shown in Figure 1, it is possible to omit the IGFETs connected to one of the data lines 41 or 42, for example the IGFETs 25, 26, 27 and 28, and to omit the corresponding data output line, for example the data output line 47. Further, with regard to the data detection circuits shown in Figures 4 to 7, the IGFETs 127 and 128, 227 and 228 having a small mutual conductance may be omitted. Further, the drive terminal 229 shown in Figure 6 and 7 may be connected to the drive terminal 33 of the switching circuit 30 shown in Figure 1. Further, in Figure 1, it is possible to perform respective interchanges between the IGFETs 21, 24, 25 and 28 and the IGFETs 22, 23, 26 and 27.

WHAT WE CLAIM IS:—

1. A semiconductor memory device comprising a pair of complementary data

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lines 46 and 47 which has leaked during the dip selecting operation.

When the inverted signal F of the column selection signal S is applied to the drive terminal 129, the IG FETs 121 and 123 are rendered conducting. Where, under this condition, for example "1" and "0" level data signals appear on the data lines 41 and 42, respectively, the IG FET 122 is not rendered conducting and accordingly the signal level on the data output line 46 remains at a "0" level. On the other hand, the IG FET 124 is rendered conducting upon receipt of the "0" level data signal from the data line 42, so that the signal level on the data output line 47 is altered to a "1" level by the power source terminal V_{DS} . Thus, the "1" and "0" level data signals on the data lines 41 and 42 are read onto the output lines 46 and 47 as "0" and "1" level data signals, respectively.

The data detection circuit shown in Figure 4 is constituted by elements fewer in number than those constituting the data detection circuit of Figure 1. Namely, in the data detection circuit of Figure 1, $n \times 8$ elements are required for the memory cells arranged in the form of a matrix having n columns, whereas in the data detection circuit of Figure 4 only $(n \times 4 + 4)$ elements are required for the memory cells arranged in the form of n -column matrix.

The data detection circuit shown in Figure 5 which is constructed by making interchanges between the IG FETs 121 and 122 and between the IG FETs 123 and 124, of the data detection circuit shown in Figure 4, performs the same functions as in the case of the data detection circuit of Figure 4.

Note that in the data detection circuits of Figures 4 and 5 the data output lines are usually kept at a "0" level, whereas the data detection circuit of Figure 6 is so constructed that the data output lines are so excited as to normally have a potential corresponding to "1" level. In Figure 6, n channel type IG FETs 221 and 222 and n channel type IG FETs 223 and 224 are connected in series between the data output lines 46, 47 and ground, respectively. Respective gate electrodes of the IG FETs 221 and 223 are connected to the data lines 41 and 42, respectively, and respective gate electrodes of the IG FETs 222 and 224 are connected to a drive terminal 229 for receiving the column selection signal. The data detection circuit shown in Figure 6 further includes p channel type IG FETs 225 and 226 respectively connected between a power source terminal V_{DS} and the data output lines 46, 47. Respective gate electrodes of the IG FETs 225 and 226 are supplied with the chip selection signal C through a drive

terminal 230, and during a period in which a chip selecting operation is not carried out the IG FETs 225 and 226 are rendered conducting, so that the data output lines 46 and 47 are so excited through the power source terminal V_{DS} as to have a potential corresponding to a "1" level. Connected in parallel with the IG FETs 225 and 226 are p channel type IG FETs 227 and 228 having a small mutual conductance, respectively. The IG FETs 227 and 228 have their respective gate electrodes kept at ground potential and are rendered always conducting to compensate that portion of the charge in the data output lines 46 and 47 which has leaked during the chip selecting operation.

The data detection circuit shown in Figure 6 operates in accordance with a similar principle, and has a similar function and effect, as in the case of the data detection circuit shown in Figure 4. When an inverted signal S is applied to the drive terminal 229, the IG FETs 222 and 224 are rendered conductive. Where, under this condition, for example, "1" and "0" level data signals appear on the data lines 41 and 42, respectively, the IGFET 223 is not rendered conductive, and accordingly the signal on the data output line 47 remains at "1" level. On the other hand, the IGFET 221 is rendered conductive, and the signal level on the data output line 46 is changed to "0" level or ground level. Further, the data detection circuit shown in Figure 7 which is constructed by making interchanges between the IGFETs 221 and 222 and between the IGFETs 223 and 224, of the data detection circuit of Figure 6, functions in the same manner as in the case of the data detection circuit of Figure 6.

This invention has above been explained by describing five embodiments, but is not limited thereto. For instance, with regard to the data detection circuit shown in Figure 1, it is possible to omit the IGFETs connected to one of the data lines 41 or 42, for example the IGFETs 25, 26, 27 and 28, and to omit the corresponding data output line, for example the data output line 47. Further, with regard to the data detection circuits shown in Figures 4 to 7, the IGFETs 127 and 128, 227 and 228 having a small mutual conductance may be omitted. Further, the drive terminal 229 shown in Figure 6 and 7 may be connected to the drive terminal 33 of the switching circuit 30 shown in Figure 1. Further, in Figure 1, it is possible to perform respective interchanges between the IGFETs 21, 24, 25 and 28 and the IGFETs 22, 23, 26 and 27.

WHAT WE CLAIM IS:—

1. A semiconductor memory device comprising a pair of complementary data



(12)

input lines, a plurality of pairs of complementary data lines, a plurality of memory cells disposed in the form of a matrix, the memory cells of each column being connected between the corresponding pair of complementary data lines, a respective switching circuit for each column having a first drive terminal for receiving a column selection signal and two switching elements each connected between the respective one of said pair of complementary data lines in the corresponding column and the corresponding complementary data input line and responsive to said column selection signal to connect each of said pair of complementary data lines in the corresponding column to each of said pair of complementary data input lines, respectively, and a respective data detection circuit separate from the respective switching circuit for each column having a second drive terminal for receiving a signal corresponding to said column selection signal and directly connected to at least one of said pair of complementary data lines in the corresponding column and adapted, upon receipt of said signal corresponding to said column selection signal, to provide a signal corresponding to a data signal from said at least one complementary data line.

2. A semiconductor memory device according to Claim 1, wherein said plurality memory cells, said data detection circuit and said switching circuit are each constituted by insulated gate field effect transistors.

3. A semiconductor memory device according to Claim 2, wherein each said insulated gate field effect transistor is constituted by a field effect transistor having an aluminum gate electrode.

4. A semiconductor memory device according to Claim 2, wherein said insulated gate field effect transistor is constituted by a field effect transistor having a polycrystalline silicon gate electrode.

5. A semiconductor memory device according to any preceding claim, wherein said data detection circuit comprises a first series circuit including first and second switching elements and a second series circuit connected in series with said first series circuit and including third and fourth switching elements, said first and second series circuit being connected between a first-voltage receiving terminal for receiving a first specified voltage and a second-voltage receiving terminal for receiving a second specified voltage lower than said first specified voltage, said first and fourth switching elements being responsive to said column selection signal; and one of said

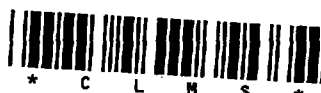
second and third switching elements being opened and the other switching element being closed upon receipt of a data signal from one of said pair of complementary data lines, whereby said second and third switching elements constitute an inverter having an input terminal connected to said one complementary data line and adapted to generate as an output signal an inverted signal of a data signal from said one complementary data line at a connection portion between said first and second series circuits.

6. A semiconductor memory device according to Claim 5, wherein said first and second switching elements are each constituted by a p channel type field effect transistor; said third and fourth switching elements are each constituted by an n channel type field effect transistor; and the gate electrodes of said field effect transistors constituting said first and fourth switching elements are supplied with a signal and an inverted signal thereof, respectively.

7. A semiconductor memory device according to Claim 5, wherein said data detection circuit further comprises a third series circuit including fifth and sixth switching elements and a fourth series circuit connected in series with said third series circuit and including seventh and eighth switching elements, said third and fourth series circuits being connected between said first-and second-voltage receiving terminals, said fifth and eighth switching elements being responsive to said column selection signal, and one of said sixth and seventh switching elements being opened and the other switching element being closed upon receipt of a data signal from the other of said pair of complementary data lines, whereby said sixth and seventh switching elements constitute an inverter having an input terminal connected to said other complementary data line and adapted to generate as an output signal an inverted signal of a data signal from said other complementary data line at a connection portion between said third and fourth series circuits.

8. A semiconductor memory device according to Claim 7, wherein said first, second, fifth and sixth switching elements are each constituted by a p channel type field effect transistor; said third, fourth, seventh and eighth switching elements are each constituted by an n channel type field effect transistor; and the gate electrodes of said field effect transistors constituting said first and fifth switching elements, are supplied with an inverted signal of a signal applied to the gate electrodes of said field effect transistors constituting said fourth and eighth switching elements.

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9. A semiconductor memory device according to any of Claims 1 to 4, which further comprises a first data output line and in which said data detection circuit includes a first series circuit including first and second switching elements connected in series between a first-voltage receiving terminal for receiving a first specified voltage and said first data output line, said first switching element being responsive to said column selection signal and said second switching element having a control terminal connected to one of said pair of complementary data lines, and a third switching element connected between said first data output line and a second-voltage receiving terminal for receiving a second specified voltage lower than said first specified voltage and commonly used by said plurality of memory cells, the third switching element being responsive to a chip selection signal.

10. A semiconductor memory device according to Claim 9, wherein said data detection circuit further includes a resistive element connected in parallel with said third switching element.

11. A semiconductor memory device according to Claim 10, wherein said resistive element is constituted by a field effect transistor.

12. A semiconductor memory device according to Claim 9, which further comprises a second complementary data output line and in which said data detection circuit further includes a second series circuit having fourth and fifth switching elements connected in series between said first-voltage receiving terminal and said second complementary data output line, said fourth switching element being responsive to said column selection signal and said fifth switching element having a control terminal connected to the other of said pair of complementary data lines, and a sixth switching element connected between said second complementary data output line and said second-voltage receiving terminal for receiving said second specified voltage by commonly used said plurality of memory cells, the sixth switching element being responsive to said chip selection signal.

13. A semiconductor memory device according to Claim 9, wherein said first and second switching element are each constituted by a p channel type field effect transistor, and said third switching element

is constituted by an n channel type field effect transistor.

14. A semiconductor memory device according to any of Claims 1 to 4, which further comprises a first data output line and in which said data detection circuit includes a first series circuit having first and second switching elements connected in series between a first-voltage receiving terminal for receiving a first specified voltage and said first data output line, said first switching element being responsive to said column selection signal and said second switching element having a control terminal connected to one of said pair of complementary data lines, and a third switching element connected between said first data output line and a second-voltage receiving terminal for receiving a second specified voltage higher than said first specified voltage and commonly used by said plurality of memory cells, the third switching element being responsive to a chip selection signal.

15. A semiconductor memory device according to Claim 14, wherein said data detection circuit further includes a resistive element higher connected in parallel with said third switching element.

16. A semiconductor memory device according to Claim 15, wherein said resistive element is constituted by a field effect transistor.

17. A semiconductor memory device according to Claim 14, wherein said first and second switching elements are each constituted by an n channel type field effect transistor, and said third switching element is constituted by a p channel type field effect transistor.

18. A semiconductor memory device according to Claim 14, which further comprises a second complementary data output line and in which said data detection circuit further includes a second series circuit having fourth and fifth switching elements connected in series between said first-voltage receiving terminal and said second complementary data output line, said fourth switching element being responsive to said column selection signal and said fifth switching element having a control terminal connected to the other of said pair of complementary data lines, and a sixth switching element connected between said second complementary data output line and said second-voltage receiving terminal for receiving said second specified voltage commonly used by said



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plurality of memory cells, the sixth switching element being responsive to said chip selection signal.

- 5 19. A semiconductor memory device, substantially as hereinbefore described with reference to the accompanying drawings.

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