

SPECIFICATION

Title of Invention: CONVEYANCE METHOD AND PROCESSING SYSTEM

5 **Technical Field**

[0001]

The present disclosure relates to a substrate transfer method and a processing system.

10 **Background**

[0002]

Patent Document 1 discloses a gas processing apparatus comprising: a chamber for performing desired gas processing on a substrate accommodated therein; a transfer mechanism for continuously transferring a plurality of substrates to the chamber; and a control mechanism for controlling introduction of a processing gas and operation of the transfer mechanism so that the processing gas is introduced into the chamber before loading the substrate into the chamber and the substrate is loaded into the chamber after a predetermined time.

Prior Art Documents

Patent Documents

25 [0003]

Patent Document 1: Japanese Laid-open Patent Publication

No. 2008-160000

Summary

Problems to Be Resolved by the Invention

5 [0004]

A technique according to the present disclosure appropriately adjusts a transfer timing of a plurality of substrates that are continuously processed in a substrate processing apparatus, and efficiently performs substrate
10 processing in the substrate processing apparatus.

Means for Solving the Problems

[0005]

One aspect of the present disclosure is, in a processing
15 system comprising at least one processing unit for performing desired processing on a substrate and a transfer unit for transferring the substrate to the processing unit, a method of transferring a plurality of substrates to be continuously processed from the transfer unit to the processing unit. An
20 adjustment value for arbitrarily changing a processing time for the substrate is assigned in advance to each of the plurality of substrates. The method includes: obtaining the adjustment value assigned to a first substrate to be processed at this time; obtaining a reference adjustment value assigned
25 to a reference substrate processed prior to the first substrate; obtaining an actual time, which is time for an

actual processing performed on the reference substrate;
calculating a predicted processing time for the first
substrate by reflecting a difference between the adjustment
value assigned to the first substrate and the reference
5 adjustment value in the actual time; and adjusting a transfer
timing of a second substrate to be processed after the first
substrate, based on the calculated predicted processing time.

Effect of the Invention

10 [0006]

According to the present disclosure, a transfer timing
of a plurality of substrates that are continuously processed
in a substrate processing apparatus is appropriately adjusted,
and substrate processing in the substrate processing
15 apparatus is efficiently performed.

Brief Description of the Drawings

[0007]

FIG. 1 is a plan view showing a schematic configuration
20 of a substrate processing apparatus according to the present
embodiment.

FIG. 2 is a flowchart showing main steps of a method for
controlling a transfer timing of a wafer according to the
present embodiment.

25 FIG. 3 is an explanatory diagram showing details of
recipe information recorded in a recipe database.

FIGS. 4A to 4E are explanatory diagram schematically showing how wafers are transferred according to the present embodiment.

5 **Detailed Description**

[0008]

Conventionally, there is known a vacuum processing apparatus that transfers a semiconductor wafer (substrate: hereinafter simply referred to as a "wafer") under a vacuum
10 atmosphere and performs various vacuum processes on the wafer. In this vacuum processing apparatus, transfer between various processing modules and various vacuum processing are sequentially and continuously performed for a plurality of wafers loaded into the vacuum processing apparatus.

15 [0009]

The above-mentioned Patent Document 1 discloses a gas processing apparatus that sequentially performs Chemical Oxide Removal (COR) processing and Post Heat Treatment (PHT) processing on a wafer as vacuum processing. According to the
20 gas processing apparatus disclosed in Patent Document 1, transfer of a wafer is controlled so that a plurality of wafers are continuously transferred to each processing chamber (processing module) according to instructions from a process controller.

25 [0010]

In the transfer of the wafer and various vacuum

processing, it is required to control a transfer timing of a wafer to various processing modules and to shorten processing standby time of the wafer in order to suppress a decrease in throughput in the vacuum processing apparatus.

5 [0011]

Conventionally, in this controlling the transfer timing of the wafer, a "recipe actual time" (hereinafter, simply referred to as an "actual time" in some cases) created by saving as a recipe a measurement time when performing a target vacuum processing (recipe) on a wafer (hereinafter, referred to as a "preceding wafer") processed prior to a current wafer (hereinafter, referred to as the "current wafer") for which the timing control is to be performed is used. Specifically, wafer transfer can be optimized by predicting a time required for the same recipe performed on the current wafer using the actual time of the preceding wafer on which the target recipe was performed and by controlling the transfer timing of the current wafer in accordance with a timing of the end of the recipe.

20 [0012]

By the way, the "actual time" for controlling the transfer timing of the wafer includes data (hereinafter, referred to as "variable data") for adjusting a processing time of the target recipe for the current wafer, for example, based on a processing result of previous processing of the current wafer, a processing result of the target recipe for

the preceding wafer, or the like. The variable data is assigned and set for each of a plurality of wafers loaded into the vacuum processing apparatus, for example, by manual input by an operator or automatic input based on the processing
5 result of the previous processing.

[0013]

However, in the above-described conventional method for controlling the transfer timing of the wafer, the variable data assigned to each wafer is not taken into consideration,
10 and there is a risk that the throughput decreases when the variable data differs between the preceding wafer and the current wafer. Specifically, the transfer timing of the current wafer is controlled based on the actual time of the preceding wafer as described above, but in this case, since
15 the current wafer is transferred on the assumption that the variable data of the preceding wafer and the current wafer are the same, there is a risk that the transfer timing is not correctly predicted and that processing standby time occur, resulting in a decrease in throughput. Patent Document 1 does
20 not disclose the decrease in throughput caused by such different variable data, and there is room for improvement from this point of view.

[0014]

The technique according to the present disclosure has
25 been made in view of the above circumstances, and appropriately adjusts a transfer timing of a plurality of

substrates that are continuously processed in a substrate processing apparatus and efficiently performs substrate processing in the substrate processing apparatus. Hereinafter, a vacuum processing apparatus according to one embodiment and a wafer transfer method according to this embodiment will be described with reference to the drawings. In this specification and drawings, elements having substantially the same functional configuration are denoted by the same reference numerals, thereby omitting redundant description.

[0015]

<Vacuum processing apparatus>

First, a configuration of a vacuum processing apparatus according to one embodiment will be described. FIG. 1 is a plan view schematically showing an outline of a configuration of a vacuum processing apparatus 1. In this embodiment, a case where the vacuum processing apparatus 1 comprises a COR module and a PHT module as processing modules will be described as an example. A configuration of various processing modules included in the vacuum processing apparatus 1 of the present disclosure is not limited to this, and may be arbitrarily selected.

[0016]

As shown in FIG. 1, the vacuum processing apparatus 1 has a configuration in which an atmospheric part 10 and a decompression part 11 are integrally connected via load lock

modules 20a and 20b. The atmospheric part 10 includes a plurality of atmospheric modules that perform desired processing on a wafer W in an atmospheric pressure atmosphere. The decompression part 11 includes a plurality of
5 decompression modules that perform desired processing on the wafer W in a decompressed atmosphere.

[0017]

The load lock module 20a temporarily holds the wafer W in order to deliver the wafer W transferred from a loader
10 module 30 of the atmospheric part 10, which will be described later, to a transfer module 60 of the decompression part 11, which will be described later. The load lock module 20a has a plurality of, for example, two stockers (not shown) inside, which hold two wafers W inside at the same time.

15 [0018]

The load lock module 20a is connected to the loader module 30 and the transfer module 60, which will be described later, via a gate (not shown) provided with a gate valve (not shown). This gate valve ensures airtightness and mutual
20 communication between the load lock module 20a and the loader module 30 and between the load lock module 20a and the transfer module 60.

[0019]

An air supply unit (not shown) for supplying gas and an
25 exhaust unit (not shown) for discharging gas are connected to the load lock module 20a, and the inside of the load lock

module 20a can be switched between an atmospheric pressure atmosphere and a decompressed atmosphere by the air supply unit and the exhaust unit. That is, the load lock module 20a is configured so that the wafer W can be transferred
5 appropriately between the atmospheric part 10 having an atmospheric pressure atmosphere and the decompression part 11 having a decompressed atmosphere.

[0020]

The load lock module 20b temporarily holds the wafer W
10 in order to deliver the wafer W transferred from the transfer module 60 to the loader module 30. The load lock module 20b has the same configuration as that of the load lock module 20a. That is, the load lock module 20b has a gate valve (not shown), a gate (not shown), an air supply unit (not shown),
15 and an exhaust unit (not shown).

[0021]

The number and arrangement of the load lock modules 20a and 20b are not limited to the present embodiment, and can be set arbitrarily.

20 [0022]

The atmospheric part 10 has a loader module 30 having a wafer transfer mechanism 40 to be described later, load ports 32 for placing FOUPs 31 capable of storing a plurality of wafers W, a CST module 33 for cooling the wafer W, and an
25 orienter module 34 for adjusting a horizontal orientation of the wafer W.

[0023]

The loader module 30 has a rectangular housing inside, and the inside of the housing is maintained at an atmospheric pressure atmosphere. A plurality of, for example, three load
5 ports 32 are arranged side by side on one side surface constituting long sides of the housing of the loader module 30. The load lock modules 20a and 20b are arranged side by side on the other side surface constituting the long sides of the housing of the loader module 30. The CST module 33 is
10 provided on one side surface constituting short sides of the housing of the loader module 30. The orienter module 34 is provided on the other side surface constituting the short sides of the housing of the loader module 30.

[0024]

15 The number and arrangement of the load ports 32, the CST modules 33, and the orienter modules 34 are not limited to the present embodiment, and can be set arbitrarily. Further, the type of atmospheric module provided in the atmospheric part 10 is not limited to the present embodiment, and can be
20 arbitrarily selected.

[0025]

The FOUP 31 accommodates a plurality of wafers W, for example, 25 wafers per lot. Further, the inside of the FOUP 31 placed on the load port 32 is filled with air, nitrogen
25 gas, or the like, for example, and sealed.

[0026]

The wafer transfer mechanism 40 for transferring the wafer W is provided inside the loader module 30. The wafer transfer mechanism 40 has transfer arms 41a and 41b that hold and move the wafer W, a rotating stand 42 that rotatably supports the transfer arms 41a and 41b, and a rotating placing stand 43 on which the rotating stand 42 is mounted. The wafer transfer mechanism 40 is configured to be movable in a longitudinal direction inside the housing of the loader module 30.

10 [0027]

The decompression part 11 has the transfer module 60 for simultaneously transferring two wafers W to various processing modules, COR modules 61 for performing COR processing on the wafers W, and PHT modules 62 for performing PHT processing on the wafers W. The insides of the transfer module 60, the COR module 61, and the PHT module 62 are each maintained in a decompressed atmosphere. Further, a plurality of COR modules 61 and PHT modules 62 are provided for each transfer module 60, for example, three each.

20 [0028]

The transfer module 60 as a transfer unit is made up of a rectangular housing inside, and is connected to the load lock modules 20a and 20b via gate valves (not shown) as described above. The transfer module 60 sequentially transfers the wafer W loaded into the load lock module 20a to one COR module 61 and one PHT module 62 for COR processing

and PHT processing, and then unloads the wafer W to the atmospheric part 10 via the load lock module 20b.

[0029]

Two stages 61a and 61b on which two wafers W are
5 horizontally placed side by side are provided inside the COR
module 61 as a processing unit. The COR module 61 performs
COR processing on two wafers W at the same time by placing
the wafers W side by side on the stages 61a and 61b. An air
supply unit (not shown) for supplying processing gas, purge
10 gas, or the like and an exhaust unit (not shown) for
discharging gas are connected to the COR module 61.

[0030]

Two stages 62a and 62b on which two wafers W are
horizontally placed side by side are provided inside the PHT
15 module 62 as a processing unit. The PHT module 62 performs
PHT processing on two wafers W at the same time by placing
the wafers W side by side on the stages 62a and 62b. An air
supply unit (not shown) for supplying gas and an exhaust unit
(not shown) for discharging gas are connected to the PHT
20 module 62.

[0031]

Further, the COR module 61 and the PHT module 62 are
connected to the transfer module 60 via a gate (not shown)
provided with a gate valve (not shown). This gate valve
25 ensures airtightness and mutual communication between the
transfer module 60 and the COR module 61 and between the

transfer module 60 and the PHT module 62.

[0032]

The number, arrangement, and types of processing modules provided in the transfer module 60 are not limited to those
5 of the present embodiment, and can be set arbitrarily.

[0033]

A wafer transfer mechanism 70 for transferring the wafer W is provided inside the transfer module 60. The wafer transfer mechanism 70 has transfer arms 71a and 71b for
10 holding and moving two wafers W vertically, a rotating stand 72 for rotatably supporting the transfer arms 71a and 71b, and a rotating placing stand 73 on which the rotating stand 72 is mounted. Further, a guide rail 74 extending in a longitudinal direction of the transfer module 60 is provided
15 inside the transfer module 60. The rotating placing stand 73 is provided on the guide rail 74 so that the wafer transfer mechanism 70 can move along the guide rail 74.

[0034]

A controller 80 is provided in the vacuum processing
20 apparatus 1 described above. The controller 80 is, for example, a computer equipped with a Central Processing Unit (CPU), memory, or the like, and has a program storage unit (not shown). A program for controlling processing on the wafer W in the vacuum processing apparatus 1 is stored in the
25 program storage unit. Further, the program storage unit also stores a program for controlling operations of the various

processing modules described above and drive systems such as the transfer mechanism to control the transfer timing of the wafer in the vacuum processing apparatus 1, which will be described later. Specifically, for example, a "wafer transfer control task" for controlling a transfer operation of the wafer, which will be described later, a "recipe execution control task" for executing a recipe in the processing module, which will be described later, a "recipe management task" for managing the recipe in the processing module, which will be described later, and the like are stored. The program may be recorded in a computer-readable storage medium H and installed in the controller 80 from the storage medium H.

[0035]

<Wafer Transfer Method>

The vacuum processing apparatus 1 according to the present disclosure is configured as described above. Next, wafer processing and wafer transfer performed using the vacuum processing apparatus 1 will be described. In the following description, an example will be described in which wafers W of one lot (25 wafers) accommodated in the FOUP 31 are continuously processed two by two. Further, "wafers W1 to W25" used in the following description mean that the wafers W of one lot (25 wafers) are numbered 1 to 25 in order of wafer processing.

[0036]

Further, in normal wafer processing, the wafers W are

processed in parallel using the plurality of COR modules 61 and PHT modules 62 provided in the decompression part 11, but in the following description, in order to clarify the description of controlling the transfer timing of the wafer, a case where all the wafers W1 to W25 are processed using the same COR module 61 and PHT module 62 will be described as an example.

[0037]

First, the FOUP 31 containing a plurality of wafers W, that is, the wafers W of one lot (25 wafers) is loaded into the load port 32. When the FOUP 31 is placed on the load port 32, the wafer transfer mechanism 40 accesses the FOUP 31 and takes out the wafer W1 from the FOUP 31. The horizontal orientation of the wafer W1 unloaded from the FOUP 31 is adjusted by the orienter module 34. Next, the wafer W2 is taken out from the FOUP 31 while adjusting the horizontal orientation of the wafer W1.

[0038]

The wafer W2 taken out from the FOUP 31 is loaded into the orientor module 34 and its horizontal orientation is adjusted immediately after the wafer W1 whose horizontal orientation has been adjusted is taken out from the orienter module 34.

[0039]

The wafer W1 taken out from the orienter module 34 is transferred to a stocker (not shown) of the load lock module

20a and temporarily held. Similarly, the wafer W2 whose horizontal orientation has been adjusted is taken out from the orienter module 34 and transferred to the stocker (not shown) of the load lock module 20a.

5 [0040]

When the two wafers W1 and W2 are transferred to the load lock module 20a, the inside of the load lock module 20a is switched from an atmospheric pressure atmosphere to a decompressed atmosphere, and then communicated with the
10 inside of the transfer module 60. Subsequently, the two wafers W1 and W2 are transferred to the transfer arm 71a of the wafer transfer mechanism 70 and loaded into the transfer module 60.

[0041]

15 The wafer transfer mechanism 70 holding the two wafers W1 and W2 next moves to a position in front of one COR module 61. Subsequently, the transfer arm 71a enters the inside of the COR module 61, and the two wafers W1 and W2 are transferred to the stages 61a and 61b of the COR module 61, respectively.
20 After that, the transfer arm 71a is withdrawn from the COR module 61, and the COR processing is performed on the two wafers W1 and W2. In the COR processing according to the present embodiment, at least one recipe is selectively executed according to the purpose from among a plurality of
25 recipes for COR processing recorded in a recipe database DB, which will be described later.

[0042]

When the COR processing of the two wafers W1 and W2 is started, two wafers W3 and W4 to be processed next are taken out from the FOUP 31, loaded into the load lock module 20a via the orienter module 34, and then further transferred to a position in front of one COR module 61 by the wafer transfer mechanism 70. Here, the transfer timing of the two wafers W3 and W4 to the one COR module 61 is controlled so that the wafers W3 and W4 arrive at a position in front of the one COR module 61 at a timing when the COR processing for the two wafers W1 and W2, which are the preceding wafers, is completed. That is, the transfer timing is controlled so that the unloading of the wafers W1 and W2 from one COR module 61 and the loading of the wafers W3 and W4 into the same COR module 61 can be performed at the same time. The details of the method of controlling the transfer timing will be described later.

[0043]

Subsequently, when the COR processing for the wafers W1 and W2 is completed, the transfer arm 71b of the wafer transfer mechanism 70 enters the inside of the COR module 61, and the two wafers W1 and W2 are transferred from the stages 61a and 61b to the transfer arm 71b. Subsequently, the transfer arm 71a of the wafer transfer mechanism 70 enters the inside of the COR module 61, and the two wafers W3 and W4 are transferred from the transfer arm 71a to the stages 61a

and 61b. After that, the transfer arm 71a is withdrawn from the COR module 61, and the COR processing is performed on the two wafers W3 and W4.

[0044]

5 Next, the wafer transfer mechanism 70 holding the two wafers W1 and W2 moves to a position in front of one PHT module 62. Subsequently, the transfer arm 71b enters the PHT module 62, and the two wafers W1 and W2 are transferred to the stages 62a and 62b of the PHT module 62, respectively.
10 After that, the transfer arm 71b is withdrawn from the PHT module 62, and the PHT processing is performed on the two wafers W1 and W2. In the PHT processing according to the present embodiment, at least one recipe is selectively executed according to the purpose from among a plurality of
15 recipes for PHT processing recorded in a recipe database DB, which will be described later.

[0045]

 Subsequently, when the PHT processing for the wafers W1 and W2 is completed, the transfer arm 71b of the wafer
20 transfer mechanism 70 enters the inside of the PHT module 62, and the two wafers W1 and W2 are transferred from the stages 62a and 62b to the transfer arm 71b. At this time, it is preferable to transfer the two wafers W3 and W4 for which the COR processing has been completed to the stages 62a and 62b
25 of the PHT module 62. That is, it is preferable that the unloading of the wafers W1 and W2 from the PHT module 62 and

the loading of the wafers W3 and W4 into the same PHT module 62 are performed at the same time. Further, at this time, it is more preferable that the unloading of the wafers W3 and W4 from the COR module 61 and the loading of two wafers W5 and W6 to be processed next into the same COR module 61 are performed at the same time. As described above, the details of the method of controlling the transfer timing will be described later.

[0046]

10 After the two wafers W1 and W2 are unloaded from the PHT module 62, the wafer transfer mechanism 70 holding the two wafers W1 and W2 moves to a position in front of the load lock module 20b. Subsequently, the two wafers W1 and W2 are transferred from the transfer arm 71b of the wafer transfer
15 mechanism 70 to the stocker (not shown).

[0047]

 When the two wafers W1 and W2 are transferred to the load lock module 20b, the inside of the load lock module 20b is switched from a decompressed atmosphere to an atmospheric
20 pressure atmosphere, and then communicated with the inside of the loader module 30. Subsequently, the two wafers W1 and W2 are transferred to the wafer transfer mechanism 40 and loaded into the loader module 30. After that, the two wafers W1 and W2 are stored in the CST module 33 by the loader module 30,
25 and CST processing is performed.

[0048]

When the CST processing for a predetermined time (e.g., 1 minute) is completed, the two wafers W1 and W2 transferred to the CST module 33 are stored in the FOUP 31 placed on the load port 32 by the loader module 30 and then remain in a standby state until processing for the other wafers W3 to W25 is completed.

[0049]

In this way, a series of orientation processing, COR processing, PHT processing, and CST processing are sequentially performed on all the wafers W1 to W25. When desired processing for all the wafers W1 to W25 is completed and the last wafer W25 is stored in the FOUP 31, a series of wafer processing in the vacuum processing apparatus 1 ends.

[0050]

Wafer processing and wafer transfer in the vacuum processing apparatus 1 according to the present embodiment are performed as described above. As described above, it is desirable that the transfer timing of the wafer is controlled so that the unloading of the preceding wafers from one processing module and the loading of the current wafers into the same processing module are performed at the same time. However, especially when the variable data assigned to each wafer is different between the preceding wafers and the current wafers, it may not be possible to accurately predict an end timing of the recipe in one processing module and to appropriately control the transfer timing.

[0051]

Here, if the transfer timing of the current wafers is so early that the current wafers are transferred to the front of the processing module while the recipe for the preceding wafers in the processing module is being continued, the current wafers wait on the transfer arm 71 of the wafer transfer mechanism 70 until processing of the preceding wafers is completed. In general, as described above, in the vacuum processing apparatus 1, since a plurality of wafers W loaded from a plurality of FOUPs 31 are processed in parallel using a plurality of processing modules, if the current wafers wait on the transfer arm 71 as described above, the transfer arm 71 cannot transfer the other wafers W during this time. That is, the other wafers W cannot be processed during this time, and the throughput of the vacuum processing apparatus 1 is thereby lowered.

[0052]

On the other hand, if the transfer timing of the current wafers is so late that the current wafers are not transferred to the front of the processing module even if the recipe for the preceding wafers in the processing module is completed, the preceding wafers cannot be unloaded from the processing module and waits inside the processing module. When the preceding wafers wait as described above, the other wafers W cannot be processed in the processing module during this time, resulting in a decrease in the throughput. Further, when the

preceding wafers wait inside the processing module in this way, due to the influence of residual gas inside the processing module, the processing for the preceding wafers may proceed excessively, and a desired processing result may
5 not be obtained for the preceding wafers.

[0053]

In this way, when the transfer timing of the wafer cannot be appropriately controlled, there is a risk of a decrease in throughput or a problem in the processing results of the
10 preceding wafers. For this reason, the transfer timing of the wafer is preferably controlled so that the current wafers arrive at a position in front of the processing module between 5 seconds before and 5 seconds after the recipe of the preceding wafers is completed in the processing module, or
15 more preferably controlled so that the current wafers arrive at a position in front of the processing module approximately at the same time as the completion of the recipe of the preceding wafers.

[0054]

20 Next, the details of the method of controlling the transfer timing of the wafer W in the vacuum processing apparatus 1 described above will be described. In the following description, a case where a set time for the COR processing in the COR module 61 is t seconds and a set time
25 for the PHT processing in the PHT module 62 is T seconds ($t < T$), that is, a case where the PHT processing is longer than the

COR processing and the processing in the vacuum processing apparatus 1 in the PHT module 62 is rate-limited will be described as an example.

[0055]

5 FIG. 2 is a flowchart simply showing a series of flows of controlling the transfer timing of the wafer according to the present embodiment. As shown in FIG. 2, the above-described "wafer transfer control task", "recipe execution control task", and "recipe management task" are used in
10 controlling the transfer timing according to the present embodiment. Further, FIG. 3 is an explanatory diagram schematically showing details of recipe information recorded in the recipe database DB.

[0056]

15 First, prior to starting the processing for the wafers W in the vacuum processing apparatus 1, a transfer plan for two wafers W1 and W2 to be processed first by the wafer transfer control task is established (sequence S1 in FIG. 2).

[0057]

20 When establishing the transfer plan, the variable data V assigned to the two wafers W1 and W2 is acquired. The variable data V is an adjustment value that is set for each processing step time of various vacuum processing performed on the wafers W1 and W2, and that is input to arbitrarily
25 adjust an execution time of this processing step. By changing this variable data, the execution time of a corresponding

processing step for any wafer W can be changed arbitrarily.

[0058]

A case where the execution time of the corresponding processing step for the wafer W is changed by changing the variable data V is described as an example in the present embodiment, but the variable data V can also control other conditions related to the processing of the wafer W, for example, a flow rate or temperature of gas, and the like.

[0059]

Further, when establishing the transfer plan, the wafers W1 and W2 for which the transfer plan is to be established are set as the current wafers, and a recipe actual time during transfer of the preceding wafers for which the same recipe was executed before the wafers W1 and W2 and the variable data V assigned to the preceding wafers are acquired. The actual time and the variable data V of the preceding wafers are acquired by, for example, the recipe management task referring to the recipe database DB in which the actual time (measured processing time) of various recipes in previous execution and the variable data V are recorded in pairs.

[0060]

When the variable data V of the wafers W1 and W2 (current wafers) and the actual time and the variable data V of the preceding wafers are acquired, next, a recipe processing time required when the recipe is executed for the wafers W1 and W2 is predicted based on the various data acquired in the

sequence S1 (sequence S2 in FIG. 2).

[0061]

Specifically, when the variable data V differs between the preceding wafers and the current wafers, the recipe processing time of the preceding wafers and the current wafers fluctuates according to the variable data V difference. That is, for example, in a case where the variable data V of the preceding wafers is 10 seconds and the variable data V of the current wafers is 20 seconds, the recipe processing time for the current wafers is predicted to be 10 seconds longer than the recipe processing time for the preceding wafers. Therefore, in controlling the transfer timing of the wafer according to the present embodiment, the recipe processing time for the current wafers is predicted by the following Equation (1).

[0062]

Recipe Processing Time for Current Wafers [sec] = Actual Time for Preceding Wafers [sec] + (Variable Data V of Current Wafers [sec] - Variable Data V of Preceding Wafers [sec]) ... (1)

[0063]

In the present embodiment, the recipe processing time for the current wafers is predicted in consideration of the difference in the variable data V between the preceding wafers and the current wafers, as described above. By controlling and adjusting the transfer timing of the current wafers as

described later based on the recipe processing time predicted as described above, it is possible to suppress a decrease in processing throughput in the vacuum processing apparatus 1 even if the variable data V differs between the wafers W that are processed continuously.

[0064]

When the recipe processing time for the wafers W1 and W2 is predicted, the two wafers W1 and W2 for which the transfer plan has been established start to be transferred to various processing modules (sequence S4 in FIG. 2), and sequentially, the COR processing and the PHT processing are performed (sequence S5 in FIG. 2). Further, when transferring the wafers to the various processing modules, the wafer transfer control task provides the recipe execution control task with the recipe for the wafers W1 and W2 and the variable data V set as various processing data. Since the wafers W1 and W2 are the first wafers to be processed in the lot, the transfer timing shown in the sequence S3 in FIG. 2 is not adjusted.

[0065]

When the transfer of the two wafers W1 and W2 and the recipes in the various modules are started, a transfer plan for the two wafers W3 and W4 to be processed next is established (sequence S1 in FIG. 2), and a recipe processing time for the wafers W3 and W4 is predicted (sequence S2 in FIG. 2).

[0066]

A method of establishing the transfer plan and predicting the recipe processing time for the wafers W3 and W4 are the same as those for the wafers W1 and W2. That is, after acquiring the variable data V assigned to the wafers W3 and W4 and the actual time for the preceding wafers and the variable data V recorded in the recipe database DB, the recipe processing time for the wafers W3 and W4 as the current wafers is predicted based on the above Equation (1).

10 [0067]

When the recipe processing time for the wafers W3 and W4 is predicted, based on the established transfer plan and a transfer state (sequence S4) and a processing state (sequence S5) of the two wafers W1 and W2 to be processed earlier, the transfer timing of the two wafers W3 and W4 to various processing modules is adjusted (sequence S3 in FIG. 2).

[0068]

The relationship between the transfer and processing states (sequences S4 and S5) of the two wafers W1 and W2 and the adjustment of the transfer timing of the two wafers W3 and W4 will be specifically described. FIG. 4 is an explanatory diagram showing how the wafers are transferred in the vacuum processing apparatus 1 over time.

25 [0069]

When the recipe processing time for the wafers W1 and

W2 is predicted in the sequence S3, as shown in FIG. 4A, the two wafers W1 and W2 for which the transfer plan has been established are taken out from the FOUP 31 and loaded into one COR module 61 via the load lock module 20a, and the COR processing is performed for t seconds. This COR processing includes a plurality of processing steps as also shown in the recipe database DB in FIG. 3. The processing time of t seconds for the COR processing described above indicates the recipe processing time as a total time of these plurality of processing steps as shown in FIG. 3.

[0070]

When the COR processing for the two wafers W1 and W2 is completed, the two wafers W1 and W2 are transferred to the PHT module 62 as shown in FIG. 4B. In the present embodiment, since the PHT processing is longer than the COR processing and the processing is rate-limited in the PHT module 62, the two wafers W1 and W2 for which the COR processing has been completed are loaded into the PHT module 62 without waiting for the two wafers W3 and W4 to be processed next.

[0071]

When the two wafers W1 and W2 are loaded into the PHT module 62, the PHT processing for T seconds is started. This processing time of T seconds for the PHT processing indicates the recipe processing time as a total time of a plurality of processing steps as shown in FIG. 3.

[0072]

When the PHT processing for the wafers W1 and W2 is started, the wafers W3 and W4 are then transferred to a position in front of the PHT module 62 via the load lock module 10a and the COR module 61. Here, the arrival timing of the wafers W3 and W4 at the position in front of the PHT module 62 is preferably between 5 seconds before and 5 seconds after the completion of the PHT processing of the preceding wafers (wafers W1 and W2), more preferably substantially simultaneously with the completion of the recipe for the preceding wafers, as described above. Therefore, in controlling the transfer timing of the wafer in the present embodiment, a transfer start timing of the current wafers (wafers W3 and W4) from the FOUP 31 is controlled based on the following Equation (2).

[0073]

$$X = \text{Remaining time of recipe being executed for preceding wafers} - \text{Time required for transferring current wafers to position in front of target processing module} \dots (2)$$

[0074]

In Equation (2), the "Remaining time of recipe being executed for preceding wafers" indicates a remaining time of the PHT processing on the two wafers W1 and W2 in the PHT module 62, for example. Further, the "Time required for transferring current wafers to position in front of target processing module" indicates a time required for transferring the wafers W3 and W4 from the FOUP 31 to a position in front

of the PHT module 62 via the load lock module 10a and the COR module 61, for example.

[0075]

5 In the present embodiment, when a calculation result of Equation (2) is 0 or more ($X \geq 0$), that is, when the remaining time of the PHT processing for the wafers W1 and W2 is longer than the time required to transfer the wafers W3 and W4, the transfer of the wafers W3 and W4 is not started. In other words, if there is a possibility that a waiting time of the wafers W3 and W4 in front of the PHT module 62 occurs, the transfer of the wafers W3 and W4 is not started, and the wafers W3 and W4 wait inside the FOUP 31 until a timing at which the waiting time of the wafers W3 and W4 in front of the PHT module 62 does not occur. On the other hand, when 10 the calculation result of Equation (2) is otherwise ($X < 0$), that is, when the time required to transfer the wafers W3 and W4 is longer than the remaining time of the PHT processing for the wafers W1 and W2, the transfer of the wafers W3 and W4 is immediately started. In other words, when the waiting 15 time of the wafers W3 and W4 in front of the PHT module 62 does not occur and the waiting time of the wafers W1 and W2 inside the PHT module 62 occurs, the transfer of the wafers W3 and W4 is started.

[0076]

25 In the present embodiment, by controlling the transfer start timing of the current wafers based on the remaining time

of the recipe for the preceding wafers and the time required to transfer the current wafers in this way, a decrease in throughput in the vacuum processing apparatus 1 can be appropriately suppressed. Further, the remaining time of the recipe used for adjusting the transfer timing is calculated based on the prediction result of the recipe processing time for the preceding wafers calculated in the sequence S2 in FIG. 2. That is, since the transfer start timing is controlled based on the prediction result of the recipe processing time calculated in consideration of the variable data V assigned to the wafer W, even if the variable data V differs between the wafers W that are continuously processed, it is possible to appropriately suppress a decrease in processing throughput in the vacuum processing apparatus 1.

15 [0077]

When the transfer timing of the two wafers W3 and W4 is adjusted (sequence S3 in FIG. 2), the two wafers W3 and W4 start to be transferred to various processing modules and processed (sequences S4 and S5 in FIG. 2), and are transferred to the front of the PHT module 62 as shown in FIG. 4C.

[0078]

Then, when the PHT processing for the wafers W1 and W2 is completed, as shown in FIG. 4D, the wafers W1 and W2 are unloaded from the PHT module 62 and then the wafers W3 and W4 are loaded into the PHT module 62 .

25 [0079]

After that, the wafers W1 and W2 unloaded from the PHT module 62 are transferred to the CST module 33 via the load lock module 20b as shown in FIG. 4E. After that, the wafers W1 and W2 are further transferred to the FOUP 31 by the wafer transfer mechanism 40, thereby completing a series of wafer processing for the wafers W1 and W2.

[0080]

When the wafer processing for the wafers W1 and W2 is completed, a time actually required for various processing for the wafers W1 and W2 (recipe actual time of the wafers W1 and W2) and the variable data V assigned to the wafers W1 and W2 are stored in the recipe database DB shown in FIG. 2 (sequence S6 in FIG. 2). More specifically, data of the recipe database DB related to a target recipe is overwritten and updated with the recipe actual time and the variable V of the wafers W1 and W2. The overwritten and updated actual time in the recipe database DB and the variable data V are referred to next time the wafers W are processed according to the same recipe.

[0081]

Meanwhile, when the two wafers W3 and W4 are transferred and the recipes in the various modules are started (sequence S4 and S5 in FIG. 2), as shown in FIG. 4E, a transfer plan for the two wafers W5 and W6 to be processed next is established (sequence S1 in FIG. 2), and a recipe processing time for the wafers W5 and W6 is predicted (sequence S2 in

FIG. 2). Further, based on the established transfer plan and the transfer state (sequence S4) and the processing state (sequence S5) of the two wafers W3 and W4 to be processed earlier, a transfer timing of the two wafers W5 and W6 to various processing modules is adjusted (sequence S3 in FIG. 2), and then the two wafers W5 and W6 are transferred and the recipes in the various modules are started (sequences S4 and S5 in FIG. 2).

[0082]

10 In the present embodiment, after all the wafers W of one lot (25 wafers) are transferred and processed by the same method as the above-described method shown in FIGS. 2 and 4 in this way, when all the wafers W1 to W25 are transferred to the FOUP 31, a series of wafer processing in the vacuum processing apparatus 1 is completed. In a case where all the wafers W1 to W25 are processed with the same recipe, after the series of wafer processing is completed, an actual time and variable data V of the last processed wafer W25 are recorded in the recipe database DB.

20 [0083]

The control of the transfer timing of the wafer according to the present embodiment is performed as described above. In the above embodiment, for clarification of description, the case where a plurality of wafers W are processed using only one COR module 61 and one PHT module 62 has been described as an example. However, by processing the

wafers W in parallel by a plurality of COR modules 61 and PHT modules 62, throughput in the vacuum processing apparatus 1 can be of course improved.

[0084]

5 As described above, according to the control method of the transfer timing of the wafer according to the present embodiment, the recipe processing time of the wafer W to be processed in the vacuum processing apparatus 1 is calculated according to the above Equation (1) in consideration of a
10 variation of the variable data V, which is an adjustment value (variable) that is arbitrarily input. As a result, even if the variable data V differs between the preceding wafers and the current wafers, it is possible to calculate the processing time for each processing step to be performed on the wafer W
15 or the recipe processing time as the total time of a plurality of processing steps in consideration of the difference in the variable data V appropriately. In other words, a completion timing of the recipe for the current wafers can be calculated in consideration of the difference in the variable data V, so
20 that the transfer timing of the wafer W can be appropriately determined.

[0085]

 Since the transfer timing of the wafer W can be appropriately determined in this way, the waiting time of the
25 current wafers on the transfer arm and the waiting time of the preceding wafers inside the processing module can be

reduced. As a result, especially when using a plurality of processing modules in parallel, a time during which the transfer arm is in a standby state while holding the wafer and cannot transfer the other wafers is reduced, and a decrease in throughput in the vacuum processing apparatus 1 is suppressed. Further, a decrease in throughput and an excessive progress of processing for the preceding wafers due to a waiting time of the preceding wafers inside the processing module are suppressed.

10 [0086]

Further, since the transfer timing of the wafer W can be appropriately determined in this way, the unloading of the preceding wafers from one processing module and the loading of the current wafers into the same processing module can be performed at the same time. Accordingly, the number of times the wafer transfer mechanism moves to the front of one processing module can be reduced, and as a result, a decrease in throughput in the vacuum processing apparatus 1 is suppressed more appropriately.

20 [0087]

Further, according to the above embodiment, the recipe actual time and the variable data V of the current wafers are recorded by overwriting in the recipe database DB in which the actual time and the variable data V of the preceding wafers used for controlling the transfer timing of the wafer are recorded. Although the recipe processing time for the

wafer W may change due to, for example, changes in device characteristics of the processing module, by updating the recipe database DB by overwriting in this way, it is possible to always refer to the latest data of the preceding wafers and calculate the recipe processing time. That is, the recipe processing time can be calculated by updating changes in device characteristics and the like over time.

[0088]

In the above embodiment, the transfer plan for the wafers W is established sequentially for the wafers W before being unloaded from the FOUP 31, but the timing for establishing the transfer plan for the wafers W is not limited to this. That is, in the above embodiment, the transfer of the wafer W (unloading from the FOUP 31) is started after the transfer plan for the entire series of wafer processing is established, but the transfer plan for the wafers W may be established before transferring the wafers W to various processing modules. Specifically, for example, the transfer plan for the COR module 61 may be established for the wafers W waiting inside the FOUP 31, and then the transfer plan for the PHT module 62 may be further established for the wafer W on which the COR processing is being performed.

[0089]

In the above embodiment, the case where the COR processing in the COR module 61 is shorter than the PHT processing in the PHT module 62 (rate-limited by the PHT

processing) has been described as an example. However, of course, even when the COR processing is longer than the PHT processing (rate-limited by the COR processing), or even when the COR processing and the PHT processing have the same processing time, the control of the transfer timing of the wafer according to the technique of the present disclosure can be performed.

[0090]

As also shown in the recipe database DB of FIG. 3, the COR processing in the COR module 61 and the PHT processing in the PHT module 62 include a plurality of processing steps. The processing steps include a "time step" for performing processing at a predetermined set time, and a "stabilization step" for performing processing until a predetermined processing result (for example, temperature, pressure, and the like) is reached.

[0091]

In this stabilization step, even if the variable data V differs between the preceding wafers and the current wafers as described above, since the time until a predetermined processing result is obtained is used as the actual time, there is little risk of a decrease in throughput due to fluctuations in the variable data V. On the other hand, in the time step, if the variable data V differs between the preceding wafers and the current wafers as described above, since the actual recipe processing time is used as the actual

time, there is a high possibility that throughput will decrease due to fluctuations in the variable data V.

[0092]

Therefore, in controlling the transfer timing of the wafer according to the present embodiment, the timing control described above may be performed only in the processing steps related to the "time step" among the plurality of processing steps included in the recipe applied to the wafers W. By reducing the number of processing steps for which the timing control is performed in this way, control of processing in the vacuum processing apparatus 1 can be simplified. However, of course, the timing control described above may also be performed for the processing steps related to the "stabilization step".

[0093]

In the above embodiment, although the case of controlling the transfer timing of the wafer in the vacuum processing apparatus 1 that processes the wafer W under the decompressed atmosphere has been described as an example, the configuration of the wafer processing apparatus to which the technique according to the present disclosure is applied is not limited as long as the wafers W are continuously transferred to the plurality of processing modules and processed. That is, for example, in an atmospheric processing apparatus that continuously performs a plurality of processing under atmospheric pressure, the control of the

transfer timing of the wafer according to the technique of the present disclosure may be performed.

[0094]

Further, although the case where two wafers W are transferred and processed at the same time has been described as an example in the above embodiment, the control of the transfer timing of the wafer according to the technique of the present disclosure can be applied even in a case where the wafer W is processed singly, or three or more wafers are processed.

[0095]

It should be considered that the embodiments disclosed this time are illustrative in all respects and not restrictive. The embodiments described above may be omitted, substituted, or modified in various ways without departing from the scope and spirit of the appended claims.

Description of Reference Numerals

[0096]

1: vacuum processing apparatus
V: variable data
W: wafer

CLAIMS

[Claim 1]

A method of transferring a plurality of substrates to
5 be continuously processed from a transfer unit to a processing
unit in a processing system comprising at least one processing
unit for performing desired processing on a substrate and the
transfer unit for transferring the substrate to the processing
unit, wherein each of the plurality of substrates is assigned
10 in advance with an adjustment value for arbitrarily changing
a processing time for the substrate, the method comprising:

obtaining the adjustment value assigned to a first
substrate to be processed at this time;

obtaining a reference adjustment value assigned to a
15 reference substrate processed prior to the first substrate;

obtaining an actual time, which is time for an actual
processing performed on the reference substrate;

calculating a predicted processing time for the first
substrate by reflecting a difference between the adjustment
20 value assigned to the first substrate and the reference
adjustment value in the actual time; and

adjusting a transfer timing of a second substrate to be
processed after the first substrate, based on the calculated
predicted processing time.

25

[Claim 2]

The method of claim 1,

wherein in adjusting the transfer timing of the second substrate, a transfer start timing of the second substrate is adjusted by comparing a predicted end time of processing for the first substrate in a processing module, which is
5 calculated from the predicted processing time, and a transfer time of the second substrate to the processing module.

[Claim 3]

10 The method of claim 2, wherein the transfer start timing is adjusted so that the second substrate is transferred to the processing module between 5 seconds before and 5 seconds after the predicted end time.

15 [Claim 4]

The method of claim 2 or 3, wherein the processing system is provided with a plurality of processing modules for performing various types of processing on the substrate, and
the processing module for which the transfer start
20 timing is adjusted is a processing module among the plurality of processing modules that requires a long processing time for the substrate and causes rate-limiting in processing of the substrate in the processing system.

25 [Claim 5]

The method of any one of claims 1 to 4, further comprising:

overwriting and updating the adjustment value assigned to the first substrate with the reference adjustment value
5 after the processing for the first substrate is completed.

[Claim 6]

A processing system for continuously processing a plurality of substrates, the system comprising:

10 at least one processing unit for performing desired processing on a substrate;

a transfer unit for transferring the substrate to the processing unit; and

a controller for controlling a substrate transfer
15 operation from the transfer unit to the processing unit,

wherein each of the plurality of substrates is assigned in advance with an adjustment value for arbitrarily changing a processing time for the substrate, and

the controller controls the substrate transfer operation
20 to perform:

obtaining the adjustment value assigned to a first substrate to be processed at this time;

obtaining a reference adjustment value assigned to a reference substrate processed prior to the first substrate;

25 obtaining an actual time, which is time for an actual processing performed on the reference substrate;

calculating a predicted processing time for the first substrate by reflecting a difference between the adjustment value assigned to the first substrate and the reference adjustment value in the actual time; and

5 adjusting a transfer timing of a second substrate to be processed after the first substrate, based on the calculated predicted processing time.

[Claim 7]

10 The system of claim 6, wherein in adjusting the transfer timing of the second substrate, the controller adjusts a transfer start timing of the second substrate by comparing a predicted end time of processing for the first substrate in the processing unit, which is calculated from the predicted
15 processing time, and a transfer time of the second substrate to the processing unit.

[Claim 8]

20 The system of claim 7, wherein the controller adjusts the transfer start timing so that the second substrate is transferred to the processing unit between 5 seconds before and 5 seconds after the predicted end time.

[Claim 9]

The system of claim 7 or 8, wherein a plurality of the processing units are provided adjacent to the transfer unit, and

5 the processing unit for which the transfer start timing is adjusted is a processing unit among the plurality of processing units that requires a long processing time for the substrate and causes rate-limiting in processing of the substrate in the processing system.

10 [Claim 10]

The system of any one of claims 6 to 9, wherein the controller overwrites and updates the adjustment value assigned to the first substrate with the reference adjustment value after the processing for the first substrate is
15 completed.