Optical read/write apparatus.

The invention relates to an apparatus as defined in the preamble of Claim 1.

The invention further relates to a signal processing unit as defined in the preamble of Claim 7.

Such an optical read/write apparatus is known from EP 508 522. The requirements imposed on the processing of the low frequency components and the high frequency components of the detected signal differ substantially. The position of the detector and the alignment of the optical system are controlled by means of a control signal derived from the low frequency components of the detected signal. For this, an accurate and offset-free amplification are important. For the high frequency components, from which the information signal is derived, a comparatively large bandwidth and a relatively constant group delay are required. Said European Patent Specification proposes an optical read/write apparatus in which the high frequency components and the low frequency components are separated from one another by means of a filter having a resistor arranged between the common input terminal and the first input terminal and having a capacitor arranged between the first input terminal and the second input terminal. Subsequently, the high frequency components and the low frequency components are processed separately.

US 4,663,749 describes an optical read/write apparatus in which the low frequency components are amplified by a current amplifier whose input current also constitutes the bias current, as a result of which an offset-free low frequency amplification is achieved. The high frequency signals are processed by a separate amplifier.

JP 12-79428 describes an optical read/write apparatus in which signals from photodetectors are separated into high frequency components and low frequency components and are subsequently amplified by operational amplifiers. The amplified low frequency signal is recombined with the high frequency signal.

US 4,785,44 describes means for achieving a reliable tracking in an optical read/write apparatus. In this apparatus the high frequency components are also processed separately from the low frequency components.

Consequently, there is a need for optical read/write apparatuses having a

signal processing unit in which high frequency components and low frequency components are separated from one another directly after the output of the detector and are processed separately.

In order cater for this, according to the invention, the apparatus of the type defined in the opening paragraph is characterized in that the means M_{III} for processing the high frequency components include a bias current source and a second current mirror, an input branch of the second current mirror and a current output terminal of the bias current source both being connected to the second input terminal of the means M_{III}. The bias current source enables the second current mirror of the means M_{III} to be biased to a value at which a satisfactory bandwidth can be obtained without the operation of the means M_{II} being affected thereby.

The means M_{II} are usually implemented as a self-biased amplifier, the current supplied by the detector also serving as bias current. This may lead to the input impedance of the means M_{II} being dependent on the intensity of the current supplied by the detector. This affects the operation of the means M_I, which in its turn may result in crosstalk from the low frequency components to the high frequency components. It is the object of the apparatus defined in Claim 2 to preclude this. The effect of the operational amplifier is that the means M_{II} have such a low input impedance that they do not have any significant influence on the operation of the means M_I.

Claim 3 defines another embodiment which precludes crosstalk. In this case, the means M_{II} have a comparatively high input impedance. However, since the input impedance is now substantially signal independent allowance can be made for this in the choice of the means M_I and, if desired, the input impedance can form part of the means M_I.

The means M_I for separating high frequency components and low frequency components of the detected signal give rise to a zero point in the signal transmission from the detector to the means M_{III} for processing the high frequency components. The presence of the zero point is not of any significance for the transmission of the signal because the low frequency components do not contain any data information. However, the zero point does have an adverse effect on the flatness of the group delay response of the information signal. The object of the embodiment defined in Claim 4 is to mitigate this adverse effect. In this embodiment the low frequency component of the signal which reaches the input of the means M_{III} is reconstructed, so that the zero point is compensated by means of a pole. The reconstruction provides a flatter group-delay response of the information signal.

Claim 5 defines a practical variant of said embodiment. This variant ensures in a simple manner that the current supplied by the means IV has the correct phase for reconstructing the signal on the input of the means M_{II}.

On the one hand, a satisfactory gain matching of the low frequency components is of importance for an accurate pole/zero-point cancellation and, consequently, a flat group-delay response. On the other hand, a large bandwidth is important and the gain matching is less relevant for the high frequency components. The embodiment defined in Claim 6 provides a very accurate gain matching of the of the low frequency components and a large bandwidth for the high frequency components.

The above as well as other aspects of the invention will be described in more detail with reference to the drawings. In the drawings:

Figure 1 shows a block diagram of an optical read/write apparatus in accordance with the invention;

Figure 2 shows a block diagram of the means M_I for separating high frequency components and low frequency components of the detected signal, the means M_{II} for processing the low frequency components and the means M_{III} for processing the high frequency components,

Figure 3 shows in more detail the means M_I, M_{II} and M_{III} and shows diagrammatically means M_{IV} for coupling the means M_{II} to the means M_{III} of a first embodiment,

Figure 4 shows in more detail the means M_{IV} in the first embodiment,

Figure 5 shows in more detail the means M_{III} of a second embodiment,

Figure 6 shows in more detail the means M_I and M_{II} of a third embodiment.

Figure 1 shows diagrammatically an optical read/write apparatus for reading from and/or writing onto an optical data carrier 1. In the present case, the optical data carrier 1 is a writable optical data carrier of a customary type, for example as described in EP-A 0 265 984. The optical data carrier 1 has a transparent substrate 2 provided with a structure of tracks which are substantially concentric with one another. The tracks exhibit a radial wobble whose frequency is modulated in accordance with a DC free digital address

signal. The substrate 2 carries a layer provided with an optical pattern. The layer 3 is, for example, a radiation-sensitive dye layer or a so-called phase-change layer. The data carrier 1 is given a rotary motion about an axis 4 by customary means.

The optical read/write apparatus comprises an optical read/write head 5 for writing information patterns into or reading such patterns from a track. The head has a radiation source 6 for generating a radiation beam. The radiation source 6 is, for example, a solid-state laser. The optical read/write head further has an optical system for routing the radiation beam to a radiation-sensitive detector 10 via the data carrier 1. The detector 10 has an output 10_A for supplying a detected signal, which is a measure of radiation detected by means of the detector. In the present case, the optical system comprises a lens 7, a focusing objective 8 and a beam splitter 9. The radiation beam generated by means of the radiation source 6 is focussed onto the layer 3 of the optical data carrier 1 by means of the lens 7 and the focussing objective 8. The radiation beam reflected from the layer 3 is reflected to the detector 10 via the beam splitter 9, for example a semi-transparent mirror. Furthermore, in the present case, an astigmatic element 11 for detecting a focus error is interposed between the beam splitter 9 and the detector 10.

The output 10_A of the detector 10 is coupled to a common input terminal 0 of a signal processing unit 12 to receive the detected signal I_{IN}, the signal processing unit including means M_I for separating high frequency components and low frequency components of the detected signal I_{IN}, means M_{II} for processing the low frequency components, and means M_{III} for processing the high frequency components.

The signal processing unit 12 further including means 16 for deriving an information signal on the basis of the high frequency components. The information signal is a representation of the information stored on the data carrier. The means 16 comprise, for example, a demodulator, a time-base corrector, an error corrector, and a D/A converter.

The signal processing unit 12 further includes means 13 for deriving control signals FE (focus error signal) and RE (radial push-pull signal) on the basis of the low frequency components. The focus error signal FE is received by an input of a control circuit 14 which minimizes the focus error in a manner known per se. The radial push-pull signal RE is frequency-modulated owing to the frequency-modulated track wobble. An FM demodulator derives an address signal from the signal RE. Various methods of deriving these control signals are known, which methods are based on the division of a photo-detector into sections, for example, four quadrants or, for example, four sections disposed in line. In practice, this means that a proportional number of the means M_I and M_{II} can be used.

However, herein these means are shown for only one detector for the sake of simplicity. Preferably, the means M_I and M_{II} for the other detectors are identical thereto.

The means M_I and M_{II} and M_{III} are shown in greater detail in Figure 2.

The means M_I for separating the high frequency components and the low frequency components of the detected signal comprise a capacitive element 18.

The means M_{II} for processing the low frequency components include a current mirror having a first input terminal 24 and a first output terminal 28. The first input terminal 24 is coupled to the common input terminal 0.

The means M_{III} for processing the high frequency components have a second input terminal 40 coupled to the common input terminal 0 via the capacitive element 18. The means M_{III} for processing the high frequency components include a bias current source 60 and a second current mirror. An input branch 41 of the second current mirror and an output terminal 62 of the bias current source 60 are both connected to the second input terminal 40 of the means M_{III}.

Figure 3 shows the means M_I, M_{II} and M_{III} of a first embodiment of the optical read/write apparatus in accordance with the invention in greater detail. In the present case, the self-biased current mirror of the means M_{II} comprises a first semiconductor element 20 and a second semiconductor element 22. The first semiconductor element 20 and the second semiconductor element 22 each have a control electrode and a first and a second control electrode, a main current path being interposed between the first and the second main electrode. It is to be noted that semiconductor elements in this Figure and the following Figures are bipolar transistors whose bases, collectors and emitters constitute the control electrode, the first main electrode and the second main electrode, respectively. However, alternatively the semiconductor elements can be unipolar transistors whose gate, drain and source constitute the control electrode, the first main electrode and the second main electrode, respectively.

The current mirror 20, 22 has a first input branch for transferring an input current (I_{LF}). The first input branch connects the first input terminal 24 to a first central terminal 26 via the main current path of the first semiconductor element 20. The control electrode and the first main electrode of the first semiconductor element 20 are interconnected. The current mirror further has a first output branch for transferring an output current (I'_{LF}). The first output branch connects the first central terminal 26 to the first output terminal 28 via the main current path of the second semiconductor element 22. The control electrode of the second semiconductor element 22 is connected to the control electrode of the

first semiconductor element 20. Figure 3 also shows, in broken lines, the parasitic capacitive impedance 10_B of the detector 10 between the first input terminal 24 and the first central terminal 26.

The first semiconductor element 20 of the current mirror of the means M_{II} is connected to the first central terminal 26 via a first resistive element 30. The presence of the first resistive element 30 in the first input branch of the current mirror of the means M_{II} ensures that the means M_{II} have a relatively signal-independent input impedance. This counteracts crosstalk of the low frequency components to the high frequency components. In addition to the capacitive element 18, the means M_I include the parasitic capacitance 10_B of the detector 10. The means M_I further comprise the resistive element 30, which in the present case also forms part of the means M_{II}. Since, in the present case, the resistive element is used both in the means M_I and in the means M_{II} separate resistive elements for the means M_I and M_{II} are not necessary. This reduces the dissipation. In the present case, the means M_I produce a pole in the transfer function I_{LF}/I_{IN} at a frequency f of $2\pi/R(C_P+C_{AC})$, where R is the resistive value of the first resistive element 30 and C_P and C_{AC} are the capacitive values of the parasitic capacitance 10_B and the capacitive element 18, respectively. The transfer function for the signal from the detector 10 to the means M_{III} has a zero point for the same frequency f. The high frequency central terminal are transferred to the second input terminal 40 of the means M_{III} with an attenuation factor $\propto = C_{AC}/(C_P+C_{AC})$.

For reasons of symmetry the second semiconductor element 22 of the current mirror is connected to the central terminal 26 via a second resistive element 31.

Since the means M_{II} need only handle low frequency components of the detected signal the first and the second semiconductor element 20, 22 can be comparatively large in the case of implementation as an IC, as a result of which a satisfactory gain matching and a satisfactory DC transmission are achieved.

In the embodiment shown in Figure 3 the current mirror of the means M_{II} has a further output terminal 32 for supplying a further output current (I''_{LF}). The signal processing unit 12 further includes means M_{IV} for coupling the means M_{II} to the means M_{IV}. The means M_{IV} have a third output terminal 70 for receiving the further output current ((I''_{LF}). The means M_{IV} further have a third output terminal 72 for supplying a related current $\propto I''_{LF}$ to the second input terminal 40 of the means M_{III}.

The further output terminal 32 is connected to the first central terminal 26 via a further output branch. The further output branch is formed by a main current path of a

further semiconductor element 36 and by a further resistive element 38 arranged between said main current path and the first central terminal 26. A control electrode of the further semiconductor element 36 is connected to the control electrodes of the first semiconductor element 20 and the second semiconductor element 22.

The means M_{IV} supply a current $\propto I"_{LF}$ which is proportional to the low frequency component I_{LF} of the detected signal. The proportionality factor $\propto$ is chosen to be equal to the afore-mentioned attenuation factor. Thus, except for the proportionality factor $\propto$, the detected signal I_{IN} is reconstructed on the second input terminal 40 of the means M_{III}.

The second current mirror of the means M_{III} includes a third semiconductor element 42 and a fourth semiconductor element 44, each having a first and a second main electrode, which define a main current path, and a control electrode. The control electrode of the third semiconductor element 42 and the control electrode of the fourth semiconductor element 44 are connected to one another. The second current mirror has a second input branch 41 for transferring an input current ($I_{INIII} + I_{DCHF}$). The second input branch 41 connects the second input terminal 40 to a second central terminal 46 via the main current path of the third semiconductor element 42. The second current mirror further has a second output branch for transferring an output current (I_{OUT}). The second output branch connects the second central terminal 46 to second output terminal 47 via the main current path of the fourth semiconductor element 44.

In the present embodiment the third semiconductor element 42 is connected to the second central terminal 46 via a parallel arrangement of a third resistive element 48 and a second capacitive element 50. The fourth semiconductor element 44 is connected to the second central terminal 446 via a parallel arrangement of a fourth resistive element 52 and a third capacitive element 54. The third resistive element 48 and the fourth resistive element 52 provide accurate gain matching for low frequencies. The second capacitive element 50 and the third capacitive element 54 constitute a short-circuit for high frequencies, as a result of which the means M_{III} yet have a large bandwidth.

In the present embodiment the means M_{III} also include an operational amplifier 56 and a bias voltage source 58. The operational amplifier 56 has an inverting first input connected to the input 40 of the means M_{III}. The operational amplifier 56 has a non-inverting second input connected to a voltage output terminal 59 of the bias voltage source 58. The voltage output terminal 59 of the bias voltage source 58 is also connected to the control electrodes of the third semiconductor element 42 and the fourth semiconductor

element 44. The operational amplifier 56 has an output connected to the second central terminal 46. The operational amplifier 56 constitutes a virtual short-circuit between the control electrode and the first main electrode of the third semiconductor element 42, as a result of which this semiconductor element operates as an input branch 41 having a very low input impedance.

Figure 4 shows the means M_{IV} used in the embodiment of Figure 3 in greater detail. In the present case, the means M_{IV} are constructed as a third current mirror. The third current mirror has a third input branch for transferring an input current. The third input branch has a fifth semiconductor element 74 which connects the third input terminal 70 to a third central terminal 78 via its main current path. The third current mirror has a third output branch for transferring an output current. The third output branch has a sixth semiconductor element 76 which connects the third central terminal 78 to the third output terminal 72 via its main current path.

In the present case, a fifth resistive element 80 having a resistive impedance R1 is arranged between the main current path of the fifth semiconductor element 74 and the third central terminal 78 and a sixth resistive element 82 having a resistive impedance R2 is arranged between the main current path of the sixth semiconductor element 76 and the third central terminal 78. Thus, it is achieved that the output current is equal to the input current multiplied by a factor R1/R2. Alternatively, this factor can be realized by the choice of the resistive elements 30 and 38 in the current mirror of the means M_{II}. In that case, the main current path of the fifth semiconductor element 74 and the sixth semiconductor element 76 can be coupled directly to the third terminal 78.

Figure 5 shows an alternative version of the means M_{III}. Parts therein which correspond to those in Figure 3 have corresponding reference numerals increased by 100. In Figure 5 the non-inverting input of the operational amplifier 156 is connected to the second input terminal 140 of the means M_{III}. The inverting input of the operational amplifier 156 is connected to the voltage output terminal 159 of the bias voltage source 158. The output of the operational amplifier 156 is connected to the control electrodes of the semiconductor elements 142 and 144.

The use of an operational amplifier in the means M_{III}, as shown in Figure 3 and Figure 5, enables a comparatively large bandwidth to be obtained for the means M_{III}. For simple uses in which the high frequency components have only a comparatively small bandwidth a version of the means M_{III} is conceivable which does not employ an operational amplifier. In that case the control electrode of the third semiconductor element is connected

to the input of the means M_{III}.

Figure 6 shows an alternative version of the means M_I and M_{II}. Parts therein which correspond to those in Figure 3 have corresponding reference numerals increased by 200. In Figure 6 the means M_{II} also include an operational amplifier 235 and a bias voltage source 233. One of the inputs of the operational amplifier 235, in this case the inverting input, is connected to the first main electrode of the first semiconductor element 220. The non-inverting other input of the operational amplifier 235 is connected to a voltage output terminal 234 of the bias voltage source 233. The output of the operational amplifier 235 is coupled to one of the other electrodes, in this case the second main electrode, of the first semiconductor element 220.

The present means M_I include the capacitive element 218 and a resistive element 219. In the present case, the resistive element 219 is arranged between the common input terminal 200 and the first input terminal 224 of the means M_{II}.

In a variant of the means M_{II}, in a manner similarly to that shown in Figure 5, the voltage output terminal 234 of the bias voltage source 233 is connected to the inverting input of the operational amplifier 235 and the first main electrode of the first semiconductor element 220 is connected to the non-inverting input. The control electrodes of the semiconductor elements 220, 222 and 236 in this variant are connected to the output of the operational amplifier.

CLAIMS:



1. An optical read/write apparatus for reading from and/or writing onto an optical data carrier (1), which apparatus comprises

- a radiation source (6) for generating a radiation beam,
- an optical system (7, 8, 9, 11) for routing the radiation beam to a radiation-sensitive detector (10) via the data carrier (1), which detector has an output terminal (10_A) for supplying a detected signal (I_{IN}),
- a signal processing unit (12) having a common input terminal (0) coupled to the output terminal (10_A) of the detector (10) to receive the detected signal (I_{IN}), the signal processing unit (12) comprising:
- means M_I for separating high frequency components and low frequency components from the detected signal (I_{IN}), comprising a capacitive element (18);
- means M_{II} for processing the low frequency components, which means M_{II} include a current mirror (20, 22) having a first input terminal (24) and having a first output terminal (28), the first input terminal (24) being coupled to the common input terminal (0);
- means M_{III} for processing the high frequency components, which means M_{III} have a second input terminal (40) and a second output terminal (47), which second input terminal (40) is coupled to the common input terminal (0) via the capacitive element (18);

characterized in that the means M_{III} for processing the high frequency components include a bias current source (60) and a second current mirror (42, 44), an input branch (41) of the second current mirror and a current output terminal (62) of the bias current source (60) both being connected to the second input terminal of the means M_{III}.

2. An apparatus as claimed in Claim 1, characterized in that the current mirror (220, 222) of the means M_{II} include an operational amplifier (235), a bias voltage source (233), and a first and a second semiconductor element (220 and 222, respectively), which operational amplifier (235) has an inverting input, a non-inverting input and an output,

which semiconductor elements (220, 222) each comprise main electrodes, which define a main current path, and a control electrode, the control electrode of the first semiconductor element (220) and the control electrode of the second semiconductor element (222) being connected to one another, the current mirror of the means M_{II} comprising a first input branch for transferring an input current, which first input branch connects the first input terminal (224) to a first central terminal (226) via the main current path of the first semiconductor element (220), the first main electrode of the first semiconductor element (220) being connected to the first input terminal (224), which current mirror further comprises a first output branch for transferring an output current, which first output branch connects the first central terminal (226) to the first output terminal (228) via the main current path of the second semiconductor element (222), the operational amplifier (235) having one of its inputs connected to a voltage output terminal (234) of the bias voltage source (233), the operational amplifier (235) having its other input connected to the first main electrode of the first semiconductor element (220), and the operational amplifier having its output coupled to one of the other electrodes of the first semiconductor element (220).

3. An apparatus as claimed in Claim 1, characterized in that the current mirror of the means M_{II} comprises a first and a second semiconductor element (20 and 22, respectively), which semiconductor elements each comprise main electrodes, which define a main current path, and a control electrode, the control electrode of the first semiconductor element (20) and the control electrode of the second semiconductor element (22) being connected to one another, which current mirror comprises a first input branch for transferring an input current, which first input branch connects the first input terminal (24) to a first central terminal (26) via the main current path of the first semiconductor element (20), which current mirror further comprises a first output branch for transferring an output current, which first output branch connects the first central terminal (26) to the first output terminal (28) via the main current path of the second semiconductor element (22), the first semiconductor element (20) and the second semiconductor element (22) being connected to the first central terminal (26) via a first resistive element (30) and a second resistive element (31), respectively.

4. An apparatus as claimed in Claim 1, 2 or 3, characterized in that the current mirror of the means M_{II} has a further output terminal (32) for supplying a further output current (I''_{LF}) and the signal processing unit (12) further comprises means M_{IV} for

coupling the means M_{II} to the means M_{III}, which means M_{IV} comprise a third input terminal (70) for receiving the further output current ($I"_{LF}$) and a third output terminal for supplying to the second input terminal (40) of the means M_{III} a current ($\propto I"_{LF}$) which is related to said further output current.

5. An apparatus as claimed in Claim 4, characterized in that the means M_{IV} take the form of a third current mirror, which has a third input branch for transferring an input current, which third input branch has a fifth semiconductor element (74) which connects the third input terminal (70) of the means M_{IV} to a third central terminal (78) via its main current path, which third output branch has a sixth semiconductor element (76) which connects the third central terminal (78) to the third output terminal (72) via its main current path.

6. An apparatus as claimed in Claim 4 or 5, characterized in that the second current mirror of the means M_{III} comprises a third semiconductor element (42) and a fourth semiconductor element (44), which semiconductor elements each comprise main electrodes, which define a main current path, and a control electrode, the control electrode of the third semiconductor element (42) and the control electrode of the fourth semiconductor element (44) being connected to one another, which second current mirror comprises a second input branch (41) for transferring an input current, which second input branch (41) connects the second input terminal (40) to a second central terminal (46) via the main current path of the third semiconductor element (42), which second current mirror further comprises a second output branch for transferring an output current, which second output branch connects the second central terminal (46) to the second output terminal (47) via the main current path of the fourth semiconductor element (44), the third semiconductor element (42) of the second current mirror being connected to the second central terminal (46) via a parallel arrangement of a third resistive element (48) and a second capacitive element (50), and the fourth semiconductor element (44) being connected to the second central terminal (46) via a parallel arrangement of a fourth resistive element (52) and a third capacitive element (54).

7. A signal processing unit (12) having a common input terminal (0) for receiving a signal (I_{IN}), the signal processing unit (12) comprising:

- means M_I for separating high frequency components and low frequency components from the signal (I_{IN}), comprising a capacitive element (18);

- means M_{II} for processing the low frequency components, which means M_{II} include a current mirror (20, 22) having a first input terminal (24) and having a first output terminal (28), the first input terminal (24) being coupled to the common input terminal (0);
- means M_{III} for processing the high frequency components, which means M_{III} have a second input terminal (40) and a second output terminal (47), which second input terminal (40) is coupled to the common input terminal (0) via the capacitive element (18);

characterized in that the means M_{III} for processing the high frequency components include a bias current source (60) and a second current mirror (42, 44), an input branch (41) of the second current mirror and a current output terminal (62) of the bias current source (60) both being connected to the second input terminal (40) of the means M_{III}.

8. A signal processing unit as claimed in Claim 7, further characterized as defined in the characterizing part of as claimed in any one of the Claims 1 up to an including 6.