

# PATENT SPECIFICATION

(11) 1262876

## DRAWINGS ATTACHED

- (21) Application No. 36178/71 (22) Filed 14 Feb. 1969  
(62) Divided out of No. 1262875  
(31) Convention Application No. 705709 (32) Filed 15 Feb. 1968 in  
(33) United States of America (US)  
(45) Complete Specification published 9 Feb. 1972  
(51) International Classification H 03 d 3/26//H 03 f 3/04  
(52) Index at acceptance

H3A 1A4 3N 4G



## (54) ANGLE MODULATION SYSTEM

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware United States of America of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to angle modulation systems, and more particularly to angle modulation discriminators which are particularly useful for integrated circuit applications. The term angle modulation as used herein refers to frequency or phase modulated wave or waves modulated in both frequency and phase.

Integrated circuit technology has heretofore been applied to angle modulation detectors. One example of a frequency modulation detector system using integrated circuit techniques is described in an article published in the March 21, 1966 issue of *Electronics* at page 137, by Jack Avins. The system described in that article is currently being used commercially, and has been found to provide exceptionally high standards of performance in the field. In order to more fully capitalize on the advantages of the integrated circuit technology, it is desirable to reduce the cost of the components not incorporated on the integrated circuit chip and to utilize more fully the design constraints and advantages of integrated circuits as compared to lumped constant circuits to improve the operating performance.

It is an object of the present invention to provide a new and improved angle modulation signal system.

In accordance with the principles of the present invention, which is divided from our application No. 8109/69 (Serial No. 1262875), there is provided an angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network, said discriminator phase-shift network having first and

second outputs respectively providing first and second amplitude modulated signals referred to the same quiescent potential, said angle modulation amplifier-detector having first and second transistors connected as an emitter-coupled differential amplifier, a first semiconductive rectifier junction and a first capacitance being connected in a first series combination with their interconnection connected via a first DC path to the base electrode of said first transistor, and a second semiconductive rectifier junction and a second capacitance connected in a second series combination with their interconnection connected via second DC path to the base electrode of said second transistor, said first and said second series combinations being connected between respective one of said first and said second outputs of said discriminator phase-shift network and points of reference potential, said emitter-coupled differential amplifier constituting a signal output circuit for and providing a principal DC loading of first and second detectors respectively formed by said first and said second series combinations, and the output of said amplifier-detector being provided at at least one of the collector electrodes of said first and said second transistors in response to said first and said second amplitude-modulated signals.

An embodiment of the present invention has an angle modulation signal system having a discriminator network adapted to convert angle modulated signals to amplitude modulated signals. First and second transistors are provided operating from a source of operating potential and having their input electrodes coupled to the discriminator network. Third and fourth transistors operating from the source of operating potential are provided and are interconnected to form a differential amplifier having a first and a second input electrode. The first differential input electrode is connected to the first transistor output electrode to provide the only D.C. path between the first transistor output electrode and the

first differential input electrode. The second differential input electrode is connected to the second transistor output electrode to provide the only D.C. path between the second transistor output electrode and the second differential input electrode. The differential amplifier is adapted to be connected to signal utilization means.

In the accompanying drawings:

FIGURE 1 is a schematic circuit diagram of an angle modulation detector system embodying the present invention;

FIGURE 2 is a graphical representation of the output signals as a function of frequency of the discriminator portion of the angle modulation detector system;

FIGURE 3 is a graphical representation of the resultant wave form obtained by subtracting the values of the two rectified discriminator output signals over the linear range as a function of frequency;

FIGURE 4 is a schematic circuit diagram of an alternate discriminator network with center tap drive to the tuned circuit; and

FIGURE 5 is a schematic circuit diagram of a modification of the amplifier-detector portion of the angle modulation detector system.

Referring now to the drawings and more particularly to FIGURE 1, the dashed rectangle 10 of FIGURE 1 schematically illustrates a monolithic semiconductor chip. The chip has a plurality of contact areas about its periphery, through which external connections to the circuits on the chip can be made. For example, the contact 12 provides a common or ground potential contact area, which is connected to the various circuit-ground connections on the chip. The circuit includes a limiter 100, a discriminator 200, a portion of which is external to the chip, and a differential amplifier-detector 300.

A frequency modulated carrier wave developed across the tuned circuit 16 is applied to the input terminals 14 and 14' of the limiter 100. The signal is translated through three amplifier-limiter stages 18, 20 and 22 and is developed across an output load resistor 24. The signal developed across resistor 24 is applied to the discriminator 200, which develops two antiphase voltages that drive the detector 300.

The limiter stage 18 includes three transistors 26, 28 and 38. The emitter electrodes of transistors 26 and 28 are directly connected, the junction being connected to ground by a resistor 30. A load resistor 32 is connected between the collector electrode of the transistor 28 and a junction point 34. A source of positive regulated potential is developed at the junction point 34, described more fully hereinafter.

The collector electrode of the transistor 26 is directly connected to the junction point 34 and the base electrode of the transistor

28 is connected to ground by a radio-frequency (RF) bypass capacitor 36. The base electrode of the transistor 26 is connected to the capacitor 36 through the tuned input circuit 16 connected across the terminal 14 and 14'.

The transistor 38 in an emitter follower configuration is coupled to receive signals developed across the resistor 32. The transistor 38 has its emitter electrode connected to the ground by a resistor 40. The collector electrode of the transistor 38 is directly connected to a source of positive potential applied to the chip through the contact terminal 42.

The output signal taken at the emitter electrode of the transistor 38, is applied to the second limiter stage 20, which includes the transistors 44, 46 and 60. The emitter electrodes of the transistors 44 and 46 are directly connected, and their junction is connected to the ground by a resistor 48. The collector electrode of the transistor 46 is connected to the junction point 34 by a load resistor 50, and the collector electrode of the transistor 44 is directly connected to the junction point 34. A diode 52, a resistor 54, a resistor 56 and a diode 58 are connected in series between the junction point 34 and ground to provide a suitable bias at the junction of the two resistors for the base electrode of the transistor 46.

The transistor 60 is connected as an emitter follower, and signals developed across the emitter output resistor 62 are applied to the third limiter stage 22 through a resistor 66. The collector electrode of the transistor 60 is directly connected to the source of positive potential 42. A resistor 68 interconnects the emitter electrode of the transistor 60 and the RF bypass capacitor 36. This connection provides a negative feedback loop to stabilize the limiter circuit by providing the necessary operating bias for the base electrodes of the transistors 26, 28 and 70.

The final limiter stage 22 includes the transistors 64 and 70. The emitter electrodes of the transistors 64 and 70 are directly connected, and their junction is connected to ground through the emitter-collector current path of a transistor 72 which provides a constant source of current. The base electrode of the transistor 72 is connected to the junction point of the resistor 56 and the diode 58. A load resistor 24 interconnects the collector electrode of the transistor 70 to the junction point 34, and a direct connection is provided between the collector electrode of the transistor 64 and the junction point 34. The base electrode of the transistor 70 is directly connected to the RF bypass capacitor 36.

The base current of the transistor 64 flows through resistor 66 while the base currents of the transistors 26, 28 and 70 flow through the resistor 68. Therefore, to achieve substantially equal bias potential on the base elec-

trodes of the transistors 64 and 70, the resistor 66 should be three times as large as the resistor 68, assuming that all the transistors draw the same base current.

- 5 That is, the resistors 66 and 68 should be apportioned so that the voltage drops from the emitter electrode of the transistor 60 across the respective resistors are equal. It should be noted that the importance of the  
10 ratio is advantageous in integrated circuit fabrication techniques where it is difficult to regulate the absolute value of components, but comparatively easy to regulate their relative values. Where equal transistor base cur-  
15 rents are not used, the required ratio of the resistor 66 to the resistor 68 is readily determined.

- The biasing arrangement of the limiter circuit is accomplished utilizing only a single  
20 RF bypass capacitor 36 in the feedback network. This reduces the number of external components to be used with the integrated circuit chip and thus reduces the number of connections to be made to the chip.

- 25 Referring now to the regulated voltage supply at the junction point 34, a positive source of potential is applied to the contact area 42. A transistor 74 has its collector electrode directly connected to the terminal 42  
30 and, hence, the positive source of potential. The emitter electrode of the transistor 74 is directly connected to the base electrode of a transistor 76. The base electrode of the transistor 74 is connected to the junction point  
35 of two zener diodes 78 and 80 which are connected in series between the terminal 42 and the ground. The collector and emitter electrodes of the transistor 76 are connected between the terminal 42 and the junction point  
40 34. The specific form of voltage regulation is a matter of choice and is not critical to the operation of the circuit.

- Discriminator 200 utilizes a single parallel  
45 tuned circuit rather than the two tuned circuits typical of the prior art. Because one tuned circuit is used, there is a substantial cost saving in the discriminator network and in labor because the single tuned circuit phase-shift discriminator is more easily aligned  
50 than the prior art two tuned circuit systems.

- The discriminator 200 includes a tuned circuit 202 comprising an inductor 204 and a capacitor 206 which are not part of the  
55 integrated circuit chip but are connected electrically to the chip by the contact areas 206 and 208. A resistor 210 and a capacitor 212 are connected in series between terminal 206 and ground, the junction of the resistor and the capacitor being directly connected to the collector electrode of the transistor 70. Two  
60 capacitors 214 and 216 are connected across each side of the tuned circuit and ground. That is, capacitor 214 is connected between the terminal 206 and ground, and the capa-

citor 216 is connected between the terminal 208 and ground.

In operation, the rectangular voltage wave shape which would otherwise appear across the load resistor 24 at the last limiter stage 22 is altered by the integrating capacitor 212  
70 to develop a partially integrated or triangular wave form at the junction of the resistor 210 and the capacitor 212. This integrated wave form is further integrated by the capacitor 214 so that harmonic components at the two  
75 input terminals to the differential amplifier-detector 300 are substantially reduced.

Output signals are derived from the discriminator 200 across the capacitor 214 (or the capacitors 206 and 216 in series) and the capacitor 216. The output signals provide  
80 balanced drive voltages to the amplifier-detector network 300 and are 180° apart in phase rather than at an asymmetrical angle as in prior art quadrature systems. Anti-phase operation of the discriminator network enhances the amplitude modulation rejection of the  
85 amplifier-detector because there is a reduction in the period during which both rectifier transistors of the amplifier-detector conduct simultaneously.

Moreover, the discriminator network is so arranged that it provides a common DC path from the output of the limiter through the discriminator network to the input of each  
95 detector circuit. Thus, a DC path is provided from the collector electrode of the transistor 70 through the resistor 210 to the base electrode of the rectifier transistor 306 and, in a like manner, a DC path is provided from the  
100 collector electrode of the transistor 70 through the resistor 210 and the inductor 204 to the base electrode of the rectifier transistor 310.

This DC path which links both amplifier-detector inputs and the last limiter stage 22  
105 permits the detector transistors of the amplifier-detector 300 to be equally biased to give balanced operation without the need for adjusting separate bias circuits. Moreover, since the two input terminals to the amplifier-detector 300 are interconnected by the inductor  
110 304, the same AM components are applied on both sides of the detector, the advantage of which will be more fully explained hereinafter.

The principal frequencies of the phase-shift discriminator 200 are  $\omega_0$ ,  $\omega_L$ , and  $\omega_H$  and are as shown in FIGURE 2 which is a plot of the  
120 output signals as a function of frequency of the discriminator portion of the anegle modulation detector system. The push-pull drive signals are taken across either end of the parallel tuned circuit 202 and are designated, for convenience,  $e_1$  and  $e_2$ .  $e_1$  is the discriminator  
125 output signal derived across the capacitor 214, and  $e_2$  is the output signal derived across the capacitor 216.

At the discriminator center frequency  $\omega_0$ , these voltages are equal in magnitude and

opposite in phase. On either side of the center frequency, over a specified range, the amplitude of one signal increases, while the amplitude of the other signal decreases, the phase remaining substantially 180° apart.

The principal frequencies can be determined as follows. From FIGURE 1, it is clear that  $e_2$  will be a minimum at the resonant frequency of  $L_{204}C_{206}$  where the tuned circuit displays its greatest impedance. That is, when

$$\omega^2 = \omega_H^2 = \frac{1}{L_{204}C_{206}}$$

In a like manner,  $e_1$  will be a minimum when the equivalent inductive susceptance of  $L_{204}C_{206}$  is equal to the capacitive susceptance of  $C_{216}$ . Thus:

$$-j\omega_L C_{216} = j\omega_L C_{206} + \frac{1}{j\omega_L L_{204}}$$

from which

$$\omega_L^2 = \frac{1}{L_{204}(C_{206} + C_{216})}$$

the cross-over frequency  $\omega_0$  of the phase-shift discriminator 200 will occur when the inductive susceptance of  $L_{204}C_{206}$  is half of the capacitive susceptance of  $C_{216}$ .

Thus:

$$-j\omega_0 C_{216} = 2(j\omega_0 C_{206} + \frac{1}{j\omega_0 L_{204}})$$

from which

$$\omega_0^2 = \frac{1}{L_{204}(C_{206} + \frac{C_{216}}{2})}$$

the principal frequencies are indicated on the wave forms shown in FIGURE which are the voltages  $e_1$  and  $e_2$  across  $C_{214}$  and  $C_{216}$  respectively as a function of frequency. The resonant frequency of the composite  $\pi$  network including  $C_{214}$ ,  $L_{204}C_{206}$  and  $C_{216}$  is given by

$$\omega_r^2 = \frac{1}{L_{204}(C_{206} + \frac{C_{214}C_{216}}{C_{214} + C_{216}})}$$

In the special case where  $C_{214} = C_{216}$

$$\omega_r^2 = \omega_0^2 = \frac{1}{L_{204}(C_{206} + \frac{C_{216}}{2})}$$

so that the resonant frequency of the composite  $\pi$  section is equal to the center frequency of the discriminator circuit. Symmetry of the wave forms shown in FIGURE 2 is obtained by the selection of the capacitors 214, 216 and 212, in addition to the resistor 210. Equal values of capacitance for the capacitors 214 and 216 are not required because the value of the resistor 210 can be chosen to provide the desired symmetry in the discriminator output signals. It is desirable that the Q of the inductor 204 be maintained high in order to avoid departure from the 180° phase difference between  $e_1$  and  $e_2$ .

The linear region for  $e_1 - e_2$  as a function of frequency is the frequency range between the two peak values of  $e_1$  and  $e_2$  as shown in FIGURE 2. Beyond this range,  $e_1 - e_2$  no longer varies linearly as a function of frequency. FIGURE 3, in a different scale, shows the resultant wave form obtained by subtracting the value of the two discriminator output signals over the linear range as a function of frequency. From the equations for  $\omega_L$  and  $\omega_H$ , it can be seen that the frequency range between  $\omega_L$  and  $\omega_H$  increases as the ratio of  $C_{216}$  divided by  $C_{206}$  is increased.

The drive for the discriminator 200 is taken from the collector electrode of the transistor 70 of the limiter stage 22. In the inter-carrier sound channel of a television receiver, the drive would be a square wave of current at 4.5 MHz (according to United States standards). The filtering action of the network including capacitor 212 in association with the resistor 210 and capacitor 214 is effective in substantially attenuating harmonics of the 4.5 MHz fundamental so that the voltages  $e_1$  and  $e_2$  are essentially sinusoidal. This attenuation of harmonics improves the balance of the system in that the harmonics do not appear at the amplifier-detector network input terminals.

An advantage of the phase-shift discriminator 200 for application in TV and FM radio is that the capacitors 214 and 216 are of a magnitude which can be readily integrated on a monolithic silicon chip. For operation at substantially lower frequencies, however, these capacitors can be arranged external to the integrated circuit chip.

It should be noted that the tuned circuit 202 of the discriminator 200 is not susceptible to fabrication in integrated circuit form at the present time. However, the discriminator utilizes only one tuned circuit rather than the two tuned circuits typical of the prior art and thereby reduces the cost in number of peripheral components and connections which must be made to the chip.

An alternate phase-shift network for use with the differential amplifier-detector network 300 is shown in FIGURE 4. This phase-shift network has a quadrature relationship between the voltages rather than the previously described anti-phase operation of the discriminator network shown in FIGURE 1. The discriminator output signals are derived across the tuned circuit 202' which includes the inductor 204' and capacitor 206'. A center tap connection 218 on the inductor 204' is provided and is directly connected by a lead 220 to the collector electrode of the transistor 70 in the last limiter stage 22. A capacitor 214' interconnects the lead 220 and ground, and a capacitor 216' interconnects one end of the tuned circuit 202' and ground.

The general operation of the phase-shift network is similar to the discriminator shown in FIGURE 1 so far as the integration of the square wave of current across the capacitor 214'. The quadrature voltage is induced across the tuned circuit 202' at its resonant frequency. This resonant frequency of the tuned circuit 202' is the discriminator center frequency. The capacitor 216' is the circuit component which results in the development of the quadrature voltage.

It should be noted that the discriminator networks of FIGURE 1 and FIGURE 4 both utilize a single tuned circuit. However, the tuned circuit 202' of the phase-shift network shown in FIGURE 4 is resonant at the discriminator center frequency  $\omega$ . While the tuned circuit 202 of the phase-shift network shown in FIGURE 1 is resonant at the frequency  $\omega_H$  which is substantially removed from the discriminator center frequency. The center frequency  $\omega_0$  of tuned circuit 202 is at the frequency where the tuned circuit 202 appears to be an inductive reactance.

The anti-phase operation of the discriminator shown in FIGURE 1 gives greater AM rejection when used with the differential amplifier-detector network 300, which is described in greater detail hereinafter. This results from the fact that the anti-phase relationship results in maximum symmetry and a minimum overlap of the conduction periods of the transistors in the detector circuit. This is especially important when AM is present and it is desired that the AM component does not produce a contribution to the current in the output of the detector.

Referring again to FIGURE 1, the output of the phase-shift discriminator 200 taken across the capacitors 214 and 216 drives the amplifier-detector 300. The amplifier-detector 300 includes two stages 302 and 304. Each of the stages 302 and 304 comprise a first transistor having its emitter electrode directly connected to the base electrode of a second transistor. Thus, a transistor 306, which has its base electrode connected to one side of the tuned circuit 202 through the contact area 206,

has its emitter electrode directly connected to the base electrode of a transistor 308.

In a like manner, a transistor 310, which has its base electrode connected to the other side of the tuned circuit 202 through the contact area 208, has its emitter electrode directly connected to the base electrode of a transistor 312.

The transistors 308 and 312 have their electrodes interconnected to form a differential amplifier. The emitter electrodes of the transistors 308 and 312 are connected to the collector electrode of a constant current transistor 318 by two resistors 314 and 316, respectively. The resistors 314 and 316 provide degeneration for the differential amplifier. The constant current source includes the transistor 318 and its biasing circuitry, the resistor 56 and the diode 58. The emitter electrode of the transistor 318 is directly connected to ground and the base electrode is connected to the anode of the diode 58.

A resistor 320 connects the collector electrode of the transistor 312 to the source of potential applied at the contact area 42. An output contact area 322 is connected to the collector electrode of the transistor 312. A bypass capacitor may be connected between the collector electrode of the transistor 312 and ground. The output terminal 322, in the present embodiment, is adapted to provide an output potential representative of the angular deviation, frequency or phase, of the wave applied to the input terminals 14 and 14' of the angle modulation detector system. The transistors 306, 308 and 310, as is the case with the transistor 312, are operated from the source of positive potential applied to the contact area 42. Thus, a direct connection is provided between the collector electrodes of the transistors 306, 308 and 310 of the contact area 42.

Since the two transistors 306 and 310 of the amplifier-detector stages 302 and 304 are directly connected to the base electrodes of the transistors 308 and 312, respectively, the input resistance of the transistors 308 and 312 provides substantially all the load resistance for the two transistors 306 and 310. Because the input impedance of the transistors 308 and 312 is very high, the transistors 306 and 310 are substantially biased to cutoff and, consequently, exhibit high sensitivity because there is substantially no threshold level which must be reached before detection occurs.

When the capacitance associated with the base to emitter junction of the transistors 308 and 312, which form the differential amplifier, is too small to give the desired time constant needed for demodulation, additional capacitance such as a capacitor 324 is connected between the emitter electrode of the transistor 306 and ground, and a capacitor 326 is connected between the emitter electrode of the transistor 310 and ground. By the addition of

the capacitors 324 and 326 the desired time constants can be achieved. These capacitors can be of a very small value owing to the high input resistance associated with the emitter follower transistors 306 and 310, and therefore, are susceptible of fabrication on an integrated circuit chip.

In operation, the constant current source transistor 318 determines the total collector currents which flow through the transistors 308 and 312 of the differential amplifier, this, in turn, determines the current flowing in the base electrodes of the transistors 308 and 312. Since there are no shunt paths between the emitter electrodes of the transistors 306 and 310 and ground, the emitter current flow in the rectifier transistors 306 and 310 is substantially the base current which is flowing in the transistors 308 and 312. In this manner, the rectifier transistors 306 and 310 are biased to cut off so that detection occurs at relatively low signal input levels.

The modulated RF signal input to the amplifier-detector stage 300 is a balanced input which is applied at the base electrodes of the rectifying transistors 306 and 310. The modulated RF signal input applied to the base electrodes of the rectifier transistors 306 and 310 varies oppositely in amplitude as a function of the angle modulated signal applied to the input terminals 14 and 14' and is rectified by the transistors before being applied as the input signal to the differential amplifier to produce the desired demodulated output at the contact area 322.

Improved amplitude modulation rejection capability for the amplifier-detector system is obtained because the configuration which includes the transistors 308 and 312 interconnected as a differential amplifier provides high common mode rejection capability. In addition, because of the high gain associated with the differential amplifier, only very low levels of RF input signals are required to obtain a high level of output signal. Low level RF input signal minimize the problems of RF radiation associated with conventional modulation signal detector schemes.

Reference is now made to FIGURE 5 which is a modification of the amplifier-detector portion of the angle modulation detector systems. The circuit of FIGURE 5 is similar to the amplifier-detector shown in FIGURE 1 except that a resistor and a capacitor have been added to the network interconnecting each rectifier transistor to the differential amplifier. The emitter electrode of the rectifier transistor 306' is connected to the base electrode of the transistor 308' by a resistor 326. A capacitor 328 interconnects the emitter electrode of the transistor 306' and the ground, and a capacitor 330 interconnects the base electrode of the transistor 308' and ground.

In a like manner, the resistor 332 interconnects the emitter electrode of the transis-

tor 310' and the base of the transistor 312'. A capacitor 334 connects the emitter electrode of the transistor 310' to ground, and a capacitor 336 connects the base electrode of the transistor 312' to ground. The resistors 326 and 332 may be of unequal value to improve amplitude modulation rejection. A similar effect can be achieved with a single resistor.

Utilization of two capacitors in the emitter circuit of the rectifier transistors, as in FIGURE 5, is particularly suited for low frequency applications where it may be advantageous to provide an additional filter section. In this way, the desired rectification and filtering is accomplished with a minimum total value of capacitance.

#### WHAT WE CLAIM IS:—

1. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network, said discriminator phase-shift network having first and second outputs respectively providing first and second amplitude modulated signals referred to the same quiescent potential, said angle modulation amplifier-detector having first and second transistors connected as an emitter-coupled differential amplifier, a first semiconductive rectifier junction and a first capacitance being connected in a first series combination with their interconnection connected via a first DC path to the base electrode of said first transistor, and a second semiconductive rectifier junction and a second capacitance connected in a second series combination with their interconnection connected via second DC path to the base electrode of said second transistor, said first and said second series combinations being connected between respective ones of said first and said second outputs of said discriminator phase-shift network and points of reference potential, said emitter-coupled differential amplifier constituting a signal output circuit for and providing principal DC loading of first and second detectors respectively formed by said first and said second series combinations, and the output of said amplifier-detector being provided at at least one of the collector electrodes of said first and said second transistors in response to said first and said second amplitude-modulated signals.

8. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in Claim 1 wherein said first and said second semiconductive junctions are the base-emitter junction of third and fourth transistors, respectively, both of said third and fourth transistors being connected in common-collector configurations.

3. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift net-

the capacitors 324 and 326 the desired time constants can be achieved. These capacitors can be of a very small value owing to the high input resistance associated with the emitter follower transistors 306 and 310, and therefore, are susceptible of fabrication on an integrated circuit chip.

In operation, the constant current source transistor 318 determines the total collector currents which flow through the transistors 308 and 312 of the differential amplifier, this, in turn, determines the current flowing in the base electrodes of the transistors 308 and 312. Since there are no shunt paths between the emitter electrodes of the transistors 306 and 310 and ground, the emitter current flow in the rectifier transistors 306 and 310 is substantially the base current which is flowing in the transistors 308 and 312. In this manner, the rectifier transistors 306 and 310 are biased to cut off so that detection occurs at relatively low signal input levels.

The modulated RF signal input to the amplifier-detector stage 300 is a balanced input which is applied at the base electrodes of the rectifying transistors 306 and 310. The modulated RF signal input applied to the base electrodes of the rectifier transistors 306 and 310 varies oppositely in amplitude as a function of the angle modulated signal applied to the input terminals 14 and 14' and is rectified by the transistors before being applied as the input signal to the differential amplifier to produce the desired demodulated output at the contact area 322.

Improved amplitude modulation rejection capability for the amplifier-detector system is obtained because the configuration which includes the transistors 308 and 312 interconnected as a differential amplifier provides high common mode rejection capability. In addition, because of the high gain associated with the differential amplifier, only very low levels of RF input signals are required to obtain a high level of output signal. Low level RF input signal minimize the problems of RF radiation associated with conventional modulation signal detector schemes.

Reference is now made to FIGURE 5 which is a modification of the amplifier-detector portion of the angle modulation detector systems. The circuit of FIGURE 5 is similar to the amplifier-detector shown in FIGURE 1 except that a resistor and a capacitor have been added to the network interconnecting each rectifier transistor to the differential amplifier. The emitter electrode of the rectifier transistor 306' is connected to the base electrode of the transistor 308' by a resistor 326. A capacitor 328 interconnects the emitter electrode of the transistor 306' and the ground, and a capacitor 330 interconnects the base electrode of the transistor 308' and ground.

In a like manner, the resistor 332 interconnects the emitter electrode of the transis-

tor 310' and the base of the transistor 312'. A capacitor 334 connects the emitter electrode of the transistor 310' to ground, and a capacitor 336 connects the base electrode of the transistor 312' to ground. The resistors 326 and 332 may be of unequal value to improve amplitude modulation rejection. A similar effect can be achieved with a single resistor.

Utilization of two capacitors in the emitter circuit of the rectifier transistors, as in FIGURE 5, is particularly suited for low frequency applications where it may be advantageous to provide an additional filter section. In this way, the desired rectification and filtering is accomplished with a minimum total value of capacitance.

#### WHAT WE CLAIM IS:—

1. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network, said discriminator phase-shift network having first and second outputs respectively providing first and second amplitude modulated signals referred to the same quiescent potential, said angle modulation amplifier-detector having first and second transistors connected as an emitter-coupled differential amplifier, a first semiconductive rectifier junction and a first capacitance being connected in a first series combination with their interconnection connected via a first DC path to the base electrode of said first transistor, and a second semiconductive rectifier junction and a second capacitance connected in a second series combination with their interconnection connected via second DC path to the base electrode of said second transistor, said first and said second series combinations being connected between respective ones of said first and said second outputs of said discriminator phase-shift network and points of reference potential, said emitter-coupled differential amplifier constituting a signal output circuit for and providing principal DC loading of first and second detectors respectively formed by said first and said second series combinations, and the output of said amplifier-detector being provided at at least one of the collector electrodes of said first and said second transistors in response to said first and said second amplitude-modulated signals.

8. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in Claim 1 wherein said first and said second semiconductive junctions are the base-emitter junction of third and fourth transistors, respectively, both of said third and fourth transistors being connected in common-collector configurations.

3. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift net-



work as claimed in Claim 1 or 2 wherein said first DC path is via a first resistor, said second DC path is via a second resistor, and third and fourth capacitances respectively connect the base electrodes of said first and said second transistors to points of reference potential.

4. An angle modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in any of the previous claims wherein said transistors, said semiconductor rectifier junctions and said capacitances are fabricated within the same monolithic integrated circuit.

5. An angle-modulated signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in any of the previous claims wherein said discriminator phase-shift network has an inductive winding and a first capacitor connected in parallel combination between its said first and said second outputs, a second capacitor coupling said second output of discriminator phase-shift network to a point of reference potential and means coupling a source of angle-modulated signals to said inductive winding.

6. An angle-modulated signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in Claim 5 wherein said inductive winding has a tap to which said means coupling a source of angle modulated waves is connected.

7. An angle-modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in Claim 6 wherein means coupling a source of angle-modulated waves includes a third capacitor connecting said tap to a point of reference potential and said source of angle-modulated waves has a source resistance.

8. An angle-modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in Claim 5 wherein said means coupling a source of angle-modulated waves to said inductive winding comprises a resistor connected to said first output of said discriminator phase-shift network.

9. An angle-modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in Claim 5 or 8 wherein a third capacitor couples said first output of said discriminator phase-shift network to a point of reference potential.

10. An angle-modulation signal amplifier-detector connected to a source of angle-modulated waves by a discriminator phase-shift network as claimed in any of Claims 5-9 wherein said inductive winding is the sole inductive winding in said discriminator phase-shift network.

11. FM detector circuit having a source of FM signals, a frequency-dependent phase-shift network including an inductor and a capacitor and being connected to said source of FM signals, first and second detector transistors having their base electrodes coupled to said frequency-dependent phase-shift network, third and fourth transistors connected to an emitter coupled differential amplifier configuration, said third and fourth transistors having signal voltages supplied from the emitter electrodes of said first and of said second detector transistors, respectively, detected FM signals being taken from the collector circuit of at least one of said third and said fourth transistors.

JOHN A. DOUGLAS,  
Chartered Patent Agent,  
50, Curzon Street,  
London, W1Y 8EU,  
Agent for the Applicant.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1972.  
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from  
which copies may be obtained.



\* C L M S \*