(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 May 2008 (29.05.2008)

PCT

(10) International Publication Number
WO 2008/063543 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2007/024034

(22) International Filing Date:
16 November 2007 (16.11.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/562,209 21 November 2006 (21.11.2006) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PAL, Rohit** [IN/US]; 5 Greenhill Drive #18C, Fishkill, NY 12524 (US). **PEIDOUS, Igor** [RU/US]; 732 Huntington Drive, Fishkill, NY 12524 (US). **BROWN, David** [US/US]; 40 Patricia Drive, Pleasant Valley, NY 12569 (US).

(74) Agent: **DRAKE, Paul, S.**; Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, Mail Stop 562, Austin, TX 78741 (US).

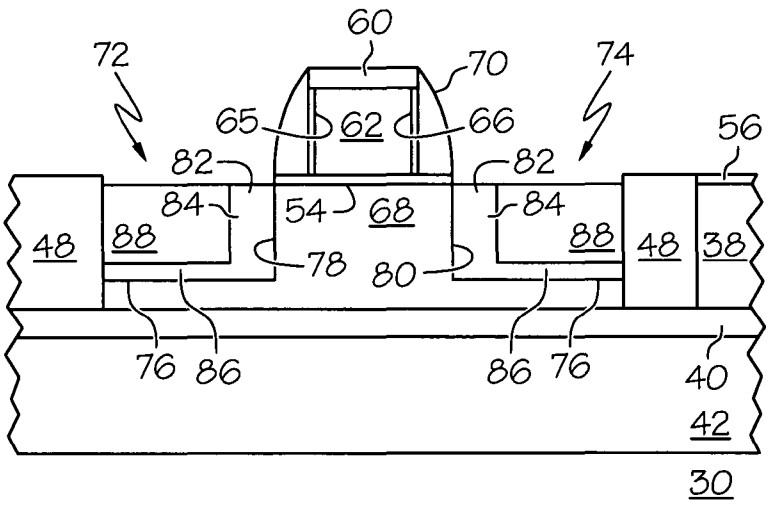
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

(54) **Title:** STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION



(57) **Abstract:** A stress enhanced MOS transistor [30] and methods for its fabrication are provided. In one embodiment the method comprises forming a gate electrode [62] overlying and defining a channel region [68] in a monocrystalline semiconductor substrate [38]. A trench [72, 74] having a side surface [78, 80] facing the channel region is etched into the monocrystalline semiconductor substrate adjacent the channel region. The trench is filled with a second monocrystalline semiconductor material [82, 90] having a first concentration of a substitutional atom and with a third monocrystalline semiconductor material [88, 100] having a second concentration of the substitutional atom. The second monocrystalline semiconductor material [82, 90] is epitaxially grown to have a wall thickness along the side surface sufficient to exert a greater stress on the channel region [68] than the stress that would be exerted by a monocrystalline semiconductor material having the second concentration if the trench was filled by the third monocrystalline material alone.

WO 2008/063543 A2