WHAT IS CLAIMED IS:

1. A packaged semiconductor chip (800) comprising:

a semiconductor substrate (810);

a radio-frequency input contact pad (812) implemented on the semiconductor substrate;

a radio-frequency output contact pad (813) implemented on the semiconductor substrate;

first (819) and second (816) direct-current, DC, contact pads implemented on the semiconductor substrate;

an input bias coupling path (873) implemented on the semiconductor substrate and electrically coupling the first DC contact pad to the second DC contact pad and the input contact pad;

one or more transistors (815) implemented on the semiconductor substrate and having an input coupled to the input contact pad;

a lead frame comprising:

one or more radio-frequency input pins (831) electrically coupled to the input contact pad;

one or more radio-frequency output pins (832) electrically coupled to the output contact pad; and

first (833) and second (837) input bias pins electrically coupled to the first and second DC contact pads, respectively; and

an output bias coupling path implemented on the semiconductor substrate and electrically coupling the output contact pad to a source of an output bias signal via at least one of the one or more radio-frequency output pins (832) of the lead frame, wherein the one or more transistors further have an output coupled to the output contact pad.

2. The packaged semiconductor chip (800) of claim 1, wherein the first (819) and second (816) DC contact pads are disposed on opposite sides of the input contact pad (812).

3. The packaged semiconductor chip (800) of claim 1, wherein:

the one or more transistors comprises a plurality of field-effect transistors; and

the input contact pad is electrically coupled to gates of the plurality of field-effect transistors.

4. The packaged semiconductor chip (800) of claim 1, wherein the input bias coupling path (873) is electrically coupled via an inter-package connection (747) to another input bias coupling path of another packaged semiconductor chip that is with the packaged semiconductor chip (800).

5. The packaged semiconductor chip (800) of claim 1, further comprising DC-blocking circuitry (871) implemented on the semiconductor substrate (810) and configured to block DC current between the input contact pad (812) and the inputs of the one or more transistors (815).

6. The packaged semiconductor chip (800) of claim 1, further comprising:

a first amplifier stage including the one or more transistors (815); and

a second amplifier stage (825) having an input coupled to an output of the first amplifier stage.

7. The packaged semiconductor chip (800) of claim 6, wherein the second amplifier stage is DC blocked from the first amplifier stage.

8. The packaged semiconductor chip (800) of claim 6, wherein the output bias coupling path electrically couples an output of the second amplifier stage with the output of the first amplifier stage.

9. The packaged semiconductor chip (800) of claim 6, wherein:

the second amplifier stage (825) comprises a plurality of transistors connected in parallel; and

inputs of the plurality of transistors are electrically coupled.

10. The packaged semiconductor chip (800) of claim 1, wherein the lead frame is a component of a flat no-leads package (830).

11. The packaged semiconductor chip (800) of claim 1, further comprising an output matching circuit (1360) disposed within the package (830, 1330).

12. The packaged semiconductor chip (800) of claim 11, wherein the output matching circuit (1360) is implemented on the semiconductor substrate (810, 1310).

13. A power amplifier (300, 700) comprising:

a printed circuit board (340, 740); and

a plurality of packaged semiconductor chips (351-364, 730, 731) mounted on the printed circuit board in a power amplifier configuration, each of the plurality of packaged semiconductor chips comprising:

a semiconductor substrate;

a radio-frequency input contact pad (812) implemented on the semiconductor substrate;

a radio-frequency output contact pad (813) implemented on the semiconductor substrate;

first (819) and second (816) direct-current (DC) contact pads implemented on the semiconductor substrate;

an input bias coupling path (873) implemented on the semiconductor substrate and electrically coupling the first DC contact pad to the second DC contact pad and the input contact pad;

one or more transistors (815) implemented on the semiconductor substrate and having an input coupled to the input contact pad;

a lead frame comprising one or more radio-frequency input pins electrically coupled to the input contact pad, one or more radio-frequency output pins electrically coupled to the output contact pad, and first and second input bias pins electrically coupled to the first and second DC contact pads, respectively;

a surface-mount packaging that at least partially houses the semiconductor substrate and the lead frame; and

an output bias coupling path implemented on the semiconductor substrate and electrically coupling the output contact pad to a source of an output bias signal via at least one of the one or more radio-frequency output pins of the lead frame, wherein the one or more transistors further have an output coupled to the output contact pad.

14. The power amplifier (300, 700) of claim 13, wherein the plurality of packaged semiconductor chips are identical.

15. The power amplifier (300, 700) of claim 13, wherein the plurality of packaged semiconductor chips comprises:

a first set of parallel packaged semiconductor chips; and

a second set of parallel packaged semiconductor chips;

wherein each of the first set of parallel packaged semiconductor chips is connected in series with at least one of the second set of parallel packaged semiconductor chips.

16. The power amplifier (300, 700) of claim 13, further comprising matching circuitry (1361) implemented on the printed circuit board (340, 740) configured to combine with parasitic elements of the plurality of packaged semiconductor chips to provide impedance matching for the plurality of packaged semiconductor chips for high-frequency operation.

17. The power amplifier (300, 700) of claim 16, wherein the high-frequency operation corresponds to the K_a frequency band.

18. A method of manufacturing a power amplifier, the method comprising:

providing a plurality of packaged semiconductor chips (351-364, 730, 731) each including respective internal bias coupling paths (873) electrically coupling a first direct-current (DC) contact pad (819), a second DC contact pad (816), and an input terminal (811) of respective packaged semiconductor chips and output bias coupling paths (875) implemented on a semiconductor substrate and electrically coupling a source of an output bias signal via an output terminal of respective packaged semiconductor ships, wherein each packaged semiconductor comprises one or more transistors having an output coupled to the output terminal;

providing a first circuit board (340, 740);

forming first electrical connections (342, 343) in the first circuit board for connecting to a first subset (351-364, 730, 731) of the plurality of packaged semiconductor chips; and

surface mounting the first subset of the plurality of packaged semiconductor chips on the first circuit board in a first multi-stage power amplifier configuration;

wherein the first electrical connections comprise parallel daisy-chain connections (747) between at least two of the first subset of the plurality of packaged semiconductor chips.

19. The method of claim 18, further comprising, after said surface mounting the first subset of the plurality of packaged semiconductor chips:

providing a second circuit board (340, 740);

forming second electrical connections (342, 343) in the second circuit board for connecting to a second subset (351-364, 730, 731) of the plurality of packaged semiconductor chips; and

surface mounting the second subset of the plurality of packaged semiconductor chips on the second circuit board in a second multi-stage power amplifier configuration, the second multi-stage power amplifier configuration having a greater number of amplifier stages than the first multi-stage power amplifier configuration;

wherein the second electrical connections comprise parallel daisy-chain connections (747) between at least two of the second subset of the plurality of packaged semiconductor chips and wherein the output bias coupling paths electrically couple the second subset of the plurality of packaged semiconductor chips to the first subset of the plurality of packaged semiconductor chips.

20. The method of claim 18, further comprising determining biasing values for the first subset of the plurality of packaged semiconductor chips based on parasitic elements of the first subset of the plurality of packaged semiconductor chips at a high operational frequency.

21. The method of claim 18, further comprising determining a number of packaged semiconductor chips of the plurality of packaged semiconductor chips to connect in parallel after said providing the plurality of packaged semiconductor chips.

22. The method of claim 18, further comprising determining a number of packaged semiconductor chips of the plurality of packaged semiconductor chips to connect in series after said providing the plurality of packaged semiconductor chips.