

Description

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device and, according to the first part of claim 1 and to a technique effective for use in a one-chip microcomputer in which an ROM (i.e., Read Only Memory) to be stored with a data processing program is constructed of an EPROM (i.e., Electrically Programmable Read Only Memory).

In a one-chip microcomputer, a predetermined data processing is executed in accordance with a program which is written in the built-in ROM. Prior to the present invention, we have conceived the use of an EPROM as the built-in ROM. This use of the EPROM makes it possible to promptly provide a one-chip microcomputer which has the data processing function desired by the user and to improve the mass productivity. If a mask type ROM is used as the aforementioned ROM, more specifically, it takes time to fabricate a variety of masks during program development.

In case the EPROM is used as above, it would be convenient to conduct the writing operation by the use of an existing EPROM writer. As compared with the address space in the microcomputer, however, the ratio to be occupied by the EPROM is far smaller, e.g. at most 4K (4K x 8 bits) of an address space of 8K. As a result, errors for as many as half of the addresses are caused if the writing operation is conducted by the use of the existing EPROM writer (e.g., 8K x 8 bits = 64 Kbits) having the same address space as that of the microcomputer. In case the existing EPROM writer is used, more specifically, it is desirable that the construction of the usable EPROM writer be not restricted. In accordance with the existing EPROM writer, the address data are renewed sequentially from the start address, and the data to be written are sequentially outputted. The EPROM writer reads out the data written into the EPROM and checks them each time the writing operation into one address is executed. If, in this case, the start address of the EPROM is conveniently coincident with that of the EPROM, the data are written into the EPROM in a normal manner. However, the address space to be given to the built-in EPROM has not always a range convenient for the EPROM writer. In case the address data outside of the address range of the EPROM are outputted from the EPROM writer at the start of the data writing operation, no data are written into the EPROM. In this case, it is substantially impossible to check (verify) the write data after the data writing operation is conducted, because the address data designate memories other than the EPROM. As a result, errors, which should

not exist, are detected by executing the verifying operation. Thus, in the operation to write into the addresses in which the EPROM is present, the check (or verification) can be made, but all data become erroneous for the remaining write check so that no continuous write is conducted. Incidentally, a high-grade EPROM writer capable of arbitrarily designating the addressing range is present but has a high price and raises a problem in distribution.

Incidentally, the EPROM is disclosed in Japanese Patent Laid-Open No. 54 - 152933, for example.

Address discriminators used for protecting specific memory areas, I/O ports or storage facilities from access by unauthorised programs are disclosed in EP-A-0 109 504 and US-A-4 298 934 for example.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor integrated circuit device according to the preamble of claim 1 which may be programmed by a conventional EPROM - programmer. It is a further object to provide an operating method for the above device.

These objects are solved by the device of claim 1 and the method set forth in claim 11.

These and other objects and novel features of the present invention will become apparent from the description to be made herein with reference to the accompanying drawings.

Representatives of the present invention to be disclosed herein will be briefly described in the following. It is made possible to write a programmable ROM by means of a simple writer by adding a function to discriminate an address space, which is assigned to the programmable ROM to be stored with a data processing program, and a function to send out a signal identical to a blank to the output for the assigned address other than the address space assigned.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing one embodiment of the one-chip microcomputer to which the present invention is applied;

Fig. 2 is a diagram showing an address space for explaining the summary of the writing operation of the same;

Fig. 3 is a specific circuit diagram showing a control circuit WCON of Fig. 1;

Fig. 4 is a specific circuit diagram showing an EPROM of Fig. 1; and

Fig. 5 is a specific circuit diagram showing input and output ports of Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a block diagram showing the embodiment of the one-chip microcomputer to which the present invention is applied.

A rectangular encircled by double-dotted lines in Fig. 1 indicates an integrated circuit LSI. The respective circuit blocks formed in the rectangular construct the one-chip microcomputer as a whole and are formed in one semiconductor substrate made of silicon by the known semiconductor integrated circuit device fabricating technique.

Indicated by a symbol CPU is a micro processor which has its major component blocks exemplified as representatives. Specifically: symbol A indicates an accumulator; symbol X an index register; symbol CC a condition code register; symbol SP a stack pointer; symbols PCH and PCL program counters; symbol CPU-CONT a CPU controller; and symbol ALU an arithmetic logic operation unit.

The construction of such microprocessor CPU is well known in the art by "Fundamentals of Microcomputer" published by on April 10, 1983 by KK OHM and written by Koji YADA, for example, and its detail description is omitted.

Indicated at symbols I/O₁ and I/O₂ are input/output ports each having a data transmission direction register therein. The input/output port I/O₁ can be controlled by a control circuit WCON, and its specific example will be described later with reference to Fig. 3. On the other hand, symbol I indicates an input only port.

Indicated at symbol OSC is an oscillator for generating a highly accurate reference frequency signal by making use of a quartz crystal unit Xtal attached externally, although not especially limited thereto. Clock pulses necessary for the microprocessor CPU are generated by that reference frequency signal. This reference frequency signal is used as a reference time pulse of a timer, too. This timer is composed of a counter COUT, a prescaler PR and a controller CONT.

Indicated at symbol RAM is a random access memory which is used mainly as a memory circuit for temporary data.

Indicated at symbol EPROM is an electrically programmable read only memory which is to be written with a program for a variety of data processings.

The respective circuit blocks described above are connected around the micro processor CPU with one another through a bus BUS. This bus contains a data bus and an address bus. In the bus BUS, incidentally, the address bus ADD is linked to the external terminal and can be linked directly to the EPROM.

In the microcomputer of the present embodiment, the aforementioned EPROM is used, and there is provided the control circuit WCON for controlling the write of the EPROM and so on. The control circuit WCON receives a chip enable signal through an external terminal $\overline{CE}$ to enable the data to be written in the EPROM if the chip enable signal is in an EPROM direct access mode (or at a low level). If in the EPROM direct access mode, the control circuit WCON outputs a control signal $\overline{ce}$ for an interruption into the CPU control circuit CPU-CONT. This CPU control circuit CPU-CONT is interrupted by the control signal $\overline{ce}$ to control the CPU input/output port I/O₂, the input only port I and so on and to open the internal bus BUS. The control circuit WCON discriminates the voltage level fed from an external terminal V_{pp} to control the write/read operation modes and to feed its writing high voltage to the aforementioned EPROM. For example, if either a relative low voltage (e.g. 5 V) equal to an internal supply voltage V_{cc} or the ground potential (i.e., 0 V) of the circuit is supplied from the external terminal V_{pp}, the control circuit WCON generates a high-level discrimination signal. This high-level signal is used to establish the read operation mode, for example, when the EPROM is selected by the CPU. As a result, the verifying operation is made possible. If the writing high voltage (e.g., about 12 V) of the EPROM is fed from the external terminal V_{pp}, on the other hand, the control circuit WCON generates a low-level discrimination signal. For example, the data input buffer of the EPROM is rendered into its operative state in response to a low-level pulse generated by feeding the aforementioned high voltage V_{pp} for a predetermined period, and a write signal of a logic "0" generated by making use of the high voltage V_{pp} is prepared in accordance with the data fed from the data bus so that the logic "0" is written in a memory cell (e.g., a FAMOS transistor) selected. At this time, incidentally, the addressing of the EPROM is conducted in response to the address signal fed from the external terminal.

Moreover, the aforementioned address signal is fed to the address discrimination circuit contained in the aforementioned control circuit WCON. This address discrimination circuit inhibits the write operation and feeds out the read signal at that time as a blank (i.e., a logic "1"), although not limitative thereto, if it detects the set address other than those in the address space to which the EPROM is assigned. Incidentally, the aforementioned write inhibiting function need not be provided. This is because the non-existing address designation of the EPROM is conducted so that EPROM is not selected not to effect the writing operation.

The writing operation of the EPROM of the present embodiment will be schematically de-

scribed with reference to the address space diagram of Fig. 2.

Let the case be considered, in which, of address spaces A0 to A3 set by the address bus ADD: the address of the input/output port is assigned to A0 to A1; the area of the EPROM is assigned to A1 to A2; and an RAM area is assigned to the remaining A2 to A3. In the writing operation of the EPROM by the writer, then, the continuous writing operations of the area A0 to A3 are conducted, and the blank (i.e., the logic "1") is written for the set addresses (i.e., the hatched areas) of those other than the aforementioned EPROM areas (A0 to A1 and A2 to A3) when in the verifying operation (e.g., the read check after the write). For these writing operations, the control circuit WCON makes its output blank (i.e., the logic "1") for the set addresses other than those of the aforementioned EPROM areas (A0 to A1 and A2 to A3) so that the continuous writing operation can be conducted without any write error.

Fig. 3 shows a specific circuit of the control circuit WCON of Fig. 1.

The control circuit WCON is constructed of a voltage level detector VDT, an address discriminator ADC, and first and second control signal generators CSG₁ and CSG₂.

The voltage level detector VDT is composed of an input circuit HSC for voltage level detection and an inverter IV₂ as a buffer. The input circuit HSC is made of a hysteresis circuit so that it may be insensitive to the undesired noises applied to the external terminal Vpp, although not limitative thereto. The hysteresis circuit is not shown in detail because it is known per se, and both its two threshold voltages are made to take intermediate values between the supply voltage Vcc of the circuit and the high voltage such as 12 V fed to the terminal Vpp. With the construction described above, the voltage level detector VDL outputs a high-level discrimination signal ϕ_{vd} substantially equal to the supply voltage Vcc, when the supply voltage Vcc of the circuit or the ground voltage is fed to the external terminal Vpp, and a low-level discrimination signal ϕ_{vd} substantially equal to 0 V when the high voltage as high as about 12 V is fed to the external terminal Vpp.

The address discriminator ADC is constructed to discriminate the address space of the EPROM with reference to the upper three bits of the (not-shown) address bus in the internal bus BUS, although not especially limitative thereto. More specifically, the output of a NAND circuit ND₄ is set at a low level only when the most significant bit am and the next significant am-1 of the address signal are at the logics "0" and "1", whereas the output of a NAND circuit ND₅ is set at a low level only when the bits am and am-1 are at "1" and "0".

Likewise, the output of a NAND circuit ND₆ is set at the low level only when the bits am, am-1 and am-2 take the values "1", "1" and "0", respectively. In accordance with the outputs of those NAND circuits ND₄ to ND₆, the output of a NAND circuit ND₇, i.e., the output ϕ_{ad} of the address discriminator ADC is set at the high level, if the bits am, am-1 and am-2 are within the range "010" to "110", and otherwise at the low level. The output ϕ_{ad} is fed to the second control signal generator CSG₂ and to the first control signal generator CSG₁ as a kind of chip enable signal.

In response to the output ϕ_{vd} of the voltage level detector VDT, the chip enable signal fed through the external terminal CE and the output ϕ_{ad} of the address discriminator ADC, the first control signal generator CSG₁ outputs control signals ϕ_r , ϕ_w and $\overline{we}$ necessary for the EPROM, and a control signal $\overline{ce}$ indicating the direct access mode of the EPROM.

The control signal $\overline{ce}$ is made substantially identical to the chip enable signal (which will be referred to as a CE signal) of the external terminal CE, although not limitative thereto, such that it is set at the high level if the CE signal is at the high level, i.e., not the chip enable level, whereas it is set at the low level if the CE signal is at the low level, i.e., at the chip enable level.

The first control signal generator CSG₁ contains a not-shown OR circuit for generating the internal chip enable signal by OR composing the CE signal and an inverted level signal of the discrimination signal ϕ_{ad} outputted from the address discriminator ADC.

Although not especially limitative, the combination of the high level of the discrimination signal ϕ_{vd} and the chip enable level of the internal chip enable signal is deemed as the reading operation mode, whereas the combination of the low level of the discrimination signal ϕ_{vd} and the chip enable level of the internal chip enable signal is deemed as the program mode or the write mode. The non-chip enable level of the internal chip enable signal is deemed as a standby mode.

The control signal ϕ_r is used for controlling the operations of output buffer circuits OB₁ to OB_n of the EPROM, as will be described later with reference to Fig. 4, so that it is set at the high level in the reading operation mode and at the low level in the remaining modes.

The control signal ϕ_w is used for controlling the operations of input buffers DW₁ to DW_n of the EPROM so that it is set at the high level in the program mode and at the low level in the remaining modes.

The control signal $\overline{we}$ is changed in synchronism with the control signal ϕ_w so that it is set at the low level in the program mode and at the high

level in the remaining modes.

The second control signal generator CSG_2 is composed, as shown in Fig. 3, of a NAND circuit ND_3 and inverter circuits IV_3 to IV_5 so that it outputs a control signal ϕ_c in response to the outputs ϕ_{ad} and $\overline{ce}$ of the address discriminator ADC and the output ϕ_r of the first control signal generator CSG_1 . The control signal ϕ_c is set at the high level when the discrimination signal ϕ_{ad} and the control signal $\overline{ce}$ are at the low level and when the control signal ϕ_r is at the low level, i.e., when the reading operation mode is designated by the $\overline{CE}$ signal and the detection signal ϕ_{rd} and when the address other than those in the address space of the EPROM is designated by the address discriminator ADC.

The EPROM is composed, as shown in Fig. 4, of: an address decoder DEC made receptive of the address signal through the bus line BUS; a memory array MM having its word lines W_0 to W_k selected by the address decoder DEC; a column switch C-SW connected between the memory array MM and common data lines CD_1 to CD_n and adapted to be switched by the address decoder DEC; sense amplifiers SA_1 to SA_n linked to the common data lines CD_1 to CD_n , respectively; the output buffer circuits OB_1 to OB_n connected between the respective sense amplifiers SA_1 to SA_n and the bus line BUS; the input buffer circuits DW_1 to DW_n connected between the bus line BUS and the common data lines CD_1 to CD_n ; and a high-voltage supply circuit connected between the each word line of the memory array MM and the external terminal V_{pp} .

The address decoder DEC is made receptive of not only the address signal but also the control signal $\overline{we}$ and the write voltage V_{pp} to output the selection signal substantially at the selection level of the supply voltage V_{cc} of the circuit and the selection signal substantially at the non-selection level of the ground potential of the circuit to the column switch C-SW and the word lines W_0 to W_k of the memory array MM if the control signal $\overline{we}$ is at the high level. If the control signal $\overline{we}$ is generally at the low level of 0 V and if the voltage V_{pp} is generally at the write level of 12 V, the selection level of the selection signal to be fed to the column switch C-SW is set generally at the write level. At this time, moreover, the word level to be selected from the word lines W_0 to W_k is set generally at the write level by the high-voltage supply circuit HVS.

The output buffer circuits OB_1 to OB_n have their operations controlled by the control signal ϕ_r , such that they output such data signals to the bus line BUS if the control signal ϕ_r is at the high level as correspond to the data signals as outputted from the sense amplifiers SA_1 to SA_n . The output buffer

circuits OB_1 to OB_n are brought into their high-output impedance states if the control signal ϕ_r is at the low level.

The input buffer circuits DW_1 to DW_n receive the voltage V_{pp} , and have their operations controlled by the control signal ϕ_w . If the control signal ϕ_w is at the high level, the respective input buffer circuits DW_1 to DW_n outputs such a signal at the level of 0 V or the V_{pp} level to the respective common data lines CD_1 to CD_n as corresponds to the data signal fed through the bus line BUS. If the control signal ϕ_w is at the low level, the respective input buffer circuits DW_1 to DW_n are brought into the high-output impedance states.

As a result, when in the reading operations the read data signals of the memory array MM fed to the respective common data lines CD_1 to CD_n through the column switch C-SW are fed to the bus line BUS through the sense amplifiers SA_1 to SA_n and the output buffers OB_1 to OB_n , respectively.

When in the writing operations on the other hand, the high-voltage level write data signals outputted from the input buffer circuits DW_1 to DW_n are fed to the memory array MM through the common data lines CD_1 to CD_n and the column switch C-SW.

In accordance with the present embodiment, the input/output circuit I/O_1 has its construction modified slightly as the input/output circuit of the EPROM direct access mode for the ordinary input/output circuit.

A specific example of the construction of the input/output circuit I/O_1 is shown in Fig. 5. The input/output circuit I/O_1 contains: circuits composing the ordinary input/output circuit such as an output buffer OB and an input buffer IB linked to an input/output terminal I/O and data transmission direction registers RGr and RGi having their respective contents determined by the control signals fed through the bus line BUS; NAND circuits ND_1 to ND_3 , a gate circuit GC; an inverter circuit IV_1 ; and an OR circuit OR.

In accordance with this construction, the output of the NAND circuit ND_3 , i.e., the control input of the output buffer circuit OB is made identical to the output O_1 of the register RGr, if the control signal $\overline{ce}$ is at the high level, and to the control signal ϕ_r if the control signal $\overline{ce}$ is at the low level.

The gate circuit GC is made substantially identical to the circuit composed of the NAND circuits ND_1 to ND_3 . The output of the gate circuit GC, i.e., the control input of the input buffer circuit IB is made identical to the output O_2 of the register RGi, if the control signal $\overline{ce}$ is at the high level, and to the control signal ϕ_w if the control signal $\overline{ce}$ is at the low level.

The output of the OR circuit is set at the high level irrespective of the signal fed from the bus line

BUS if the signal ϕ_c is at the high level.

As a result, the output buffer and input buffer OB and IB have their respective operations controlled by the registers RGr and RGi if the control signal $\overline{ce}$ is at the high level, in other words, if the EPROM direct access mode is not designated.

The output buffer OB and the input buffer IB have their respective operations controlled by the control signals ϕ_r and ϕ_w irrespective of the outputs O_1 and O_2 of the registers RGr and RGi if the control signal $\overline{ce}$ is at the low level, in other words, if the EPROM direct access mode is designated.

In the EPROM direct access mode (namely, $\overline{ce}$ at the low level), if the control signal ϕ_w is set at the high level, the input buffer IB is accordingly brought into its operative state. In accordance with this, the write data signal fed from the EPROM writer to the input/output terminal I/O is fed to the EPROM of Fig. 4 through the input buffer IB and the bus line BUS.

If the control signal ϕ_r is at the high level in the EPROM direct access mode, the output buffer OB is accordingly brought into its operative state. In accordance with this, the outputs of the output buffers OB_1 to OB_n of Fig. 4 are outputted to the input/output terminal I/O through the OR circuit OR and the output buffer OB. If, at this time, the address space indicated by the address signal fed from the bus line BUS to the EPROM is out of that of the EPROM, the signal ϕ_c outputted from the circuit CSG₂ of Fig. 3 is set at the high level. In accordance with this, the signal at the high level is outputted from the output buffer OB of Fig. 5 irrespective of the signal level of the bus line BUS.

In the program of the EPROM by the EPROM writer, incidentally, either a socket especially for setting the semiconductor device of the present embodiment or a conversion socket for changing the pin arrangement is prepared and is linked to the socket which is mounted in the EPROM writer.

For verification of the EPROM, either the data corresponding to the address other than those of the address space of the EPROM or expectable values are all set at the (high level) "1". As a result, the signals outputted from the input/output circuit I/O₁ of Fig. 1 or 5 become coincident with the expectable values set in advance in the EPROM writer, when an address outside of the address space of the EPROM is designated.

According to the present invention, the following effects can be attained.

(1) By detecting the address designation in which the programmable ROM is not present and by blanking the read signal at that time, there can be attained an effect that the writer can continue its writing operation without any consideration into the ROM areas.

(2) Thanks to the effect (1), there can be attained another effect that the writing operation can be performed by the simplified writer which has the minimum writing function including the verifying operation.

(3) Thanks to the effects (1) and (2), there can be attained still another effect that a copying operation or the like can be easily conducted to write a plurality of semiconductor integrated circuit devices containing the programmable ROMs.

Although the present invention made by us has been described specifically in connection with the embodiment thereof, it should not be limited thereto but can naturally be modified in various manners within the scope of the gist thereof. For example, the programmable ROM should not be limited to the aforementioned EPROM but may be replaced by a variety of programmable ROMs such as an electrically writable PROM, e.g., an electrically erasable PROM EEPROM or an electrically unerasable PROM. In this modification, the control circuit WCON shown in Fig. 1 is made to conduct the write control according to the built-in programmable ROM. The signal level forcibly set when the address other than those of the address space of the programmable ROM may be either at the high level or at the low level.

Although the foregoing description has been directed mainly to the case in which the present invention is applied to the one-chip microcomputer providing the background thereof and having the built-in EPROM, the present invention should not be limited thereto but may be widely applied to a variety of semiconductor integrated circuit devices containing the programmable ROM and having a larger address space than that of the former.

Claims

1. A semiconductor integrated circuit device (LSI) including an electrically programmable read only memory (EPROM) into which data is written and subsequently checked by external writer means and including a control circuit (WCON) controlling the read/write operation of said electrically programmable read only memory, said device comprising:

a first external terminal to which an address signal is applied from said external writer means during said data write or data check operation, wherein the address space is divided into a first address space (A1 to A2) assigned to the electrically programmable read only memory (EPROM) and a second address space (A0 to A1 and A2 to A3) not assigned thereto,

a second external terminal through which



BUS if the signal ϕ_c is at the high level.

As a result, the output buffer and input buffer OB and IB have their respective operations controlled by the registers RGr and RGi if the control signal $\overline{ce}$ is at the high level, in other words, if the EPROM direct access mode is not designated.

The output buffer OB and the input buffer IB have their respective operations controlled by the control signals ϕ_r and ϕ_w irrespective of the outputs O_1 and O_2 of the registers RGr and RGi if the control signal $\overline{ce}$ is at the low level, in other words, if the EPROM direct access mode is designated.

In the EPROM direct access mode (namely, $\overline{ce}$ at the low level), if the control signal ϕ_w is set at the high level, the input buffer IB is accordingly brought into its operative state. In accordance with this, the write data signal fed from the EPROM writer to the input/output terminal I/O is fed to the EPROM of Fig. 4 through the input buffer IB and the bus line BUS.

If the control signal ϕ_r is at the high level in the EPROM direct access mode, the output buffer OB is accordingly brought into its operative state. In accordance with this, the outputs of the output buffers OB_1 to OB_n of Fig. 4 are outputted to the input/output terminal I/O through the OR circuit OR and the output buffer OB. If, at this time, the address space indicated by the address signal fed from the bus line BUS to the EPROM is out of that of the EPROM, the signal ϕ_c outputted from the circuit CSG_2 of Fig. 3 is set at the high level. In accordance with this, the signal at the high level is outputted from the output buffer OB of Fig. 5 irrespective of the signal level of the bus line BUS.

In the program of the EPROM by the EPROM writer, incidentally, either a socket especially for setting the semiconductor device of the present embodiment or a conversion socket for changing the pin arrangement is prepared and is linked to the socket which is mounted in the EPROM writer.

For verification of the EPROM, either the data corresponding to the address other than those of the address space of the EPROM or expectable values are all set at the (high level) "1". As a result, the signals outputted from the input/output circuit I/O₁ of Fig. 1 or 5 become coincident with the expectable values set in advance in the EPROM writer, when an address outside of the address space of the EPROM is designated.

According to the present invention, the following effects can be attained.

(1) By detecting the address designation in which the programmable ROM is not present and by blanking the read signal at that time, there can be attained an effect that the writer can continue its writing operation without any consideration into the ROM areas.

(2) Thanks to the effect (1), there can be attained another effect that the writing operation can be performed by the simplified writer which has the minimum writing function including the verifying operation.

(3) Thanks to the effects (1) and (2), there can be attained still another effect that a copying operation or the like can be easily conducted to write a plurality of semiconductor integrated circuit devices containing the programmable ROMs.

Although the present invention made by us has been described specifically in connection with the embodiment thereof, it should not be limited thereto but can naturally be modified in various manners within the scope of the gist thereof. For example, the programmable ROM should not be limited to the aforementioned EPROM but may be replaced by a variety of programmable ROMs such as an electrically writable PROM, e.g., an electrically erasable PROM EEPROM or an electrically unerasable PROM. In this modification, the control circuit WCON shown in Fig. 1 is made to conduct the write control according to the built-in programmable ROM. The signal level forcibly set when the address other than those of the address space of the programmable ROM may be either at the high level or at the low level.

Although the foregoing description has been directed mainly to the case in which the present invention is applied to the one-chip microcomputer providing the background thereof and having the built-in EPROM, the present invention should not be limited thereto but may be widely applied to a variety of semiconductor integrated circuit devices containing the programmable ROM and having a larger address space than that of the former.

Claims

1. A semiconductor integrated circuit device (LSI) including an electrically programmable read only memory (EPROM) into which data is written and subsequently checked by external writer means and including a control circuit (WCON) controlling the read/write operation of said electrically programmable read only memory, said device comprising:

a first external terminal to which an address signal is applied from said external writer means during said data write or data check operation, wherein the address space is divided into a first address space (A1 to A2) assigned to the electrically programmable read only memory (EPROM) and a second address space (A0 to A1 and A2 to A3) not assigned thereto,

a second external terminal through which



data is written to the electrically programmable read only memory (EPROM) from the external writer means or read from the electrically programmable read only memory (EPROM) to the external writer means during said data write or data check operation, and

a third external terminal (Vpp, CE) to which an operation select signal controlling said data write and said data check operation is supplied,

characterized in that said control circuit (WCON) further comprises

an address discriminator (ADC, WCON) discriminating whether or not the address signal received from said first external terminal designates an address in said first address space (A1 to A2) and outputting a discrimination result signal (θ_{ad}), and

a control signal generator (CSG1, CSG2, WCON) receiving said discrimination result signal (θ_{ad}) and said operation select signal (Vpp, CE), detecting whether the operation selected by said external writer means is the data write or data check operation, and outputting a first control signal (θ_c) to set the data to be outputted on said second external terminal to a predetermined level in case the data check operation is selected and the address signal designates an address in said second address space (A0 to A1, A0 to A3).

2. The device of claim 1, characterized in that the level of data inputted by the external writer means to the second external terminal in the data write operation in case that the data is to be written into said second address space (A0 to A1, A2 to A3) corresponds to said predetermined level.

3. The device of claim 1 or 2, characterized by an input-output circuit (I/O) having its input and output terminals coupled to said second external terminal,

wherein the data is written to the electrically programmable read only memory (EPROM) from the external writer means via said second external terminal and said input-output circuit (I/O) and wherein the data is read out from the electrically programmable read only memory (EPROM) to the external writer means via said input-output circuit (I/O) and said second external terminal.

4. The device of claim 3, characterized in that said first control signal (θ_c) is supplied to said input-output circuit (I/O).

5. The device of claim 3 or 4, characterized by a bus line (BUS) coupled to said first external terminal and to said second external terminal via said input-output circuit (I/O),

wherein the address input terminal of said electrically programmable read only memory (EPROM) is coupled to said first external terminal via said bus line (BUS) and the data input-output terminal of the electrically programmable read only memory (EPROM) is coupled to said second external terminal via said bus line (BUS) and said input-output circuit (I/O), and

wherein said address discriminator (ADC) is coupled to said first external terminal via said bus line (BUS).

6. The device of any of claims 1 to 5, characterized in that said control signal generator (CSG) includes means (CSG1) for outputting, in response to said discrimination result signal (θ_{ad}) and said operation select signal (Vpp, CE), a second control signal (θ_r , θ_w , θ_e) controlling the write or read operations of said electrically programmable read only memory (EPROM).

7. The device of claim 6, characterized in that said second control signal (θ_r , θ_w , θ_e) is supplied to said electrically programmable read only memory.

8. The device of any of claims 1 to 7, characterized by a microprocessor (CPU) coupled to the electrically programmable read only memory (EPROM),

wherein the data written into the electrically programmable read only memory (EPROM) constitutes a program and the microprocessor (CPU) executes a predetermined data processing in accordance with the program.

9. The device of claim 8, characterized by a random access memory (RAM) coupled to the microprocessor (CPU) for providing a work area of the microprocessor, wherein the second address space (A0 to A1, A2 to A3) comprises a space (A2 to A3) assigned to the random access memory (RAM).

10. The device of claim 8 or 9, characterized by register means (M1) coupled to the microprocessor (CPU) for storing data therein, wherein the second address space (A0 to A1 and A2 to A3) further comprises a space (A0 to A1) assigned to the register means (M1).



11. A method of programming and subsequently checking an electrically programmable read only memory (EPROM) included in a semiconductor integrated circuit device (LSI) by external writer means, an address space of the semiconductor integrated circuit device (LSI) being divided into a first address space (A1 to A2) assigned to the electrically programmable read only memory (EPROM) and a second address space (A0 to A1 and A2 to A3) not assigned thereto,

comprising the following steps:

supplying an address signal and a data signal from the writer means to the semiconductor integrated circuit device (LSI),

discriminating whether an address designated by the address signal is in the first address space (A1 to A2) or in the second address space,

writing the data indicated by the data signal into the electrically programmable read only memory (EPROM) at the address designated by the address signal and subsequently reading it by the external writer means to verify the programmed data, if the address is in the first address space (A1 to A2), and

providing a predetermined data signal from the semiconductor integrated circuit device (LSI) to the external writer means in a reading step by the external writer means, if the address designated by the address signal is in the second address space (A0 to A1, A2 to A3).

Patentansprüche

1. Integrierter Halbleiter-Schaltkreis (LSI) mit einem elektrisch programmierbaren Festpeicher (EPROM), in den Daten geschrieben werden und diese anschließend von einer externen Schreibeinrichtung geprüft werden, und mit einer Steuereinheit (WCON), die den Lese/Schreibvorgang des elektrisch programmierbaren Festspeichers steuert, wobei der Schaltkreis umfaßt:

einen ersten externen Anschluß, an den während des Datenschreib- oder Datenprüfvorgangs ein Adressensignal von der externen Schreibeinrichtung angelegt wird, wobei der Adressenbereich in einen ersten, dem elektrisch programmierbaren Festpeicher (EPROM) zugewiesenen Adressenbereich (A1 bis A2) und einen zweiten, diesem nicht zugewiesenen Adressenbereich (A0 bis A1 und A2 bis A3) aufgeteilt ist,

einen zweiten externen Anschluß, über den während des Datenschreib- bzw. des Datenprüfvorgangs Daten von der externen Schreibeinrichtung in den elektrisch programmierbaren

Festspeicher (EPROM) geschrieben oder vom elektrisch programmierbaren Festpeicher (EPROM) an die externe Schreibeinrichtung gelesen werden, und

einen dritten externen Anschluß (Vpp, CE), an den ein den Datenschreib- und den Datenprüfvorgang steuerndes Vorgangswahlsignal angelegt wird,

dadurch gekennzeichnet, daß die Steuereinheit (WCON) weiterhin umfaßt:

eine Adressenunterscheidungseinheit (ADC, WCON), die unterscheidet, ob das vom ersten externen Anschluß empfangene Adressensignal eine Adresse im ersten Adressenbereich (A1 bis A2) bezeichnet oder nicht, und ein Unterscheidungsergebnissignal (θ_{ad}) ausgibt, und

einen Steuersignalgenerator (CSG1, CSG2, WCON), der das Unterscheidungsergebnissignal (θ_{ad}) und das Vorgangswahlsignal (Vpp, CE) empfängt, feststellt, ob der von der externen Schreibeinrichtung ausgewählte Vorgang ein Datenschreib- oder ein Datenprüfvorgang ist, und ein erstes Steuersignal (θ_c) ausgibt, um die über den zweiten externen Anschluß auszugebenden Daten auf einen vorgegebenen Pegel zu setzen, falls der Datenprüfvorgang gewählt ist und das Adressensignal eine Adresse im zweiten Adressenbereich (A0 bis A1, A0 bis A3) bestimmt.

2. Schaltkreis nach Anspruch 1, dadurch gekennzeichnet, daß der Pegel der beim Datenschreibvorgang von der externen Schreibeinrichtung an den zweiten externen Anschluß gelieferten Daten dem vorgegebenen Pegel entsprechen, falls diese Daten in den zweiten Adressenbereich (A0 bis A1, A2 bis A3) geschrieben werden sollen.

3. Schaltkreis nach Anspruch 1 oder 2, gekennzeichnet durch

eine Ein-/Ausgabeschaltung (I/O), deren Ein- und Ausgabeanschlüsse mit dem zweiten externen Anschluß verbunden sind,

wobei die Daten von der externen Schreibeinrichtung über den zweiten externen Anschluß und die Ein-/Ausgabeschaltung (I/O) in den elektrisch programmierbaren Festpeicher (EPROM) geschrieben werden und wobei die Daten aus dem elektrisch programmierbaren Festpeicher (EPROM) über die Ein-/Ausgabeschaltung (I/O) und den zweiten externen Anschluß an die externe Schreibeinrichtung ausgelesen werden.

4. Schaltkreis nach Anspruch 3, dadurch gekennzeichnet, daß das erste Steuersignal (θ_c) an



die Ein-/Ausgabeschaltung (I/O) geliefert werden.

5. Schaltkreis nach Anspruch 3 oder 4, gekennzeichnet durch

eine Sammelleitung (BUS), die mit dem ersten externen Anschluß und mit dem zweiten externen Anschluß über die Ein-/Ausgabeschaltung (I/O) verbunden ist,

wobei der Adresseneingabeanschluß des elektrisch programmierbaren Festspeichers (EPROM) über diese Sammelleitung (BUS) mit dem ersten externen Anschluß verbunden ist und der Daten-Ein-/Ausgabeanschluß des elektrisch programmierbaren Festspeichers (EPROM) über die Sammelleitung (BUS) und die Ein-/Ausgabeschaltung (I/O) mit dem zweiten externen Anschluß verbunden ist, und

wobei die Adressenunterscheidungseinheit (ADC) über die Sammelleitung (BUS) mit dem ersten externen Anschluß verbunden ist.

6. Schaltkreis nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß der Steuersignal-generator (CSG) eine Einrichtung (CSG1) zur Ausgabe eines zweiten Steuersignals (Θ_r , Θ_w , w_e) in Antwort auf das Unterscheidungsergebnissignal (Θ_{ad}) und das Vorgangswahlsignal (V_{pp} , CE) umfaßt, welches die Schreib- oder Lesevorgänge des elektrisch programmierbaren Festspeichers (EPROM) steuert.

7. Schaltkreis nach Anspruch 6, dadurch gekennzeichnet, daß das zweite Steuersignal (Θ_r , Θ_w , w_e) dem elektrisch programmierbaren Festspeicher (EPROM) zugeführt wird.

8. Schaltkreis nach einem der Ansprüche 1 bis 7, gekennzeichnet durch einen Mikroprozessor (CPU), der mit dem elektrisch programmierbaren Festspeicher (EPROM) verbunden ist,

wobei die in den elektrisch programmierbaren Festspeicher (EPROM) geschriebenen Daten ein Programm darstellen und der Mikroprozessor (CPU) vorgegebene Datenverarbeitungen gemäß dem Programm ausführt.

9. Schaltkreis nach Anspruch 8, gekennzeichnet durch einen Speicher mit wahlfreiem Zugriff (RAM), der mit dem Mikroprozessor (CPU) zur Bereitstellung eines Arbeitsbereichs für den Mikroprozessor verbunden ist, wobei der zweite Adressenbereich (A0 bis A1, A2 und A3) einen Bereich (A2 bis A3) umfaßt, der dem Speicher mit wahlfreiem Zugriff (RAM) zugeordnet ist.

10. Schaltkreis nach Anspruch 8 oder 9, gekennzeichnet durch eine Registereinrichtung (M1), die mit dem Mikroprozessor (CPU) zur Speicherung von Daten darin verbunden ist, wobei der zweite Adressenbereich (A0 bis A1 und A2 bis A3) ferner einen Bereich (A0 bis A1) umfaßt, welcher der Registereinrichtung (M1) zugeordnet ist.

11. Verfahren zur Programmierung und darauffolgenden Prüfung eines in einem integrierten Halbleiterschaltkreis (LSI) enthaltenen elektrisch programmierbaren Festspeichers (EPROM) mittels einer externen Schreibeinrichtung, wobei ein Adressenbereich des integrierten Halbleiterschaltkreises (LSI) in einen ersten, dem elektrisch programmierbaren Festspeicher (EPROM) zugeordneten Adressenbereich (A1 bis A2) und einen zweiten, diesem nicht zugewiesenen Adressenbereich (A0 bis A1, A2 bis A3), geteilt ist, umfassend die folgenden Schritte:

Zuführen eines Adressensignals und eines Datensignals von der Schreibeinrichtung an den integrierten Halbleiterschaltkreis (LSI),

Unterscheiden, ob die vom zweiten Adressensignal bestimmte Adresse im ersten Adressenbereich (A1 oder A2) oder im zweiten Adressenbereich liegt,

Schreiben der vom Datensignal bezeichneten Daten in den elektrisch programmierbaren Festspeicher (EPROM) an die durch das Adressensignal bestimmte Adresse und nachfolgendes Lesen derselben durch die externe Schreibeinrichtung zur Überprüfung der programmierten Daten, wenn die Adresse im ersten Adressenbereich (A1 bis A2) liegt, und

Ausgeben eines vorgegebenen Datensignals aus dem integrierten Halbleiterschaltkreis (LSI) an die externe Schreibeinrichtung in einem Leseschritt durch die externe Schreibeinrichtung, wenn die durch das Adressensignal bestimmte Adresse im zweiten Adressenbereich (A0 bis A1, A2 bis A3) liegt.

Revendications

1. Dispositif de circuit intégré à semiconducteurs (LSI) comprenant une mémoire morte électriquement programmable (EPROM) dans laquelle des données sont écrites et ultérieurement contrôlées par un moyen d'écriture extérieur et comprenant un circuit de commande (WCON) commandant l'opération de lecture/écriture de ladite mémoire morte électriquement programmable, ledit dispositif comportant:

une première borne extérieure à laquelle est appliqué un signal d'adresse depuis le



moyen d'écriture extérieur durant ladite opération d'écriture ou de contrôle de données, l'espace d'adresse étant divisé en un premier espace d'adresse (A1 à A2) affecté à la mémoire morte électriquement programmable (EPROM) et en un second espace d'adresse (A0 à A1 et A2 à A3) non affecté à celle-ci,

une seconde borne extérieure par l'intermédiaire de laquelle des données sont écrites dans la mémoire morte électriquement programmable (EPROM) à partir du moyen d'écriture extérieur ou lues à partir de la mémoire morte électriquement programmable (EPROM) vers le moyen d'écriture extérieur durant ladite opération d'écriture de données ou de contrôle de données, et

une troisième borne extérieure (V_{pp} , CE) à laquelle un signal de sélection d'opération commandant ladite opération d'écriture de données et ladite opération de contrôle de données est appliqué, caractérisé en ce que ledit signal de commande (WCON) comporte en outre

un discriminateur d'adresse (ADC, WCON) discriminant si oui ou non le signal d'adresse reçu de ladite première borne extérieure désigne une adresse dans ledit premier espace d'adresse (A1 à A2) et délivrant un signal de résultat de discrimination (θ_{ad}), et

un générateur de signaux de commande (CSG1, CSG2, WCON) recevant ledit signal de résultat de discrimination (θ_{ad}) et ledit signal de sélection d'opération (V_{pp} , CE), détectant si l'opération sélectionnée par ledit moyen d'écriture extérieur est l'opération d'écriture de données ou de contrôle de données, et délivrant un premier signal de commande (θ_c) pour fixer les données à délivrer sur ladite seconde borne extérieure à un niveau prédéterminé dans le cas où l'opération de contrôle de données est sélectionnée et le signal d'adresse désigne une adresse dans ledit second espace d'adresse (A0 à A1, A0 à A3).

2. Dispositif selon la revendication 1, caractérisé en ce que le niveau de données délivrées par le moyen d'écriture extérieur à la seconde borne extérieure au cours de l'opération d'écriture de données dans le cas où les données doivent être écrites dans ledit second espace d'adresse (A0 à A1, A2 à A3) correspond audit niveau prédéterminé.

3. Dispositif selon la revendication 1 ou 2, caractérisé par un circuit d'entrée-sortie (I/O) ayant ses bornes d'entrée et de sortie couplées à ladite seconde borne extérieure, les données étant écrites dans la mémoire morte électri-

quement programmable (EPROM) à partir du moyen d'écriture extérieur par l'intermédiaire de ladite seconde borne extérieure et dudit circuit d'entrée-sortie (I/O) et les données étant lues depuis la mémoire électriquement programmable (EPROM) vers le moyen d'écriture extérieur par l'intermédiaire dudit circuit d'entrée-sortie (I/O) et ladite seconde borne extérieure.

4. Dispositif selon la revendication 3, caractérisé en ce que ledit premier signal de commande (θ_c) est appliqué audit circuit d'entrée-sortie (I/O).

5. Dispositif selon la revendication 3 ou 4, caractérisé par une ligne de bus (BUS) couplée à ladite borne extérieure et à ladite seconde borne extérieure par l'intermédiaire dudit circuit d'entrée-sortie (I/O),

la borne d'entrée d'adresse de ladite mémoire morte électriquement programmable (EPROM) étant couplée à ladite première borne extérieure par l'intermédiaire de ladite ligne de bus (BUS), la borne d'entrée-sortie de données de la mémoire morte électriquement programmable (EPROM) étant couplée à ladite seconde borne extérieure par l'intermédiaire de la ligne de bus (BUS) et dudit circuit d'entrée-sortie (I/O), et

ledit discriminateur d'adresse (ADC) étant couplé à ladite première borne extérieure par l'intermédiaire de ladite ligne de bus (BUS).

6. Dispositif selon l'une quelconque des revendications 1 à 5, caractérisé en ce que ledit générateur de signaux de commande (CSG) comprend des moyens (CSG1) pour délivrer, en réponse audit signal de résultat de discrimination (θ_{ad}) et dudit signal de sélection d'opération (V_{pp} , CE), un second signal de commande (θ_r , θ_w , w_e) commandant les opérations d'écriture ou de lecture de ladite mémoire morte électriquement programmable (EPROM).

7. Dispositif selon la revendication 6, caractérisé en ce que ledit second signal de commande (θ_r , θ_w , w_e) est appliqué à ladite mémoire morte électriquement programmable.

8. Dispositif selon l'une quelconque des revendications 1 à 7, caractérisé par un microprocesseur (CPU) couplé à la mémoire électriquement programmable (EPROM),

les données écrites dans la mémoire morte électriquement programmable (EPROM) constituant un programme et le microproces-



seur (CPU) exécutant un traitement de données prédéterminé conformément au programme.

9. Dispositif selon la revendication 8, caractérisé par une mémoire à accès sélectif (RAM) couplée au microprocesseur (CPU) pour assurer une zone de travail du microprocesseur, le second espace d'adresse (A0 à A1, A2 à A3) comportant un espace (A2 à A3) affecté à la mémoire à accès sélectif (RAM). 5
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10. Dispositif selon la revendication 8 ou 9, caractérisé par un registre (M1) couplé au microprocesseur (CPU) pour y mémoriser des données, le second espace d'adresse (A0 à A1 et A2 à A3) comportant en outre un espace (A0 à A1) affecté au registre (M1). 15

11. Procédé de programmation et de contrôle ultérieur d'une mémoire morte électriquement programmable (EPROM) compris dans un dispositif de circuit intégré à semiconducteurs (LSI) par un moyen d'écriture extérieur, un espace d'adresse du dispositif de circuit intégré à semiconducteurs (LSI) étant divisé en un premier espace d'adresse (A1 à A2) affecté à la mémoire morte électriquement programmable (EPROM) et un second espace d'adresse (A0 à A1 et A2 à A3) non affecté à celle-ci, 20
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comportant les étapes suivantes consistant à :
 délivrer un signal d'adresse et un signal de données provenant du moyen d'écriture au dispositif de circuit intégré à semiconducteurs (LSI), 35
 discriminer si une adresse désignée par le signal d'adresse se trouve dans le premier espace d'adresse (A1 à A2) ou dans le second espace d'adresse, 40
 écrire les données indiquées par le signal de données dans la mémoire morte électriquement programmable (EPROM) à l'adresse désignée par le signal d'adresse et ultérieurement à la lecture par le moyen d'écriture extérieur pour vérifier les données programmées, si l'adresse se trouve dans le premier espace d'adresse (A1 à A2), et 45
 délivrer un signal de données prédéterminé provenant du dispositif de circuit intégré à semiconducteurs (LSI) au moyen d'écriture extérieur au cours d'une étape de lecture par le moyen d'écriture extérieur, si l'adresse désignée par le signal d'adresse se trouve dans le second espace d'adresse (A0 à A1, A2 à A3). 50
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