What is claimed is:

1. A method of operating a memory device, comprising:

determining whether to access a first memory cell of a first memory cell array or a second memory cell of a second memory cell array, wherein a first digit line coupled to the first memory cell is coupled to a paging buffer register comprising a sense amplifier; and

operating a transfer gate based at least in part on determining to read the second memory cell of the second memory cell array, wherein the transfer gate is configured to selectively couple a second digit line coupled to the second memory cell to the paging buffer register through the first digit line, wherein the first memory cell comprises a first ferroelectric memory cell and the second memory cell comprises a second ferroelectric memory cell.

2. The method of claim 1, wherein the first ferroelectric memory cell is configured to operate in a volatile mode and the second ferroelectric memory cell is configured to operate in a non-volatile mode.

3. The method of claim 1, wherein operating the transfer gate comprises:

closing the transfer gate when determining to access the second memory cell, to couple the second digit line to the paging buffer register through the first digit line.

4. The method of claim 3, further comprising:

transferring a data bit, after closing the transfer gate, at least one of: between the second memory cell and a data processor, or between the second memory cell and the first memory cell.

5. The method of claim **1**, wherein operating the transfer gate comprises:

opening the transfer gate when determining to not access the second memory cell.

6. A method of operating a memory device, comprising:

determining whether to access a first memory cell of a first memory cell array or a second memory cell of a second memory cell array, wherein a first digit line coupled to the first memory cell is coupled to a paging buffer register comprising a sense amplifier, wherein the first digit line is coupled to a first plurality of memory cells including the first memory cell; and

operating a transfer gate based at least in part on determining to read the second memory cell of the second memory cell array, wherein the transfer gate is configured to selectively couple a second digit line coupled to the second memory cell to the paging buffer register through the first digit line, wherein the second digit line is coupled to a second plurality of memory cells including the second memory cell, and wherein the first plurality of memory cells comprises fewer memory cells than the second plurality of memory cells.

7. A method of operating a memory device, comprising:

determining whether to access a first memory cell of a first memory cell array or a second memory cell of a second memory cell array, wherein a first digit line coupled to the first memory cell is coupled to a paging buffer register comprising a sense amplifier;

operating a transfer gate based at least in part on determining to read the second memory cell of the second memory cell array, wherein the transfer gate is configured to selectively couple a second digit line coupled to the second memory cell to the paging buffer register through the first digit line; and

operating the first memory cell array as an embedded cache for the second memory cell array.

8. A method of operating a memory device, comprising:

determining whether to access a first memory cell of a first memory cell array or a second memory cell of a second memory cell array, wherein a first digit line coupled to the first memory cell is coupled to a paging buffer register comprising a sense amplifier;

operating a transfer gate based at least in part on determining to read the second memory cell of the second memory cell array, wherein the transfer gate is configured to selectively couple a second digit line coupled to the second memory cell to the paging buffer register through the first digit line; and

preventing inversion of a ferroelectric film of a capacitor of the first memory cell by biasing a cell plate of the first memory cell.

9. The method of claim **8**, further comprising:

biasing each cell plate of each memory cell in the second memory cell array to a common voltage.

10. The method of claim **8**, further comprising:

independently biasing a voltage of each cell plate of each memory cell in the second memory cell array.

11. An apparatus, comprising:

a first memory cell array comprising a first digit line connected to a first plurality of memory cells;

a second memory cell array comprising a second digit line connected to a second plurality of memory cells;

a paging buffer register comprising a first sense amplifier shared by the first memory cell array and the second memory cell array, wherein the first digit line is coupled to the first sense amplifier; and

a first transfer gate operable to selectively couple the second digit line to the first sense amplifier through the first digit line, wherein the first memory cell array comprises a first ferroelectric memory cell and the second memory cell array comprises a second ferroelectric memory cell.

12. The apparatus of claim **11**, wherein the first plurality of memory cells comprises fewer memory cells than the second plurality of memory cells.

13. The apparatus of claim **11**, wherein the second memory cell array further comprises a third digit line connected to a third plurality of memory cells, wherein the paging buffer register further comprises a second sense amplifier, and wherein the apparatus further comprises:

a third memory cell array comprising a fourth digit line connected to a fourth plurality of memory cells, wherein the second sense amplifier is shared by the third plurality of memory cells and the fourth plurality of memory cells, wherein the fourth digit line is coupled to the second sense amplifier; and

a second transfer gate operable to selectively couple the third digit line to the second sense amplifier through the fourth digit line.

14. The apparatus of claim **13**, wherein the first plurality of memory cells comprises a first subset of memory cells coupled to eau-pie-de the first digit line and a second subset of memory cells coupled to the first digit line, and wherein the first digit line is coupled to the first sense amplifier between the first subset of memory cells and the second subset of memory cells.

15. The apparatus of claim **11**, wherein the first sense amplifier comprises:

a first circuit operable to bias the first digit line to a first voltage prior to reading from the first memory cell array; and

a second circuit operable to bias the first digit line and the second digit line to a second voltage prior to reading from the second memory cell array.

16. The apparatus of claim **15**, wherein the first sense amplifier comprises:

a third circuit operable to bias the first digit line and the second digit line, in parallel, to the second voltage.

17. The apparatus of claim **16**, wherein a cell plate of each memory cell in the second plurality of memory cells is connected to a common voltage rail.

18. The apparatus of claim **11**, wherein the first memory cell array comprises a first plurality of ferroelectric memory cells that includes a first ferroelectric memory cell and the second memory cell array comprises a second plurality of ferroelectric memory cells that includes a second ferroelectric memory cell.

19. The apparatus of claim **18**, wherein the first plurality of ferroelectric memory cells is configured to operate in a volatile mode and the second plurality of ferroelectric memory cells is configured to operate in a non-volatile mode.

20. An apparatus, comprising:

a first memory cell array comprising a first digit line connected to a first plurality of memory cells;

a second memory cell array comprising a second digit line connected to a second plurality of memory cells;

a paging buffer register comprising a first sense amplifier shared by the first memory cell array and the second memory cell array, wherein the first digit line is coupled to the first sense amplifier;

a first transfer gate operable to selectively couple the second digit line to the first sense amplifier through the first digit line, wherein each of a plurality of access lines is coupled to a first memory cell in a first subset of memory cells and a second memory cell in a second subset of memory cells; and

a first access line of the plurality of access lines is coupled to a functioning memory cell in the first subset of memory cells and a non-functioning memory cell in the second subset of memory cells.

21. A data processing system, comprising:

a processor;

a main memory; and

a memory controller configured to transfer data between the main memory and a data processor, wherein the main memory comprises:

a first memory cell array comprising a first digit line connected to a first plurality of memory cells;

a second memory cell array comprising a second digit line connected to a second plurality of memory cells;

a paging buffer register comprising a first sense amplifier shared by the first memory cell array and the second memory cell array, wherein the first digit line is coupled to the first sense amplifier; and

a first transfer gate operable to selectively couple the second digit line to the first sense amplifier through the first digit line, wherein the first memory cell array comprises a first ferroelectric memory cell and the second memory cell array comprises a second ferroelectric memory cell.

22. The data processing system of claim **21**, wherein the first memory cell array is used by the processor as a cache for the second memory cell array.

23. The data processing system of claim **22**, wherein the processor issues at least one of: a read command to cause the memory controller to close the transfer gate and transfer data from the second memory cell array to the first memory cell array, or a write command to cause the memory controller to open the transfer gate and transfer data from the first memory cell array to the second memory cell array.

24. A data processing system, comprising:

a processor;

a main memory; and

a memory controller configured to transfer data between the main memory and a data processor, wherein the main memory comprises:

a first memory cell array comprising a first digit line connected to a first plurality of memory cells;

a second memory cell array comprising a second digit line connected to a second plurality of memory cells;

a paging buffer register comprising a first sense amplifier shared by the first memory cell array and the second memory cell array, wherein the first digit line is coupled to the first sense amplifier; and

a first transfer gate operable to selectively couple the second digit line to the first sense amplifier through the first digit line, wherein the processor causes the memory controller to operate the transfer gate and write a first type of data to the first memory cell array, or write a second type of data to the second memory cell array.