CLAIMS

1. A memory system comprising: a sense amplifier configured to amplify a voltage swing, the sense amplifier electrically coupled to a first bitline and a second bitline associated with a column of a memory array; a bl transistor electrically coupled to the first bitline, wherein the bl transistor is configured to receive as input a first electrical signal from the first bitline based on the first bitline being discharged; and a blb transistor electrically coupled to the second bitline, wherein the blb transistor is configured to receive as input a second electrical signal from the second bitline based on the second bitline being discharged, wherein an output of the bl transistor and an output of the blb transistor are electrically coupled together as a common output, wherein the sense amplifier is configured to receive as an input the common output of the bl transistor and the blb transistor as a sense amplifier enable signal, and wherein the sense amplifier is further configured to measure a voltage differential across the first bitline and the second bitline based on reception of the sense amplifier enable signal.

2. The memory system of claim 1, wherein the memory array comprises a static random-access memory (SRAM) array.

3. The memory system of claim 1, wherein the bl transistor is configured to conduct electricity when the first bitline is discharged, and wherein the blb transistor is configured to be powered when the second bitline is discharged.

4. The memory system of claim 1, wherein the common output of the bl transistor and the blb transistor are connected across two or more columns in the memory array configured to be accessed together.

5. The memory system of claim 1, further comprising a multiplexor electrically coupled between a plurality of bitlines and the sense amplifier, the plurality of bitlines including the first bitline and the second bitline, the multiplexor configured to select a pair of bitlines of the plurality of bitlines and to output the pair of bitlines to the sense amplifier.

6. The memory system of claim 1, further comprising a program clock transistor electrically coupled to the bl transistor and the blb transistor, wherein the program clock transistor is configured to disable the common output of the bl transistor and the blb transistor.

7. The memory system of claim 6, wherein a size of the program clock transistor determines a strength of the program clock transistor.

8. The memory system of claim 6, wherein a gate voltage of the program clock transistor determines a strength of the program clock transistor when it is conducting electricity during a read operation.

9. The memory system of claim 6, wherein the program clock transistor is configured to disable the common output of the bl transistor and the blb transistor based on enabling a subset of program clock transistors.

10. The memory system of claim 1, further comprising a multiplexor configured to select an input from a program sense amplifier enable signal transistor or the common output of the bl transistor and the blb transistor.

11. The memory system of claim 1, further comprising a discharge transistor configured to disable the common output of the bl transistor and the blb transistor.

12. The memory system of claim 1, further comprising: a plurality of columns of the memory array including the column, wherein less than all of the plurality of columns are associated with a plurality of pairs of bl transistors and blb transistors including the bl transistor and the blb transistor.

13. A method of operating a memory system comprising: receiving, at a bl transistor electrically coupled to a first bitline of a column of a memory array, a first electrical signal from the first bitline based on the first bitline being discharged; receiving, at a blb transistor electrically coupled to a second bitline of the column of the memory array, a second electrical signal from the second bitline based on the second bitline being discharged, wherein an output of the bl transistor and an output of the blb transistor are electrically coupled together as a common output; receiving, at a sense amplifier configured to amplify a voltage swing, the common output of the bl transistor and the blb transistor as a sense amplifier enable signal, wherein the sense amplifier is electrically coupled to the first bitline and the second bitline; and measuring, by the sense amplifier, a voltage differential across the first bitline and the second bitline based on reception of the sense amplifier enable signal.

14. The method of claim 13, wherein the memory array comprises a static random-access memory (SRAM) array.

15. The method of claim 13, wherein the bl transistor is conducting electricity when the first bitline is discharged, and wherein the blb transistor is powered when the second bitline is discharged.

16. The method of claim 13, wherein the common output of the bl transistor and the blb transistor are connected across two or more columns in the memory array that are accessed together.

17. The method of claim 13, further comprising: selecting, by a multiplexor electrically coupled between a plurality of bitlines and the sense amplifier, the plurality of bitlines including the first bitline and the second bitline, a pair of bitlines of the plurality of bitlines; and outputting, by the multiplexor, the pair of bitlines to the sense amplifier.

18. The method of claim 13, further comprising: disabling, by a program clock transistor electrically coupled to the bl transistor and the blb transistor, the common output of the bl transistor and the blb transistor.

19. The method of claim 18, wherein a size of the program clock transistor determines a strength of the program clock transistor.

20. The method of claim 18, wherein a gate voltage of the program clock transistor determines a strength of the program clock transistor when it is conducting electricity during a read operation.

21. The method of claim 18, wherein the program clock transistor is configured to disable the common output of the bl transistor and the blb transistor based on enabling a subset of program clock transistors.

22. The method of claim 13, further comprising: selecting, by a multiplexor, an input from a program sense amplifier enable signal transistor or the common output of the bl transistor and the blb transistor.

23. The method of claim 13, further comprising: disabling, by a discharge transistor, the common output of the bl transistor and the blb transistor.

24. The memory system of claim 13, wherein the memory array comprises a plurality of columns, including the column, wherein less than all of the plurality of columns are associated with a plurality of pairs of bl transistors and blb transistors, including the bl transistor and the blb transistor.

25. A memory system comprising: first means for receiving a first electrical signal from a first bitline of a column of a memory array based on the first bitline being discharged, the first means for receiving electrically coupled to the first bitline; second means for receiving a second electrical signal from a second bitline of the column of the memory array based on the second bitline being discharged, the second means for receiving electrically coupled to the second bitline, wherein an output of the first means for receiving and an output of the second means for receiving are electrically coupled together as a common output; and means for amplifying a voltage swing configured to receive the common output of the first means for receiving and the second means for receiving as a sense amplifier enable signal, the means for amplifying the voltage swing electrically coupled to the first bitline and the second bitline, wherein the means for amplifying the voltage swing is further configured to measure a voltage differential across the first bitline and the second bitline based on reception of the sense amplifier enable signal.

26. The memory system of claim 25, further comprising: means for selecting and outputting a pair of bitlines of a plurality of bitlines of the memory array, the plurality of bitlines including the first bitline and the second bitline, the means for selecting coupled between the plurality of bitlines and the means for amplifying the voltage swing.

27. The memory system of claim 25, further comprising: means for disabling the common output of the first means for receiving and the second means for receiving, the means for disabling electrically coupled to the first means for receiving and the second means for receiving.

28. The memory system of claim 25, further comprising: means for selecting an input from a program sense amplifier enable signal transistor or the common output of the first means for receiving and the second means for receiving.