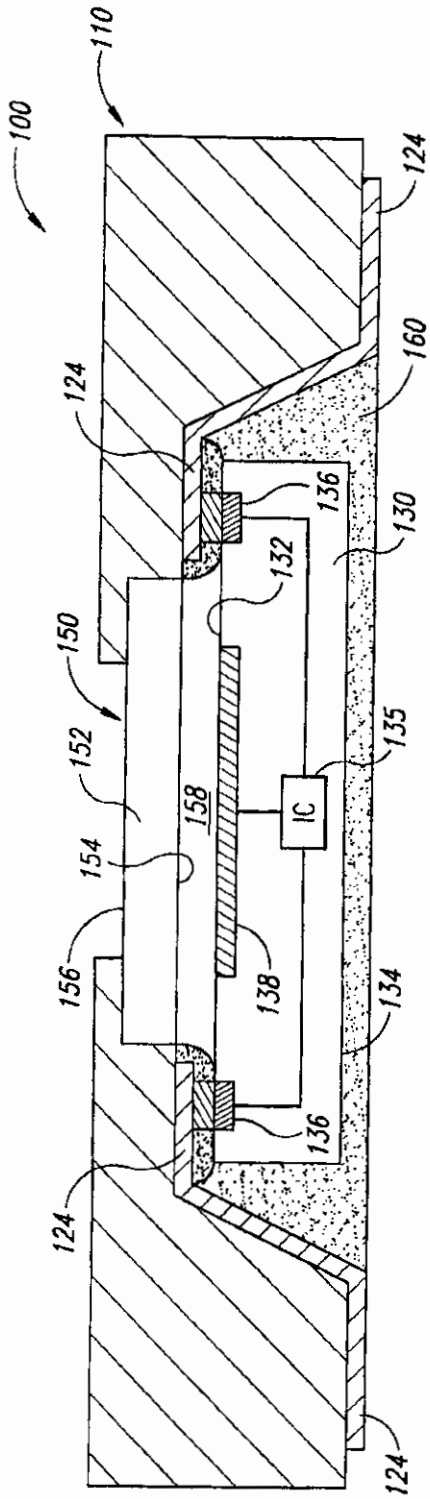

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Fig. 1

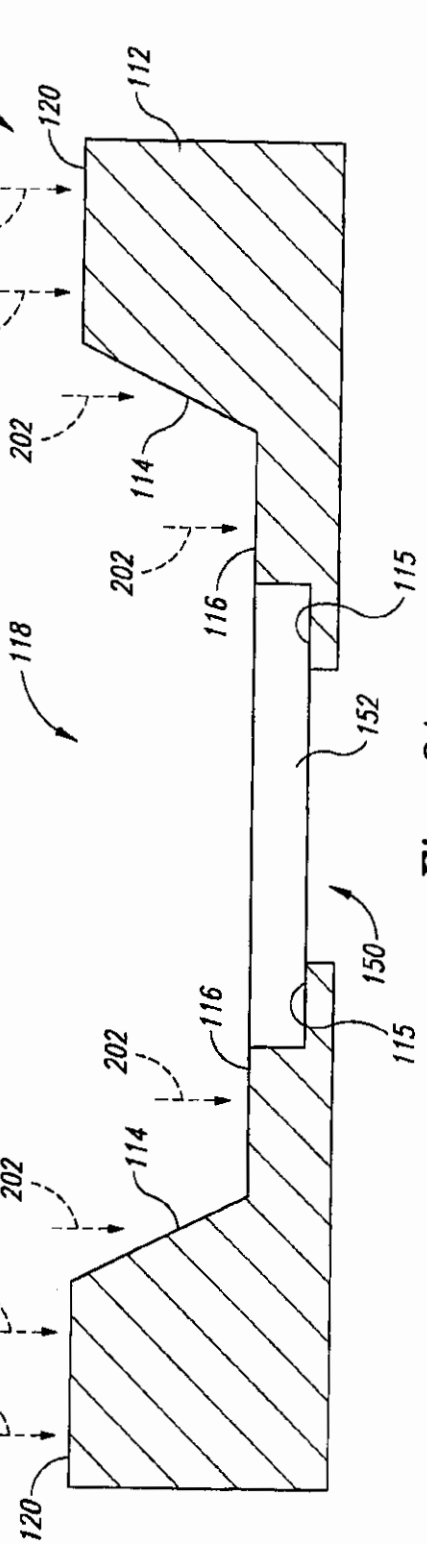

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Fig. 2A

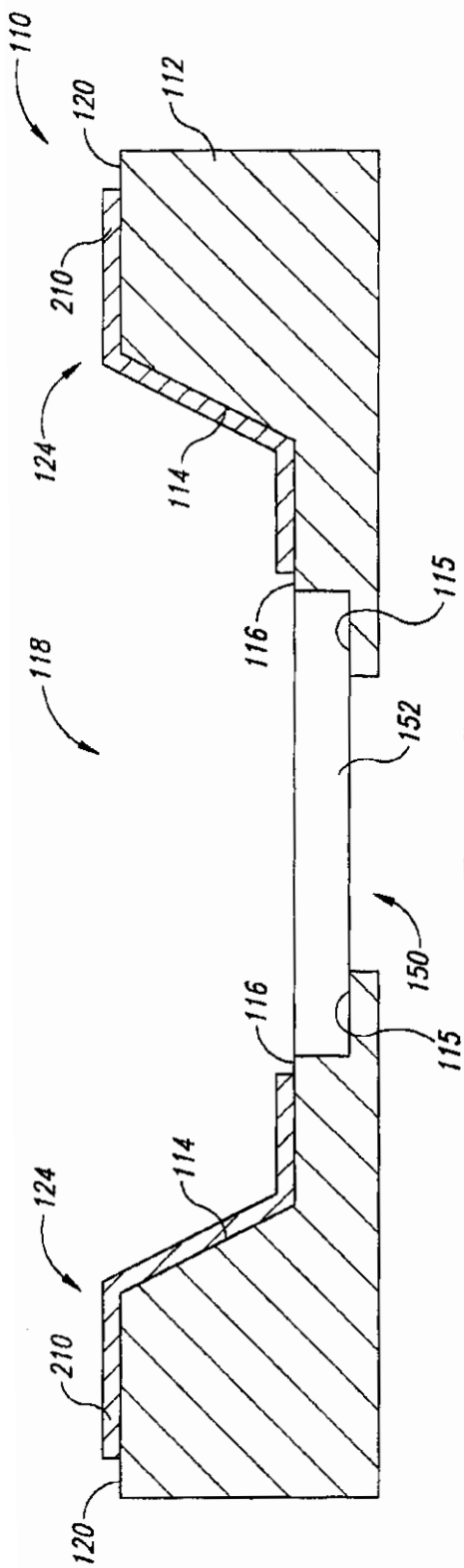

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Fig. 2B

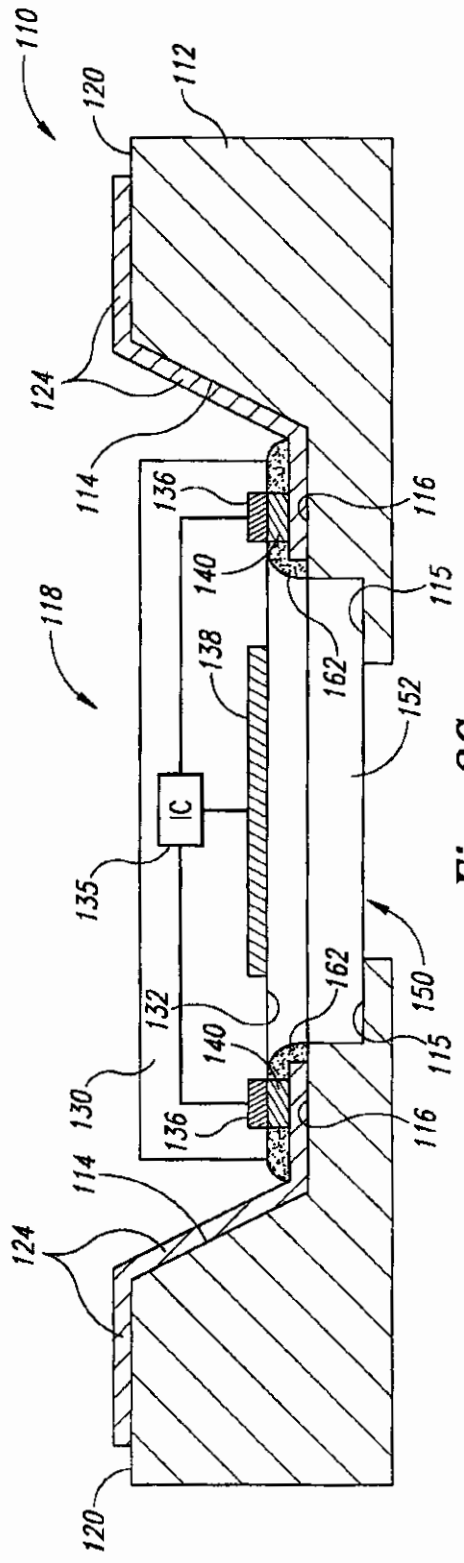

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Fig. 2C

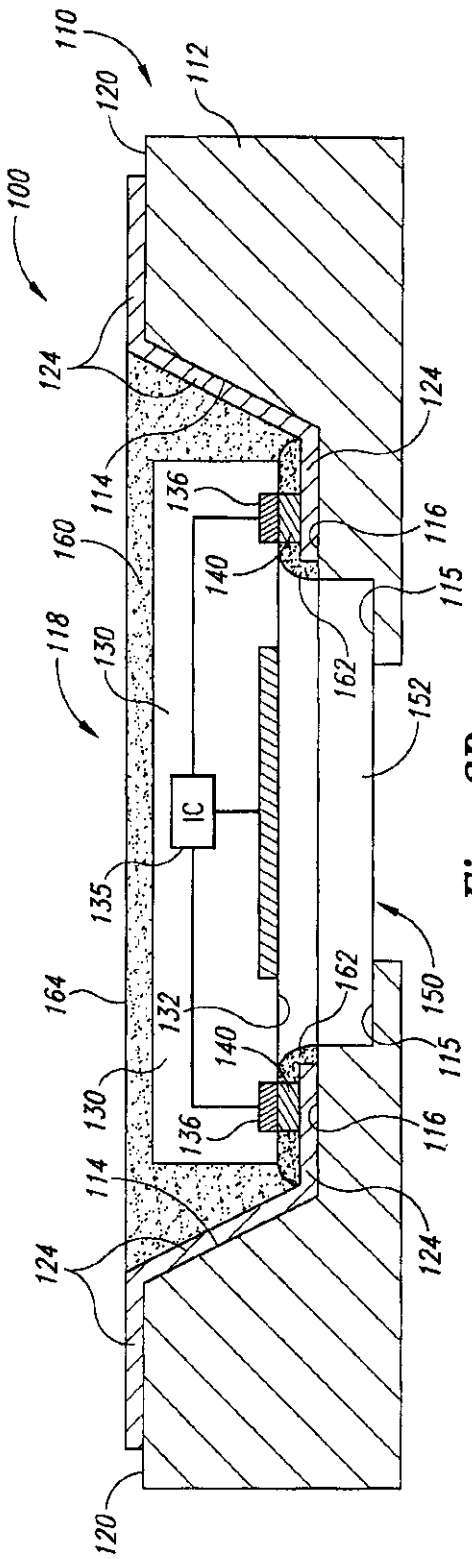

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Fig. 2D

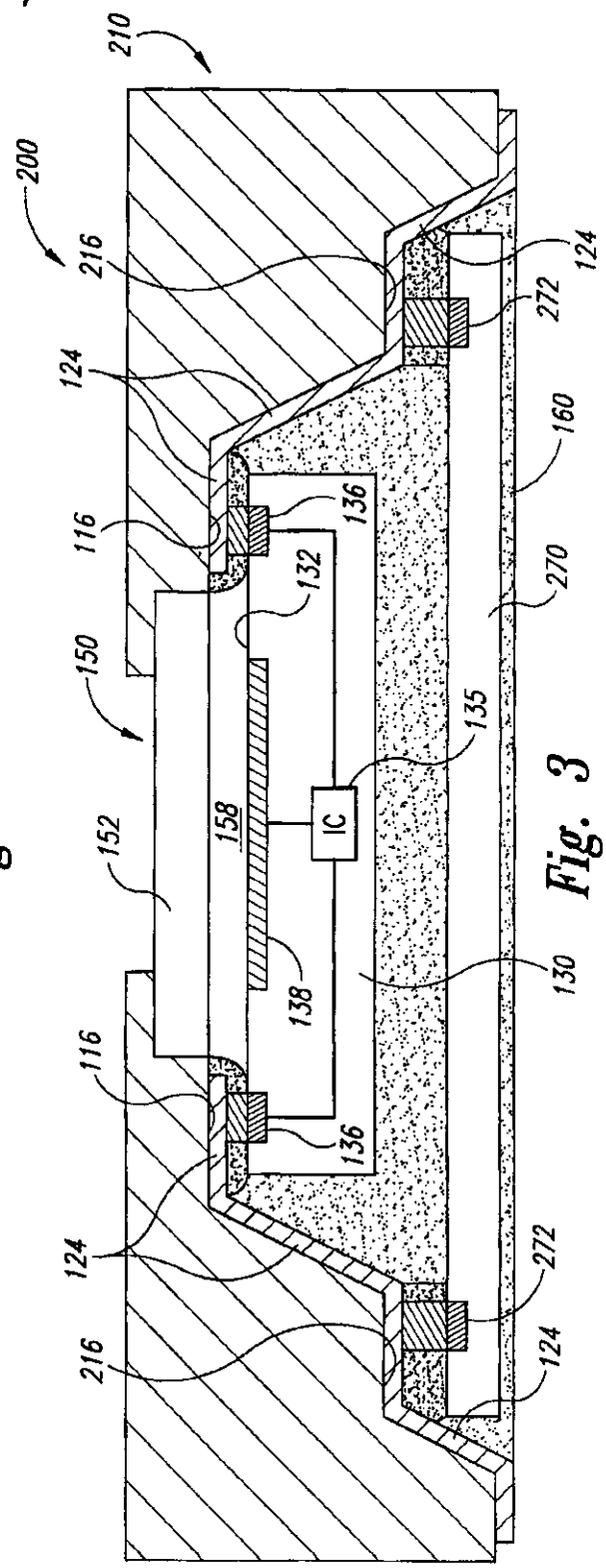

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Fig. 3

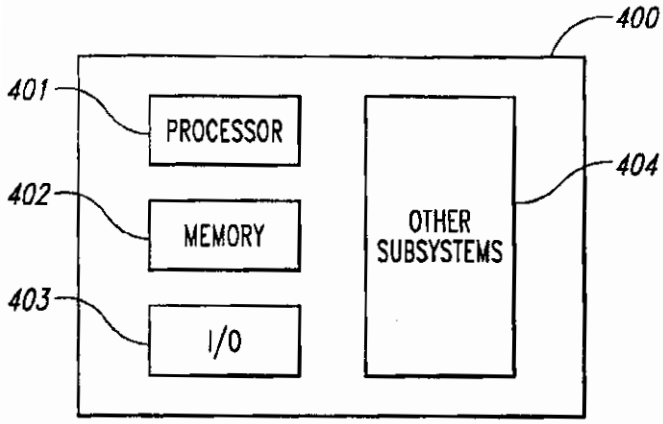

400
401
PROCESSOR
402
MEMORY
403
I/O
OTHER SUBSYSTEMS
404

Fig. 4

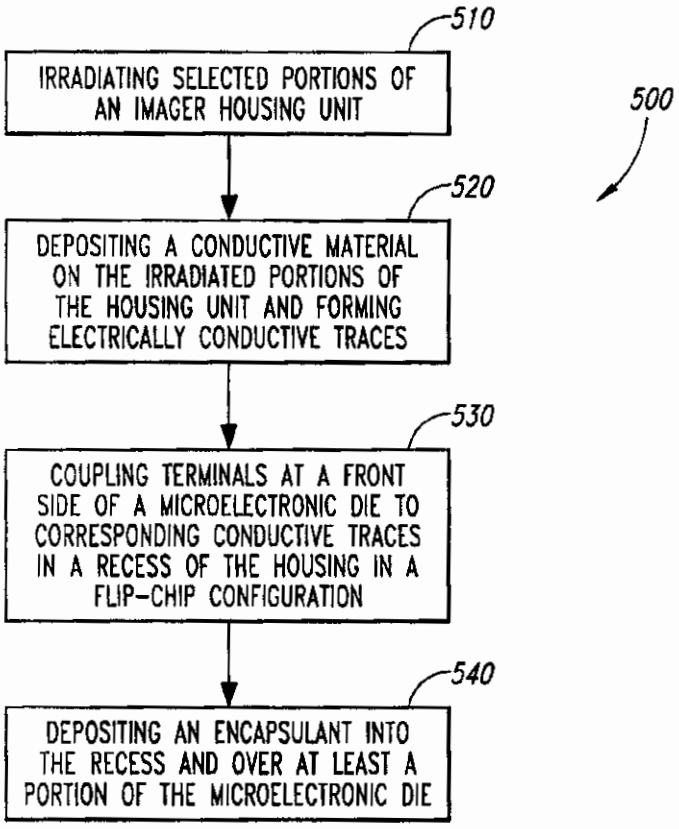

510
IRRADIATING SELECTED PORTIONS OF AN IMAGER HOUSING UNIT
500
520
DEPOSITING A CONDUCTIVE MATERIAL ON THE IRRADIATED PORTIONS OF THE HOUSING UNIT AND FORMING ELECTRICALLY CONDUCTIVE TRACES
530
COUPLING TERMINALS AT A FRONT SIDE OF A MICROELECTRONIC DIE TO CORRESPONDING CONDUCTIVE TRACES IN A RECESS OF THE HOUSING IN A FLIP-CHIP CONFIGURATION
540
DEPOSITING AN ENCAPSULANT INTO THE RECESS AND OVER AT LEAST A PORTION OF THE MICROELECTRONIC DIE

Fig. 5