FIG. 1

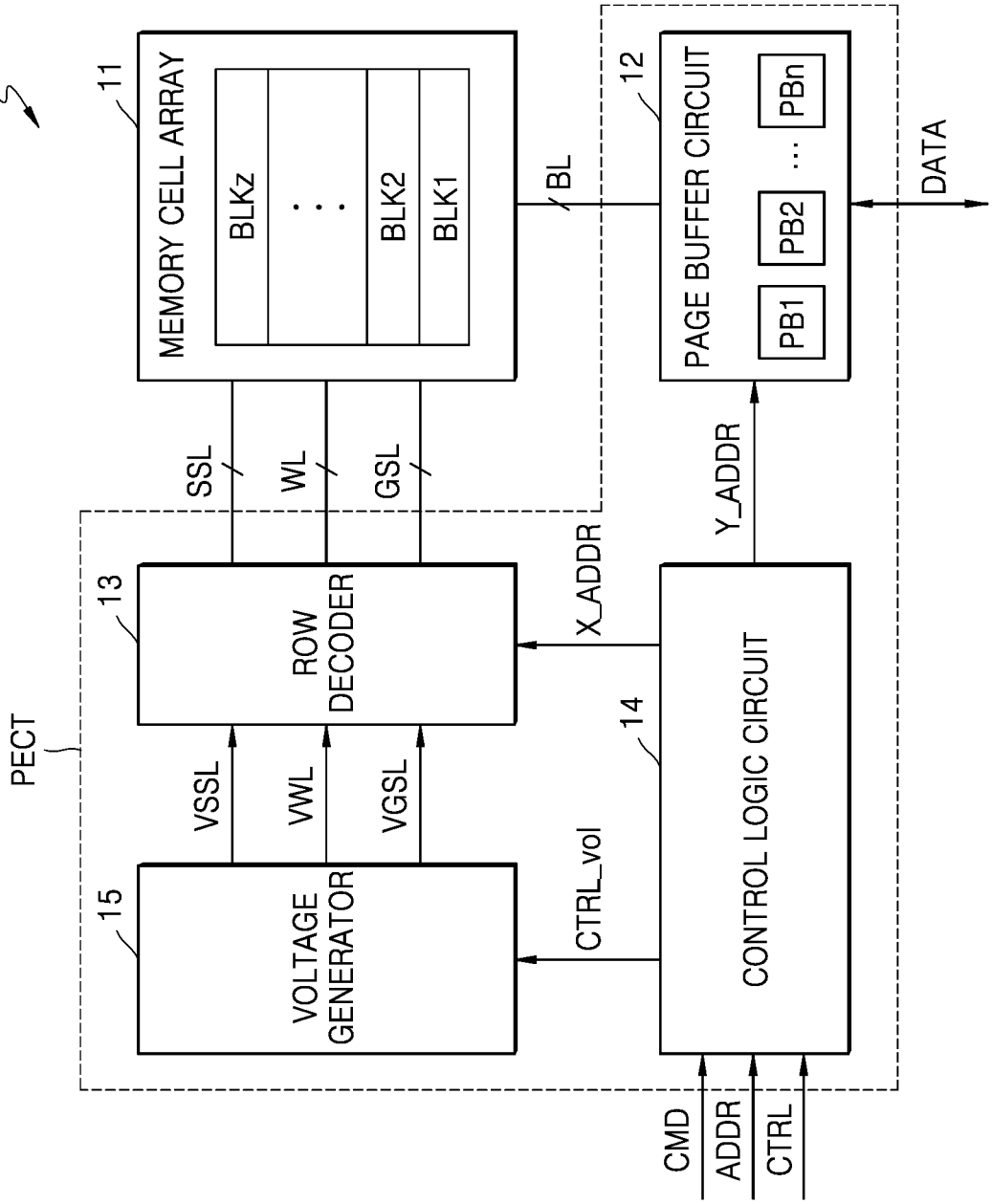

10
11
MEMORY CELL ARRAY
BLKz
BLK2
BLK1
12
PAGE BUFFER CIRCUIT
PB1
PB2
PBn
DATA
BL
SSL
WL
GSL
Y_ADDR
X_ADDR
13
ROW DECODER
PECT
VSSL
VWL
VGSL
14
CONTROL LOGIC CIRCUIT
15
VOLTAGE GENERATOR
CTRL_vol
CMD
ADDR
CTRL

FIG. 2

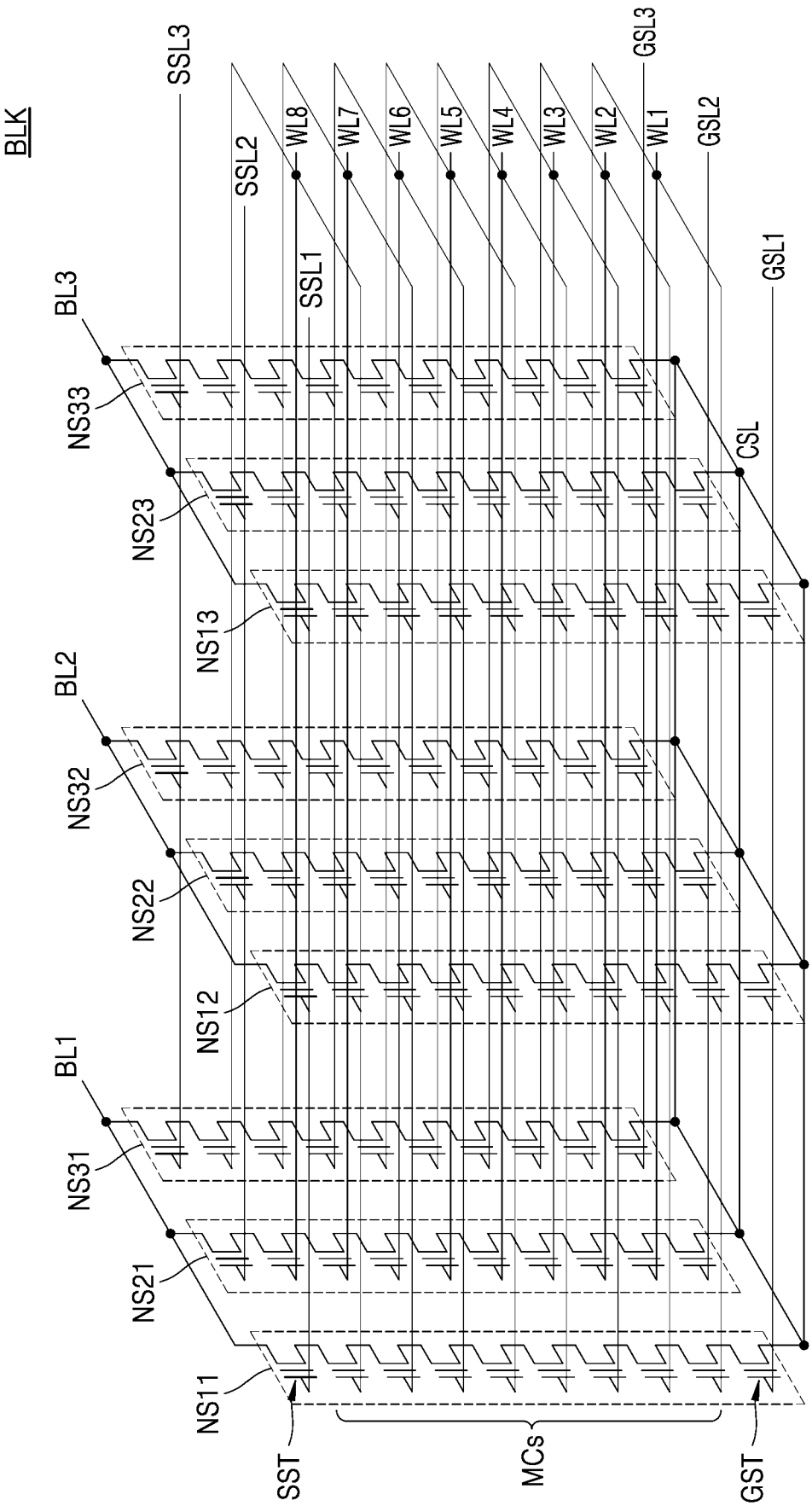

BLK
SSL3
SSL2
SSL1
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL3
GSL2
GSL1
CSL
BL3
BL2
BL1
NS33
NS23
NS13
NS32
NS22
NS12
NS31
NS21
NS11
SST
MCs
GST

FIG. 3A

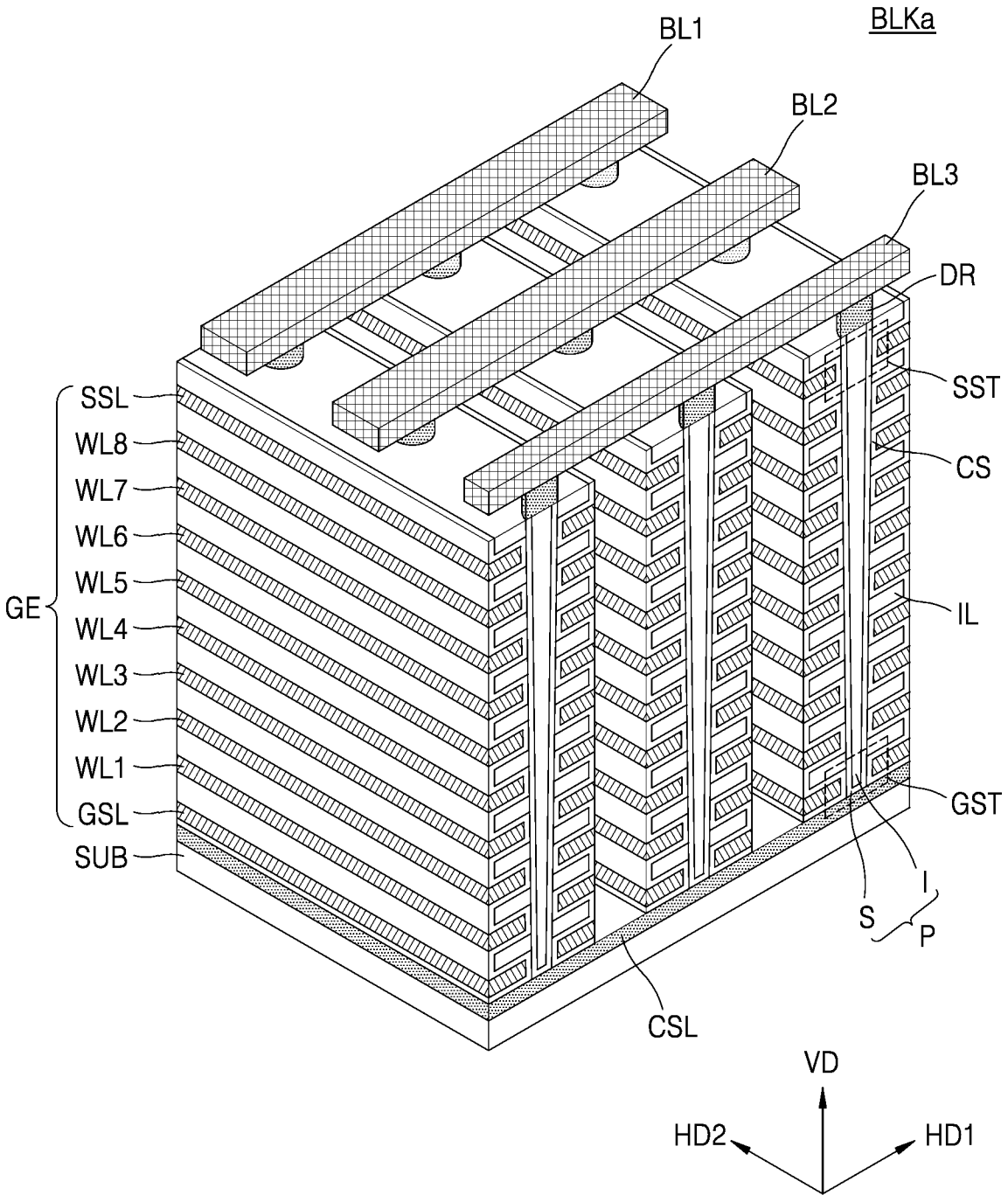

BLKa
BL1
BL2
BL3
DR
SST
CS
IL
GST
I
S
P
CSL
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
VD
HD2
HD1

FIG. 3B

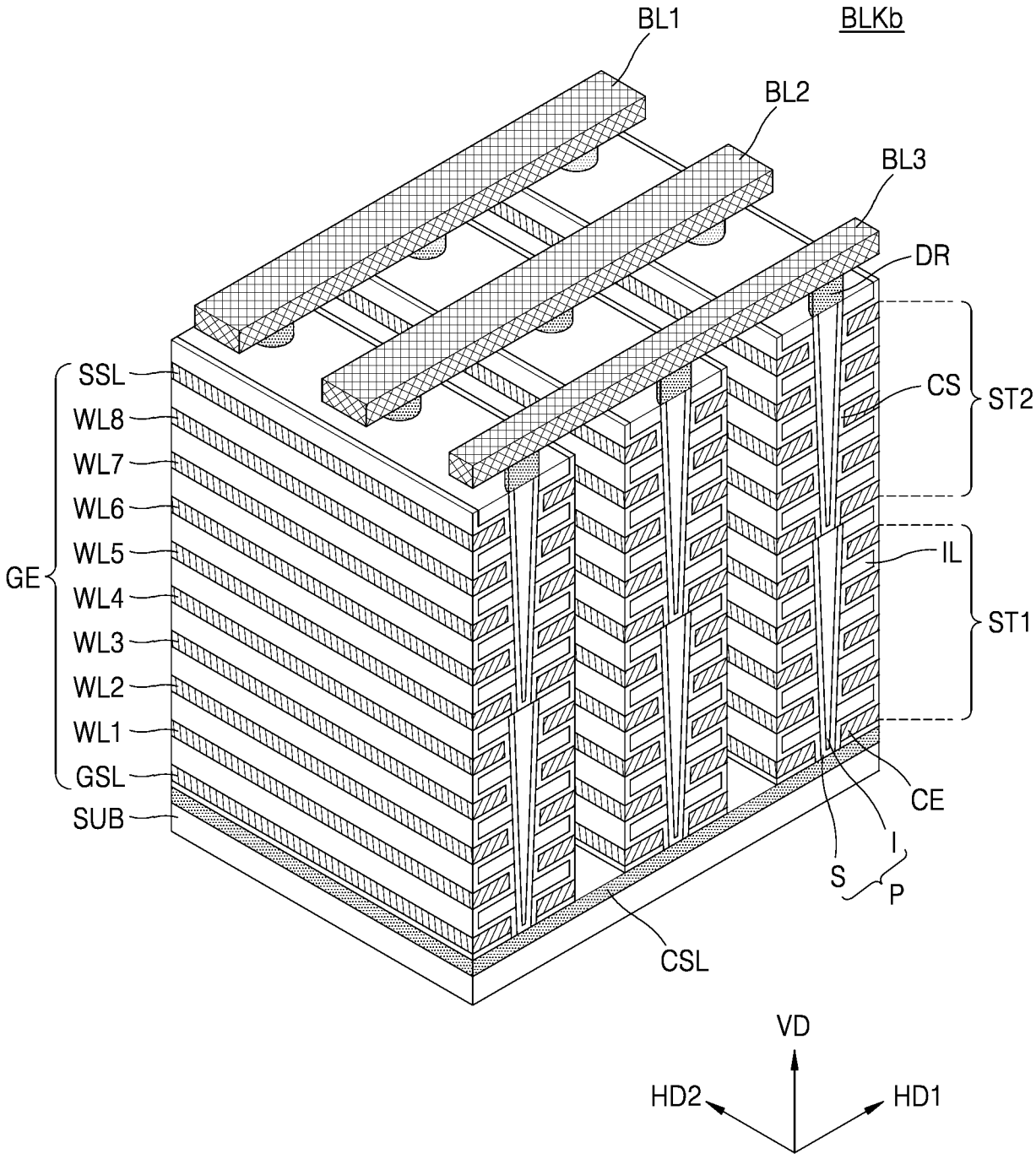

BL1
BLKb
BL2
BL3
DR
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
CS
ST2
IL
ST1
CE
I
S
P
CSL
VD
HD2
HD1

FIG. 4

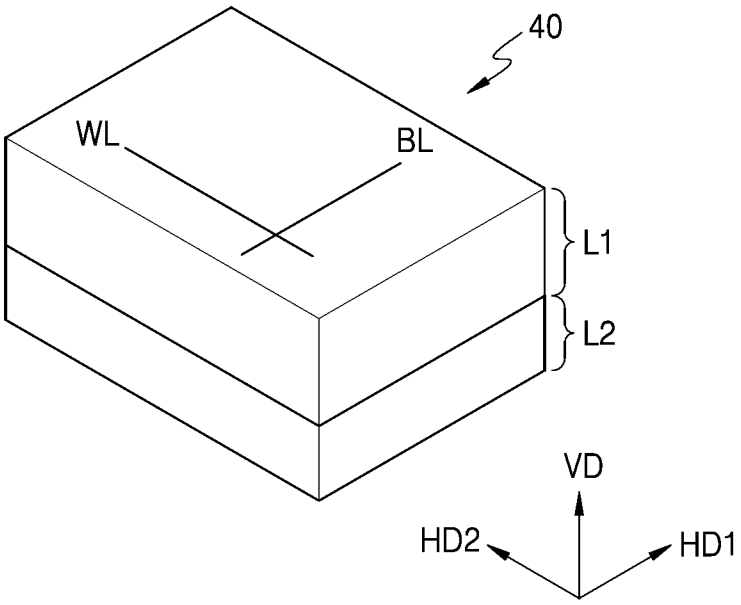


FIG. 5

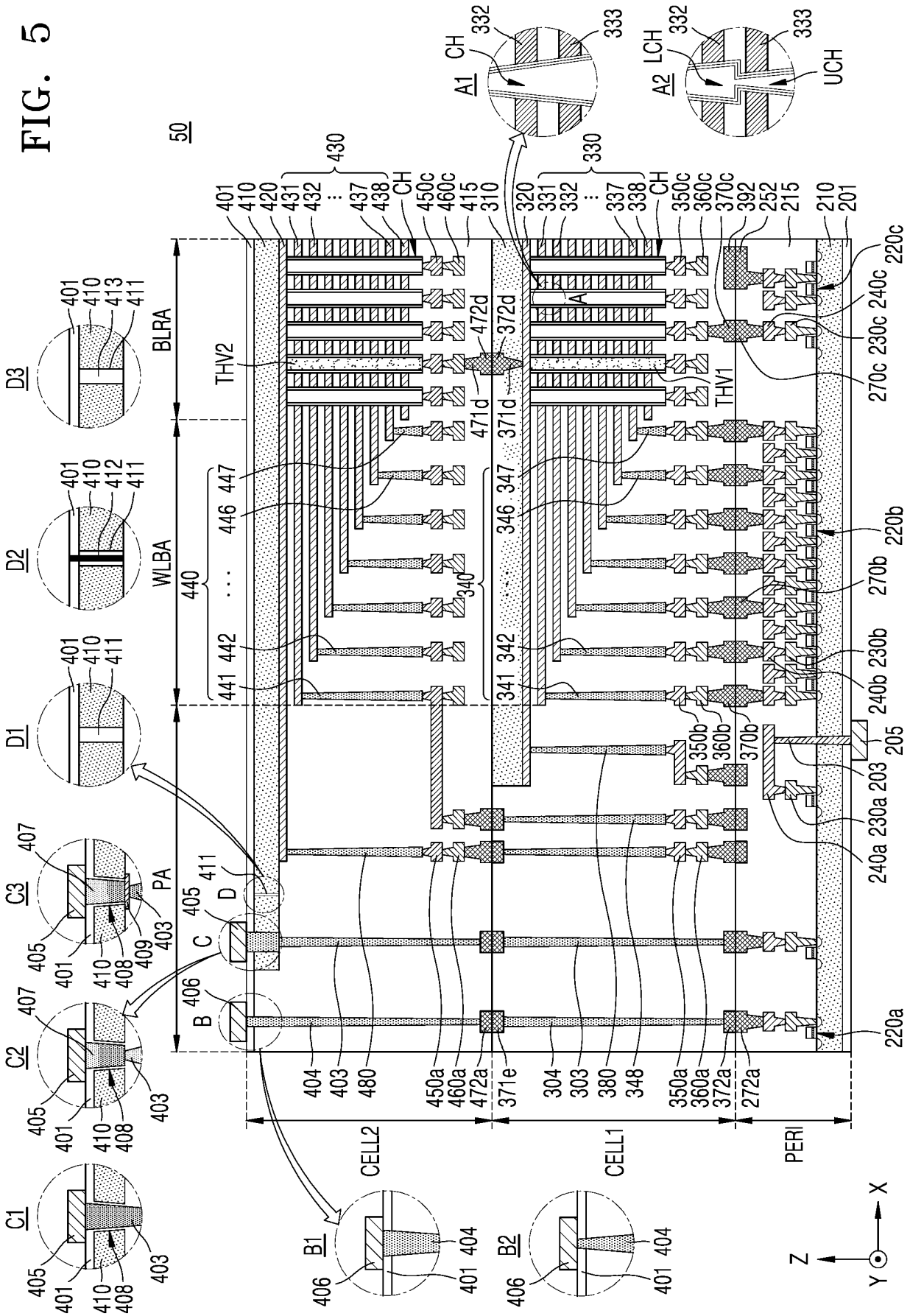

50
A1
A2
CH
LCH
UCH
332
333
430
330
401
410
420
431
432
437
438
450c
460c
415
310
320
331
337
350c
360c
370c
392
252
215
210
201
BLRA
WLBA
THV2
THV1
440
441
442
446
447
340
341
342
346
347
471d
472d
371d
372d
220c
240c
230c
270c
220b
270b
230b
240b
205
203
220a
240a
230a
D1
D2
D3
C1
C2
C3
B1
B2
A
B
C
D
PA
CELL2
CELL1
PERI
404
403
480
450a
460a
472a
371e
304
303
380
348
350a
360a
372a
272a
X
Y
Z

FIG. 6

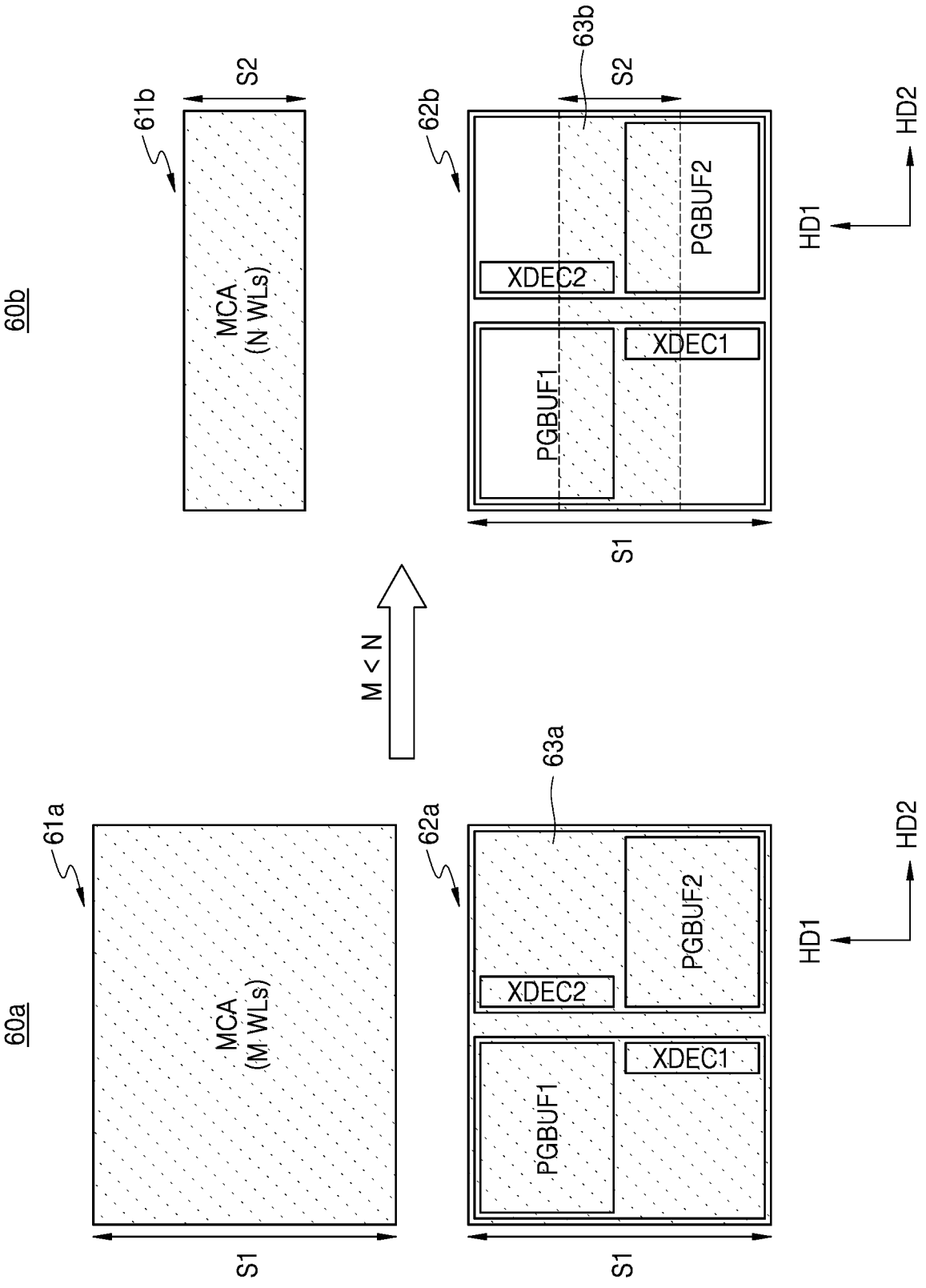

60b
61b
S2
MCA
(N WLs)
62b
63b
S2
PGBUF2
XDEC2
XDEC1
PGBUF1
S1
HD1
HD2
M < N
60a
61a
MCA
(M WLs)
62a
63a
PGBUF2
XDEC2
XDEC1
PGBUF1
S1
HD1
HD2

FIG. 7A

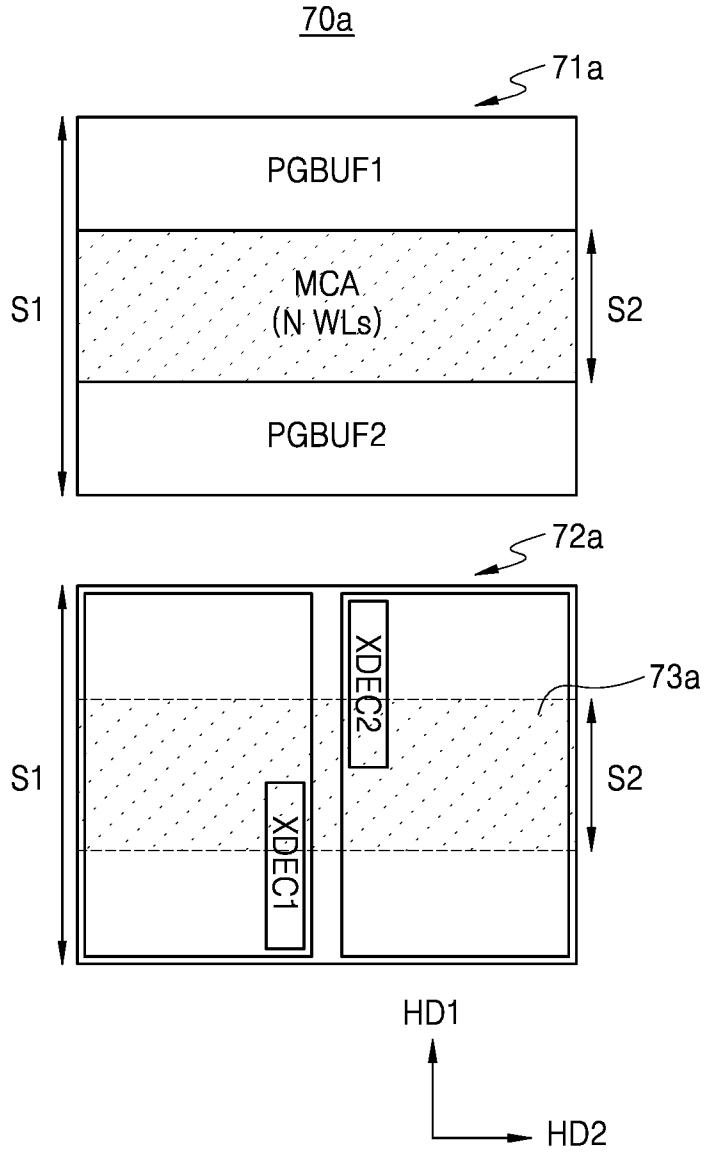

70a
71a
PGBUF1
MCA
(N WLs)
PGBUF2
S1
S2
72a
XDEC2
73a
XDEC1
S1
S2
HD1
HD2

FIG. 7B

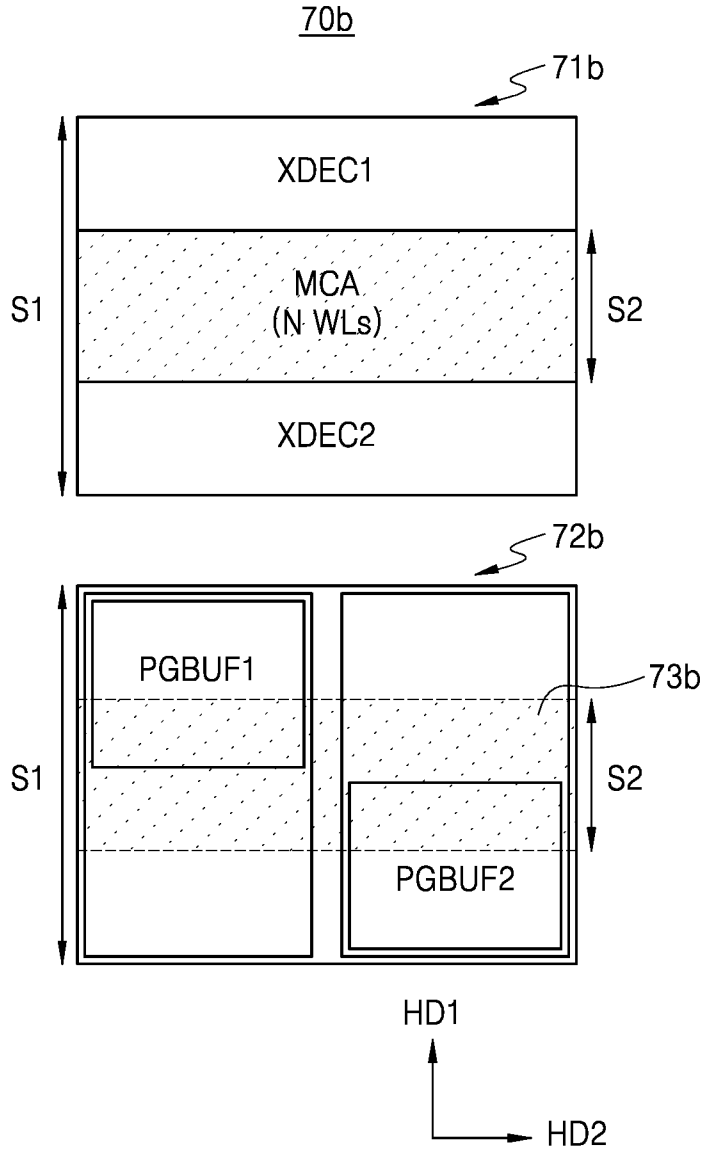

70b
71b
XDEC1
MCA
(N WLs)
XDEC2
S1
S2
72b
PGBUF1
PGBUF2
73b
S1
S2
HD1
HD2

FIG. 8

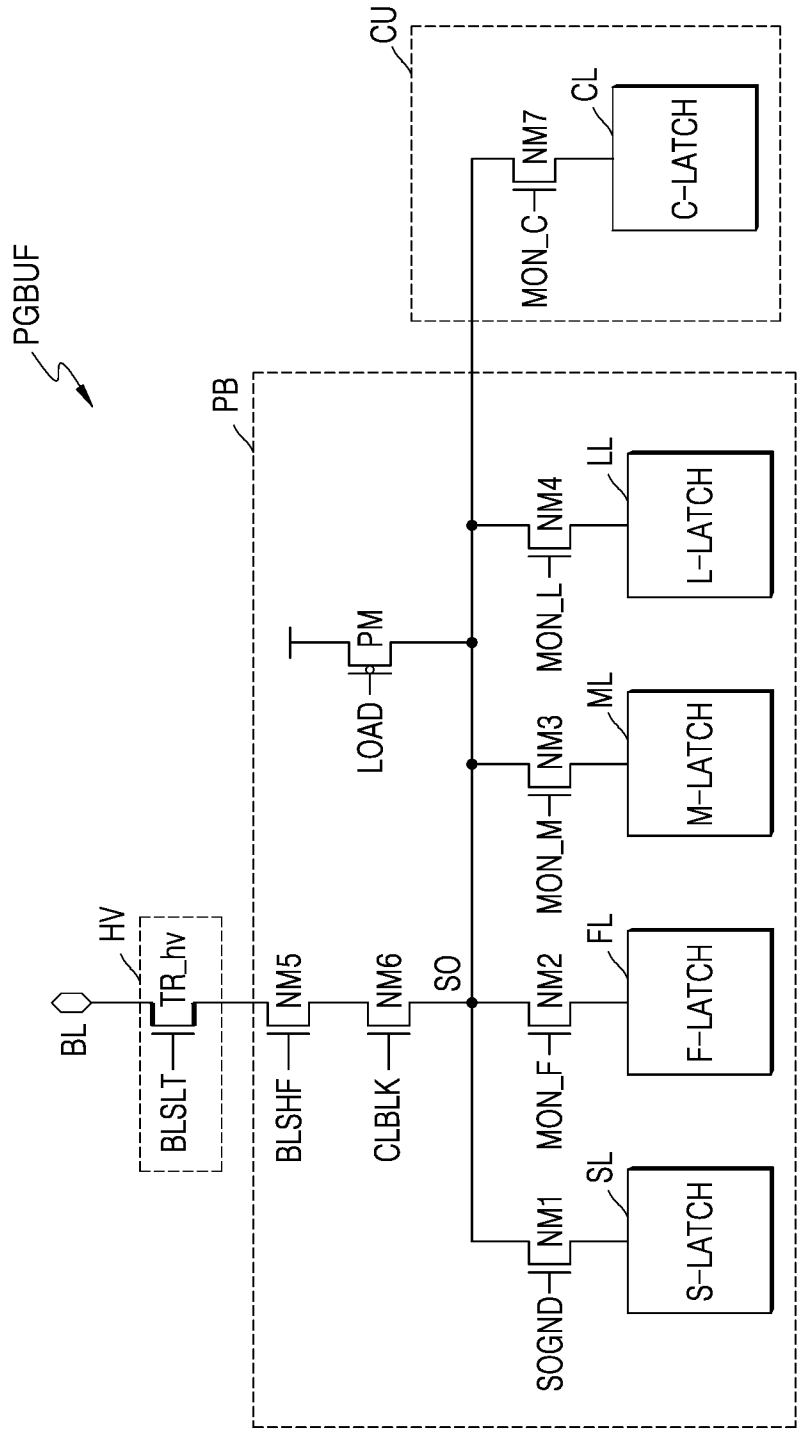

PGBUF
PB
CU
BL
HV
TR_hv
BLSLT
BLSHF
NM5
CLBLK
NM6
SO
LOAD
PM
SOGND
NM1
MON_F
NM2
MON_M
NM3
MON_L
NM4
MON_C
NM7
SL
FL
ML
LL
CL
S-LATCH
F-LATCH
M-LATCH
L-LATCH
C-LATCH

FIG. 9

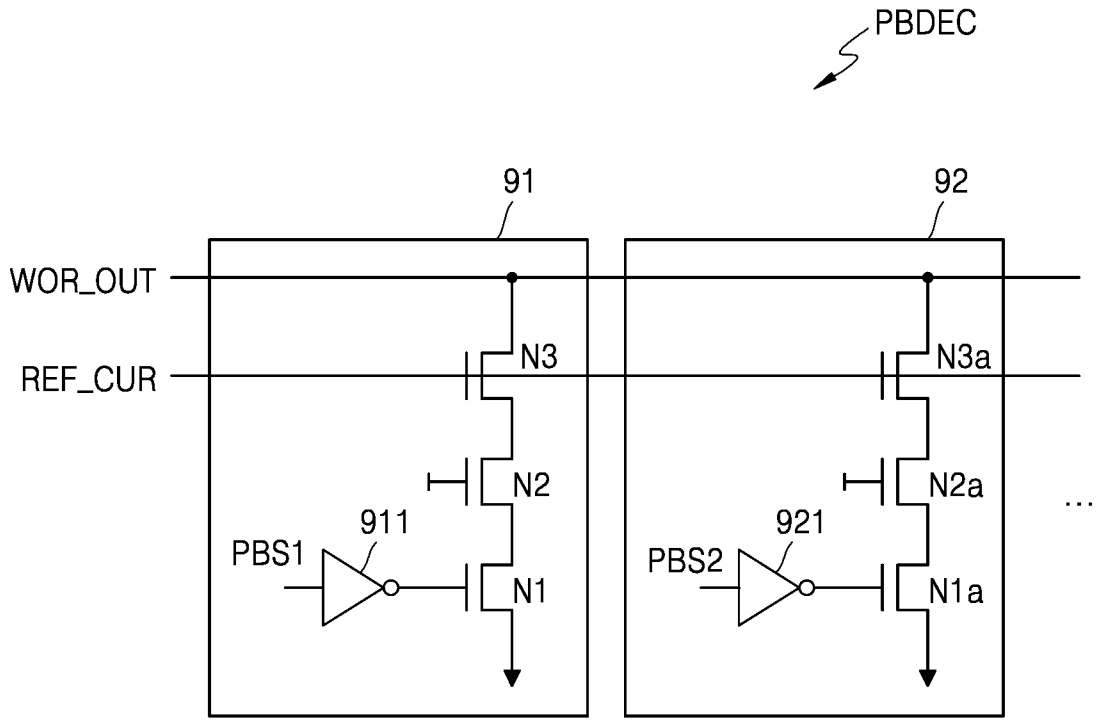

PBDEC
91
92
WOR_OUT
REF_CUR
N3
N3a
N2
N2a
911
921
PBS1
PBS2
N1
N1a
...

FIG. 10

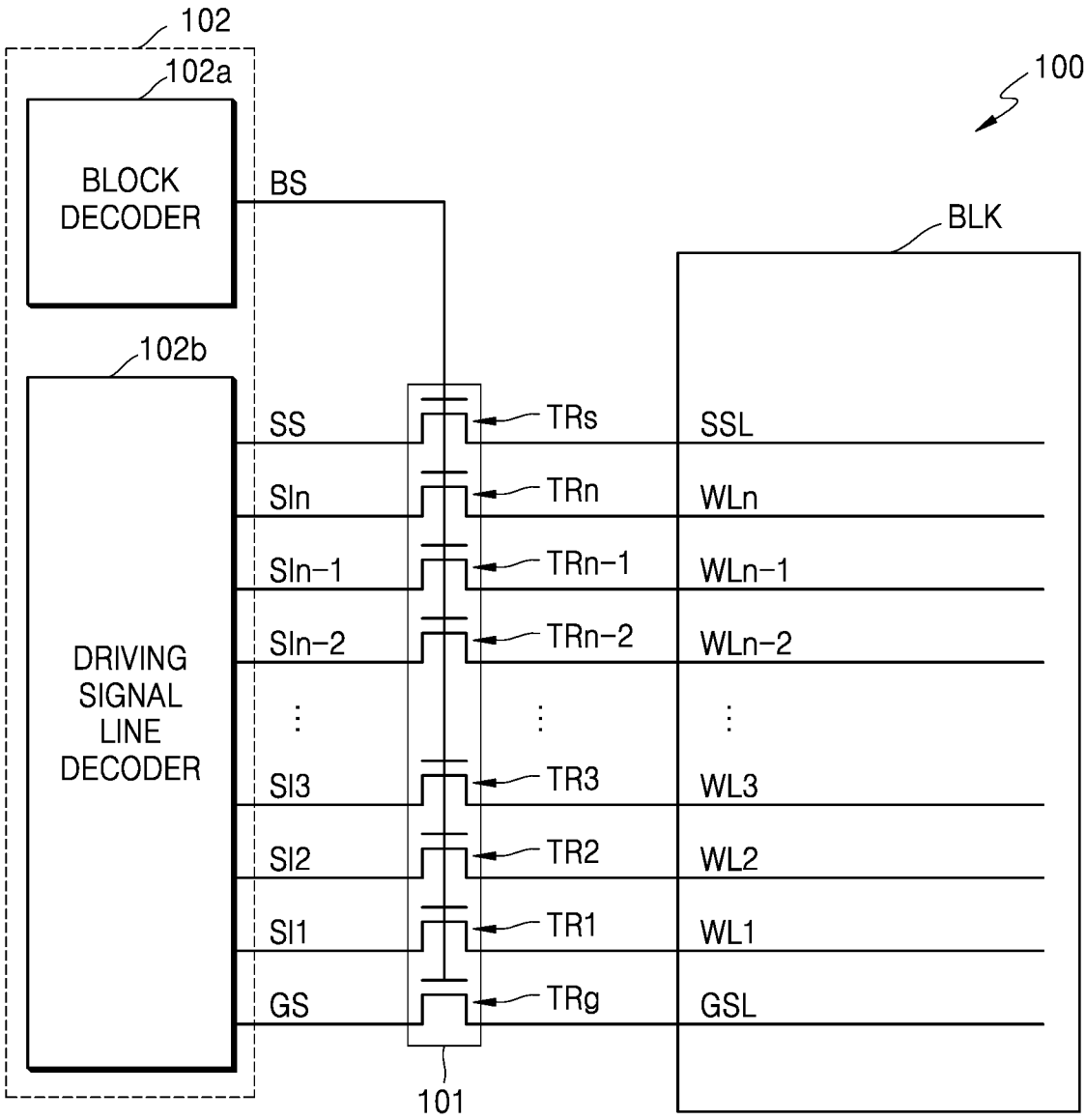

102
102a
BLOCK DECODER
102b
DRIVING SIGNAL LINE DECODER
100
BS
BLK
SS
SIn
SIn-1
SIn-2
SI3
SI2
SI1
GS
TRs
TRn
TRn-1
TRn-2
TR3
TR2
TR1
TRg
SSL
WLn
WLn-1
WLn-2
WL3
WL2
WL1
GSL
101

FIG. 11A

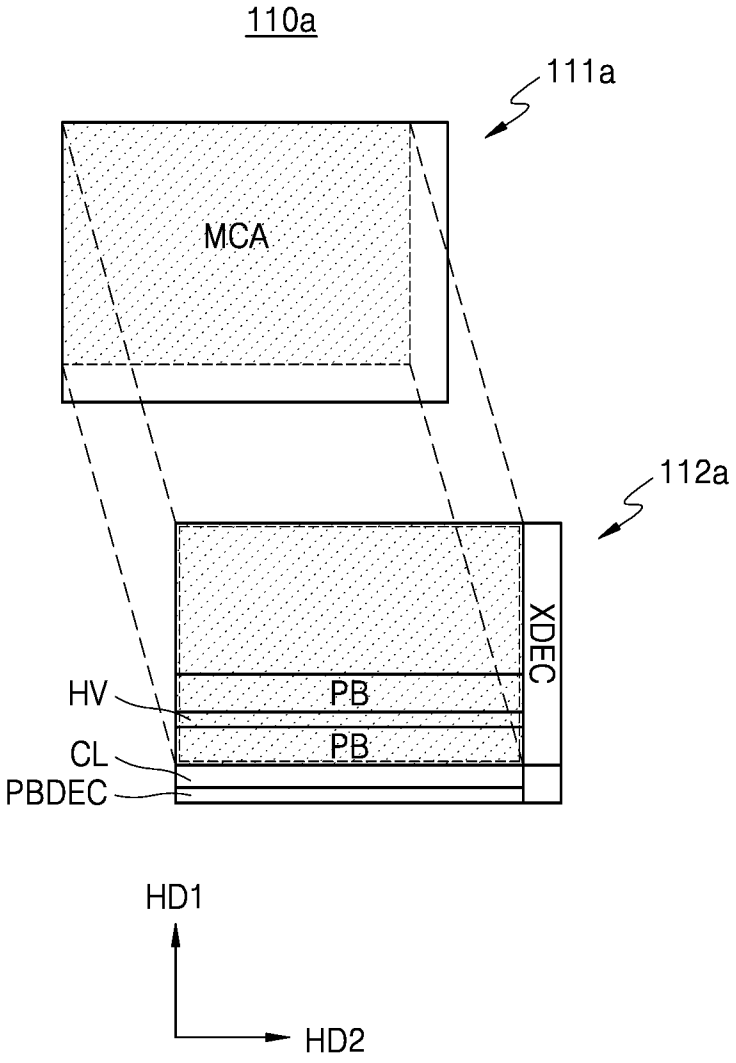


FIG. 11B

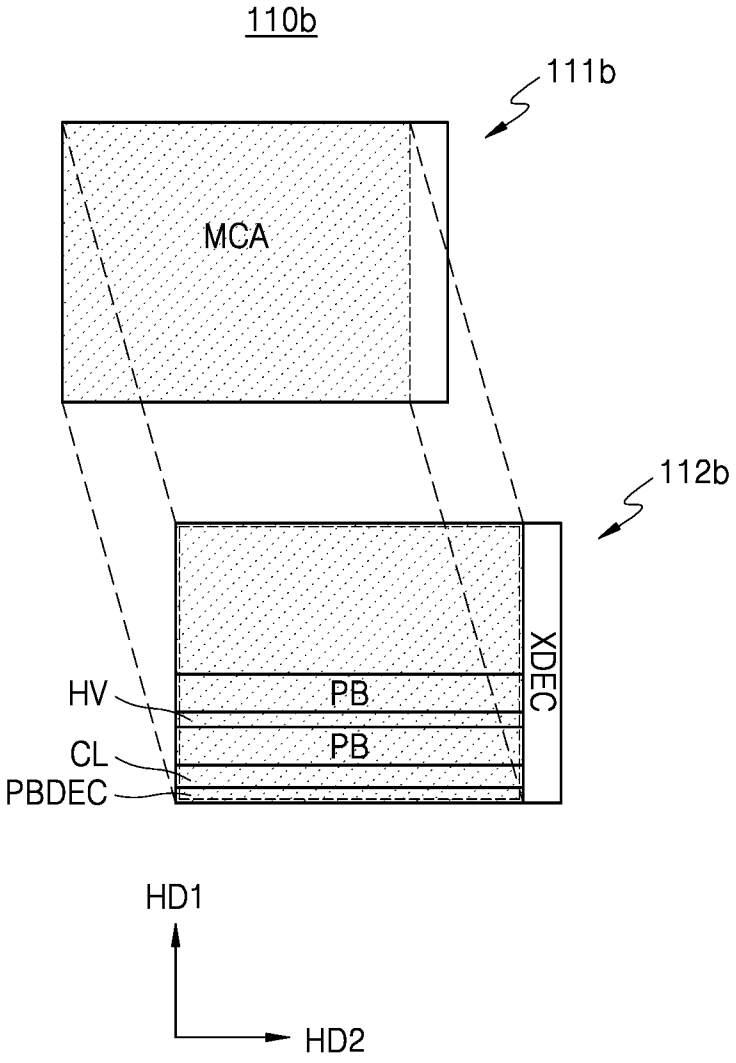


FIG. 11C

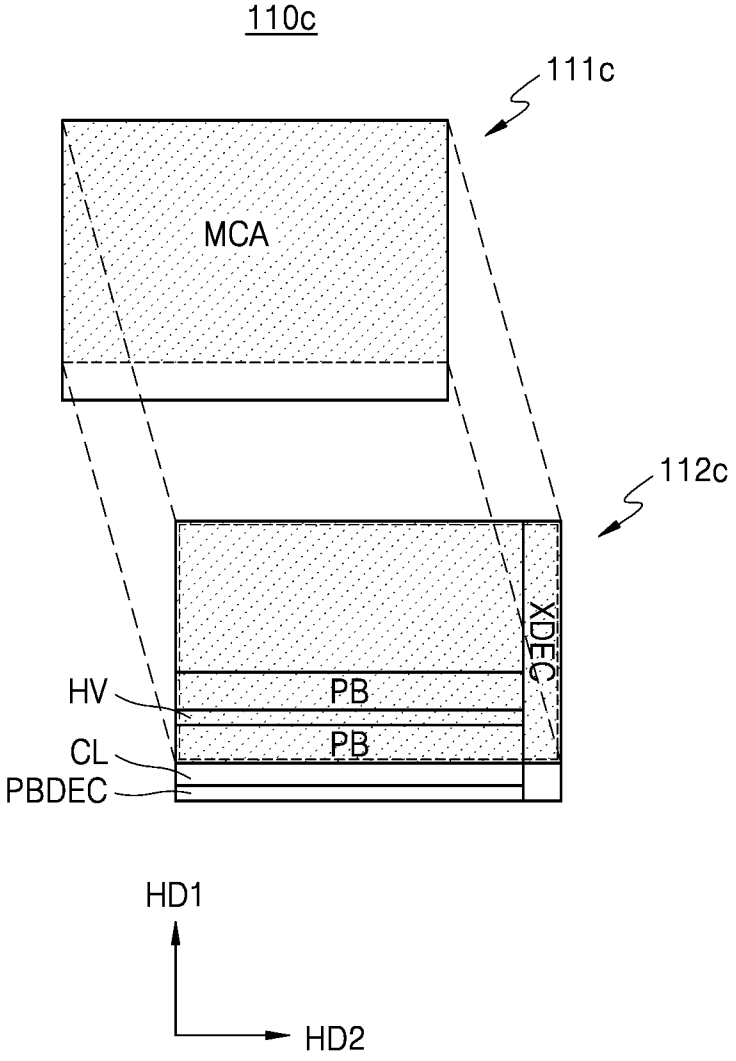


FIG. 11D

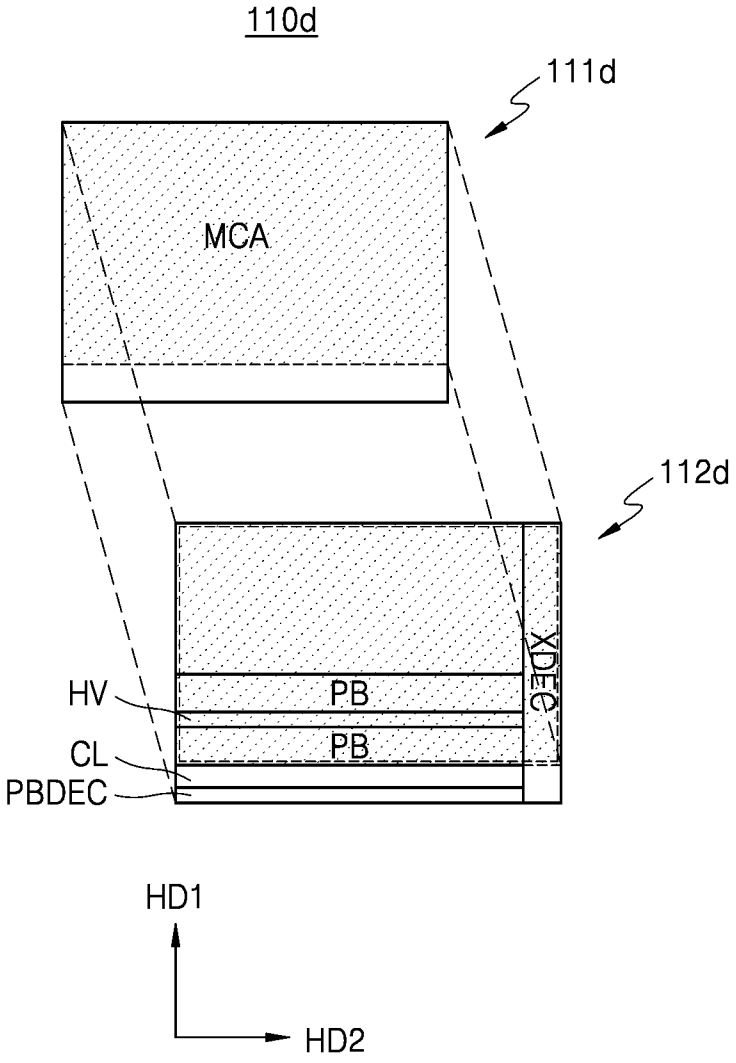


FIG. 12A

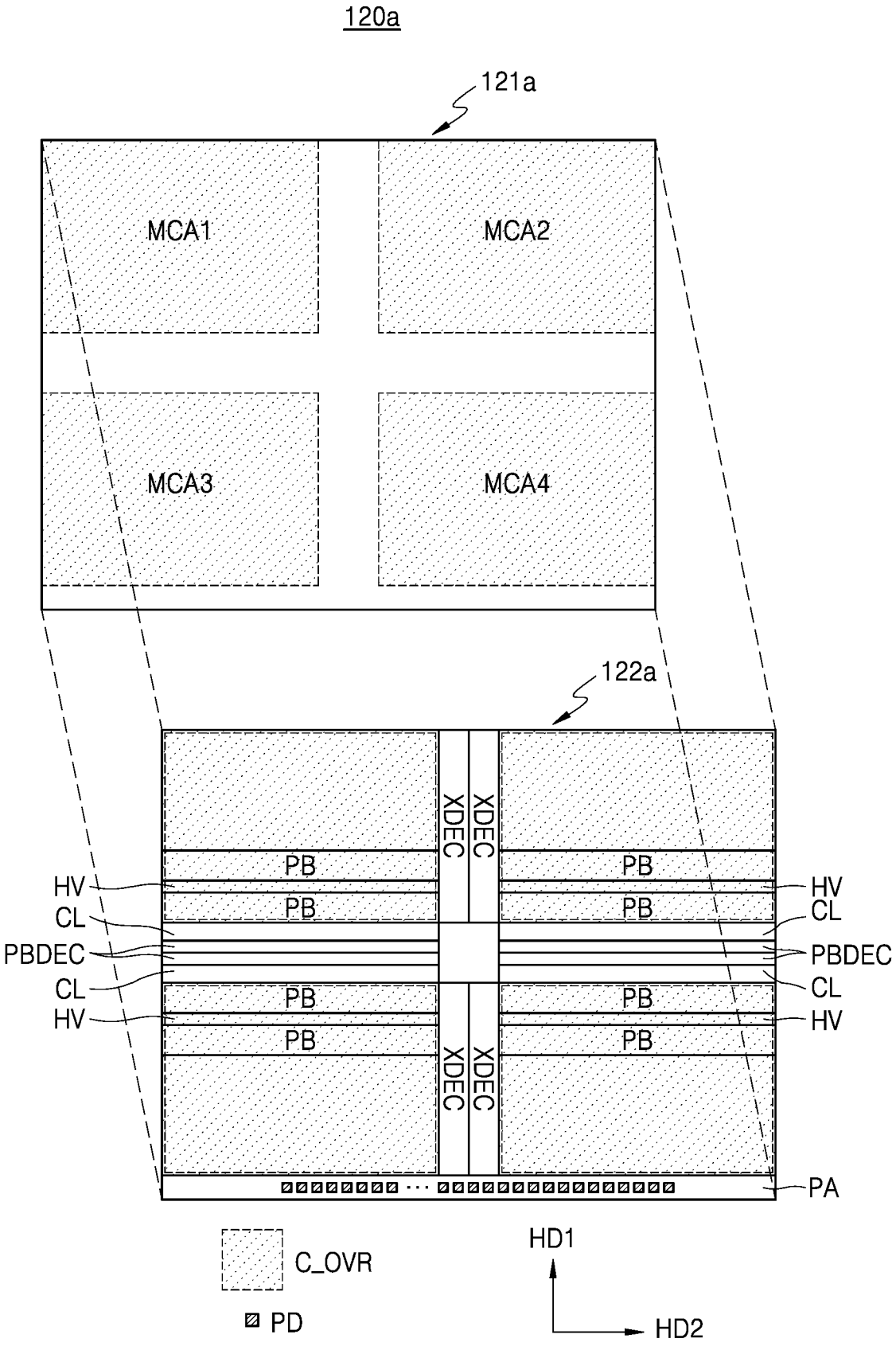

120a
121a
MCA1
MCA2
MCA3
MCA4
122a
XDEC
XDEC
PB
HV
CL
PBDEC
CL
HV
XDEC
XDEC
PA
C_OVR
PD
HD1
HD2

FIG. 12B

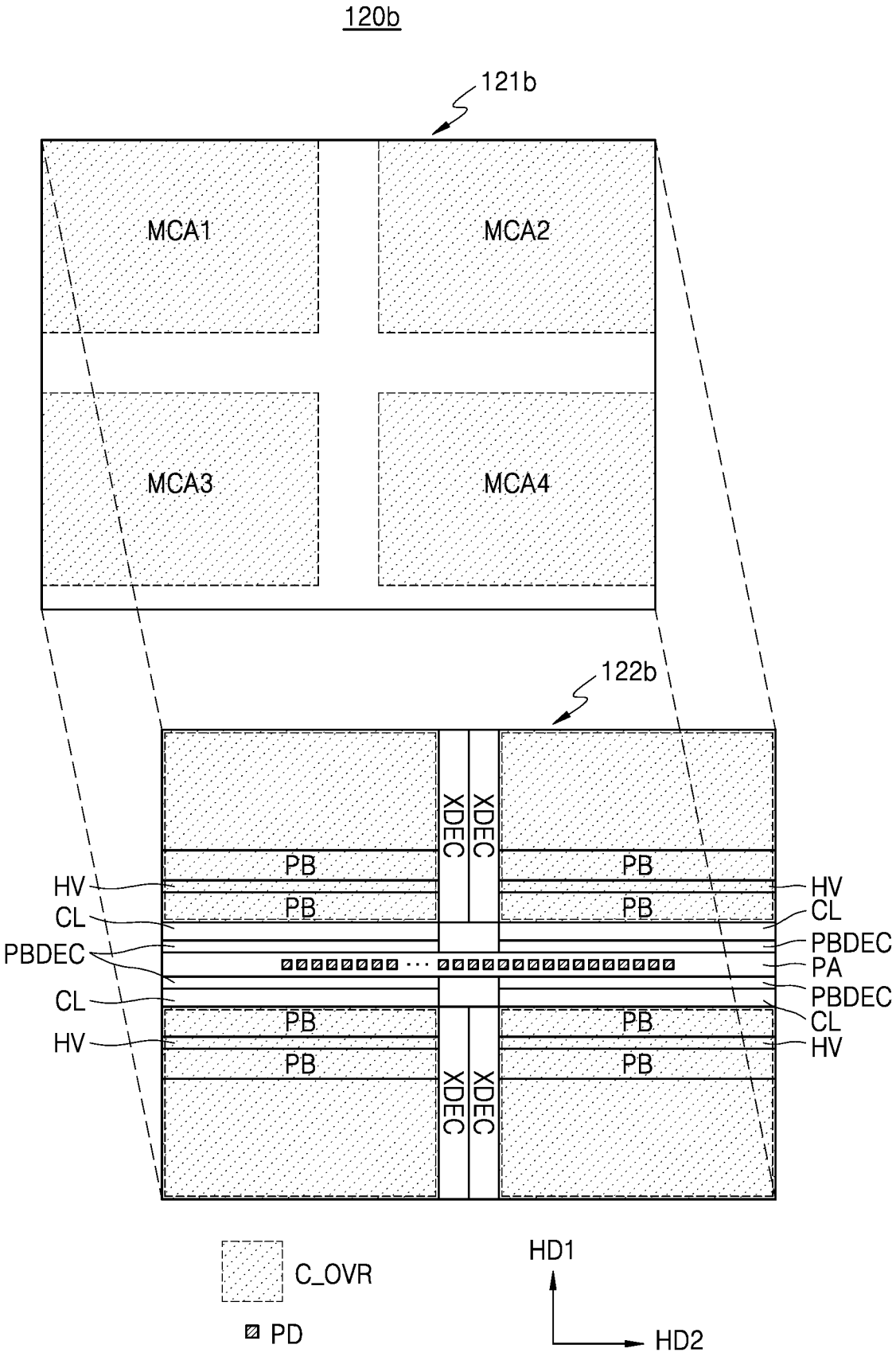

120b
121b
MCA1
MCA2
MCA3
MCA4
122b
XDEC
XDEC
PB
HV
CL
PBDEC
PA
C_OVR
PD
HD1
HD2

FIG. 12C

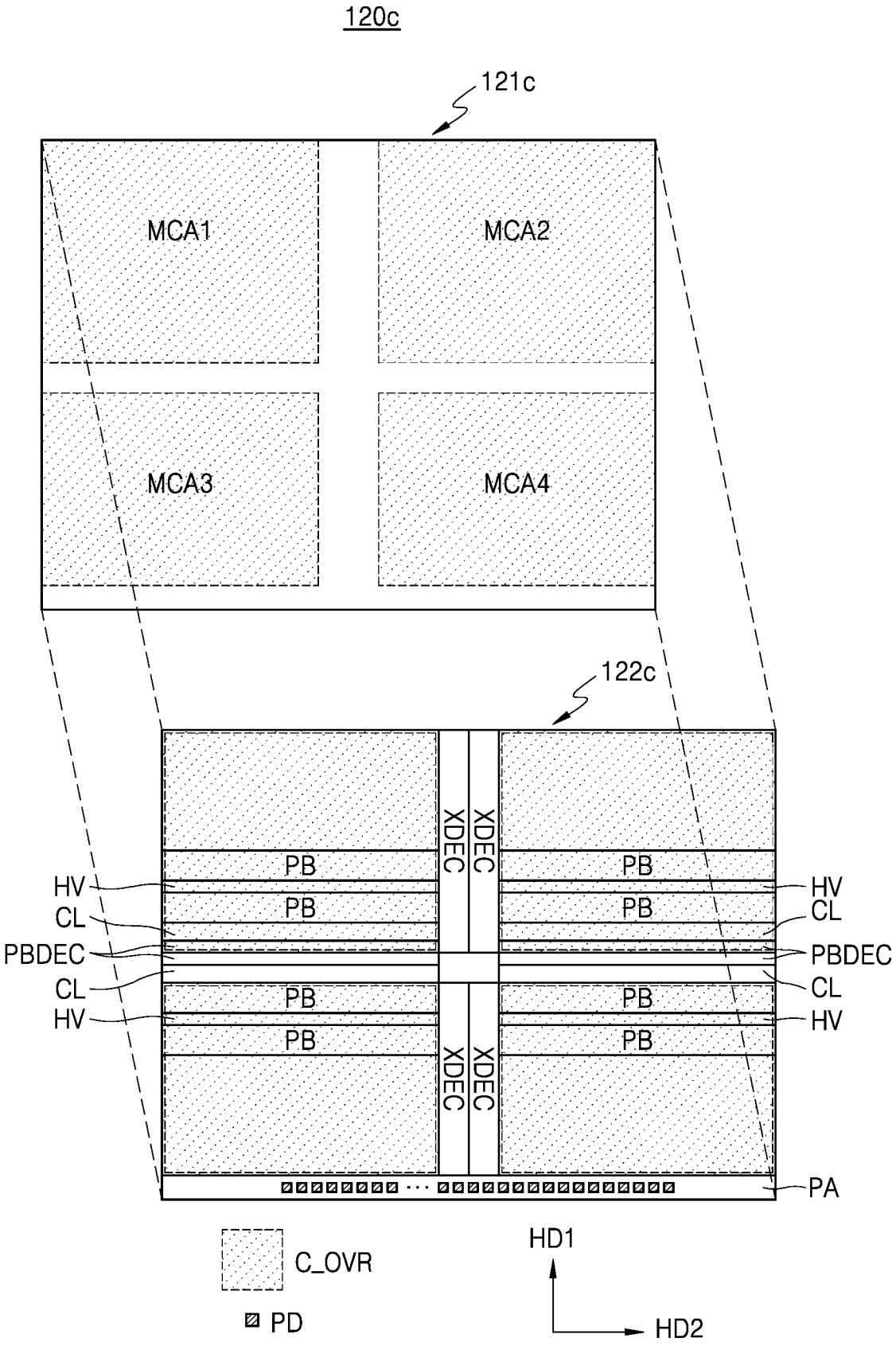

120c
121c
MCA1
MCA2
MCA3
MCA4
122c
XDEC
XDEC
PB
HV
CL
PBDEC
CL
HV
PA
C_OVR
PD
HD1
HD2

FIG. 12D

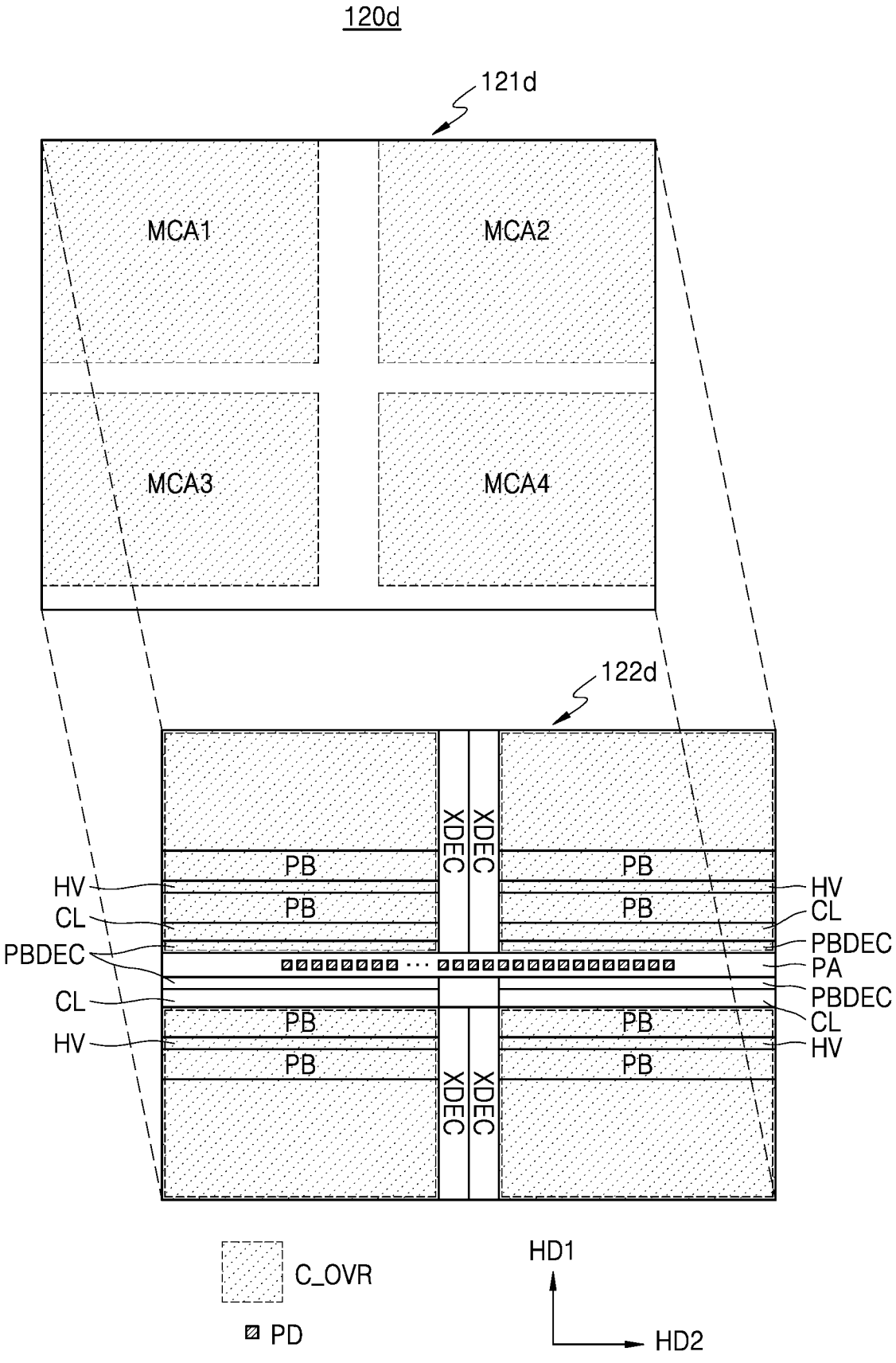

120d
121d
MCA1
MCA2
MCA3
MCA4
122d
XDEC
XDEC
PB
HV
CL
PBDEC
PA
C_OVR
PD
HD1
HD2

FIG. 12E

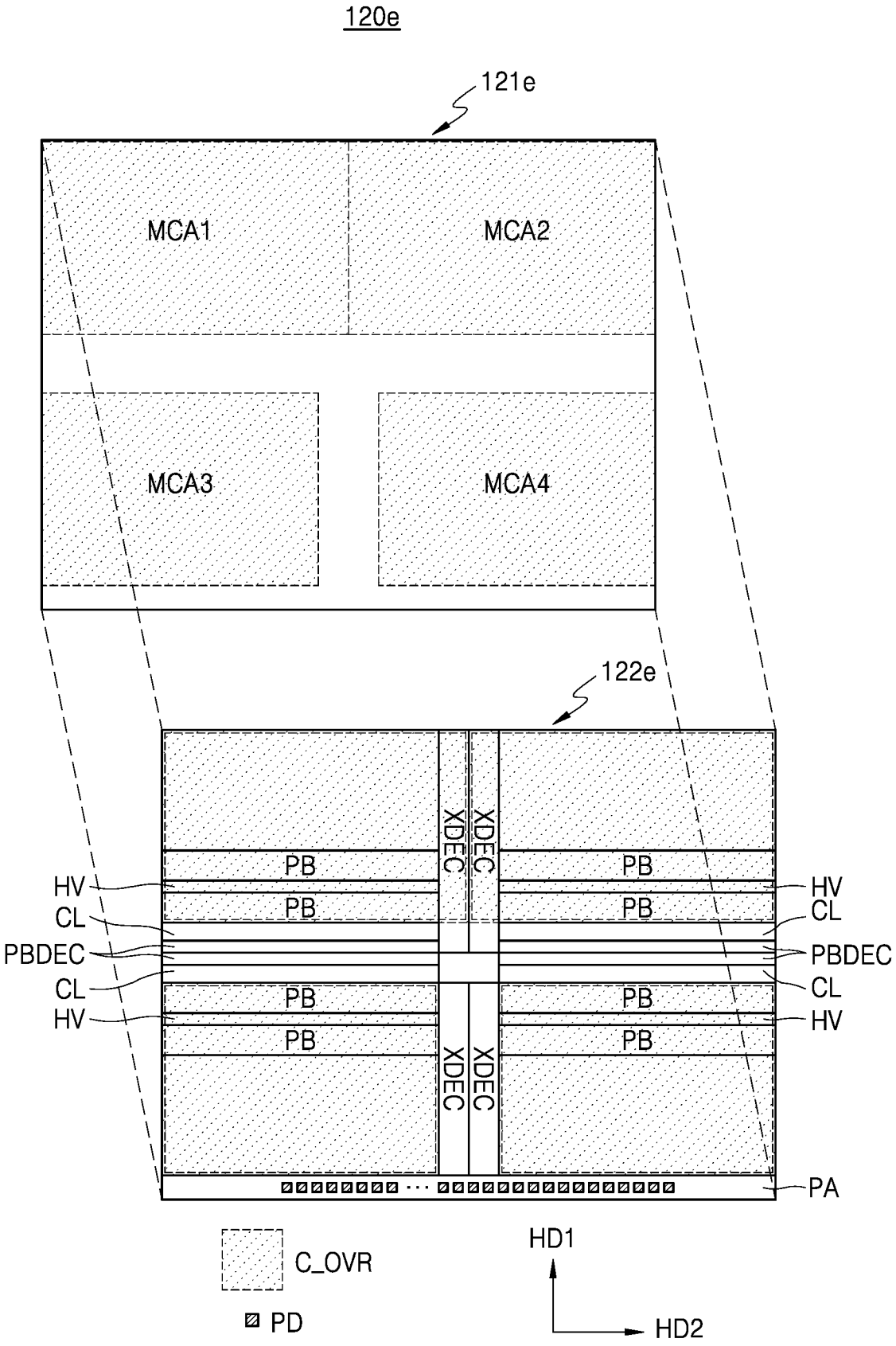

120e
121e
MCA1
MCA2
MCA3
MCA4
122e
XDEC
XDEC
PB
HV
CL
PBDEC
CL
HV
PA
C_OVR
PD
HD1
HD2

FIG. 12F

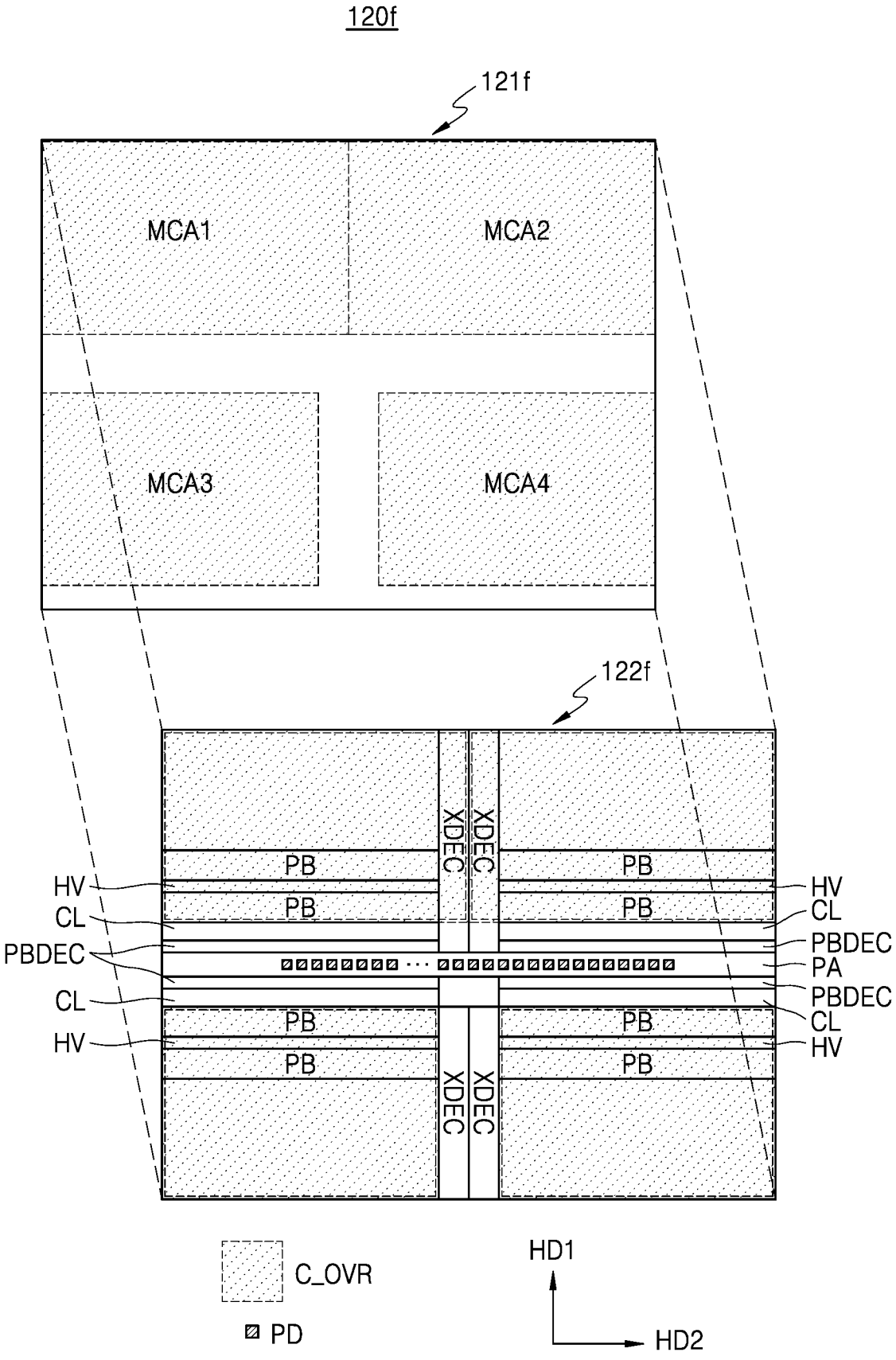

120f
121f
MCA1
MCA2
MCA3
MCA4
122f
XDEC
XDEC
PB
HV
CL
PBDEC
PA
C_OVR
PD
HD1
HD2

FIG. 13A

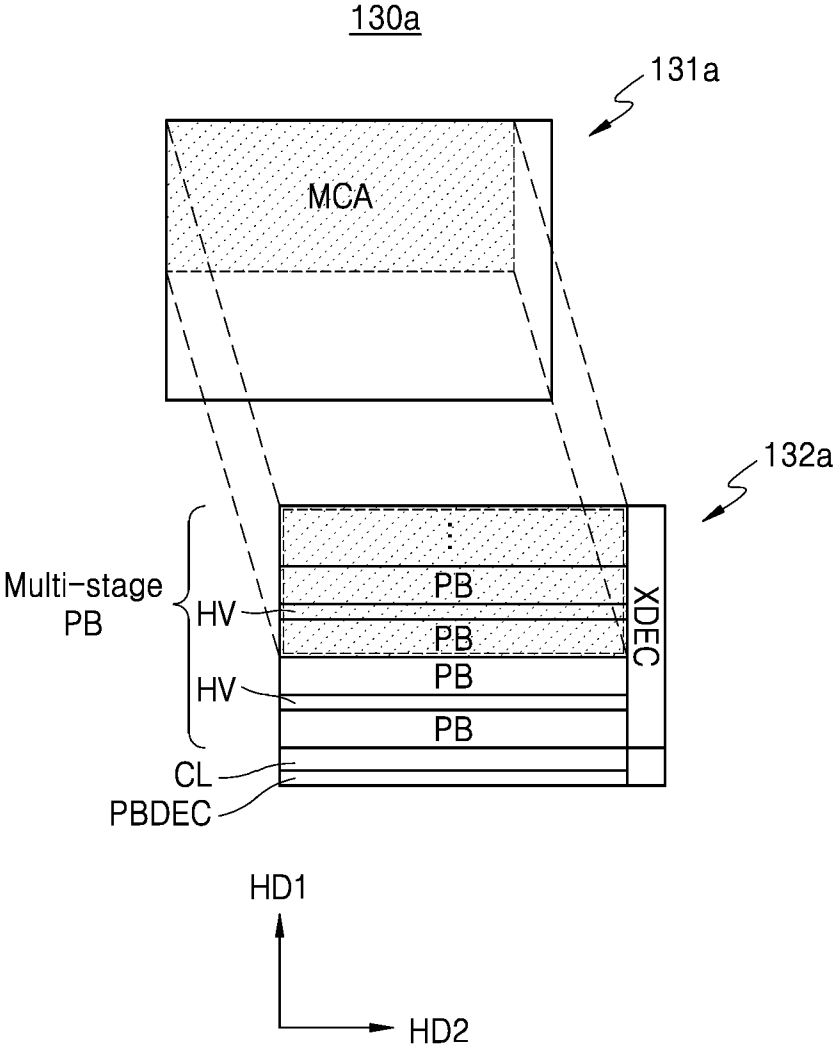

130a
131a
MCA
132a
Multi-stage PB
HV
HV
PB
PB
PB
PB
XDEC
CL
PBDEC
HD1
HD2

FIG. 13B

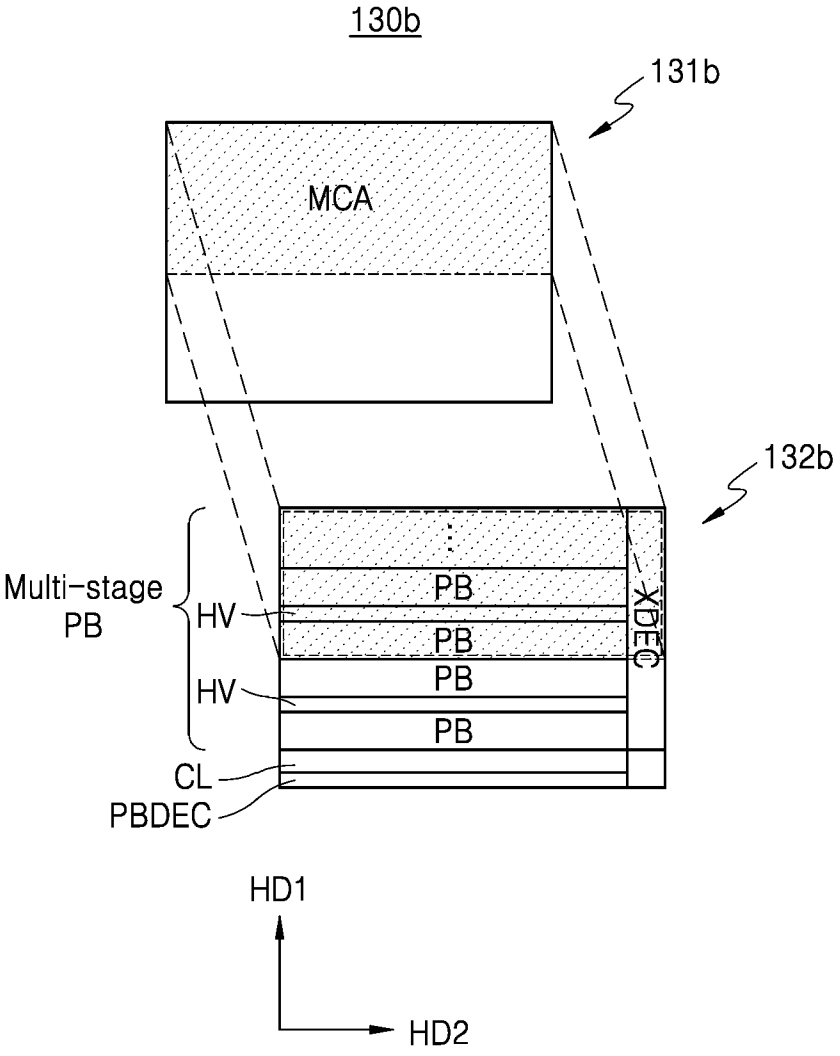

130b
131b
MCA
132b
Multi-stage PB
HV
HV
PB
PB
PB
PB
XDEC
CL
PBDEC
HD1
HD2

FIG. 14A

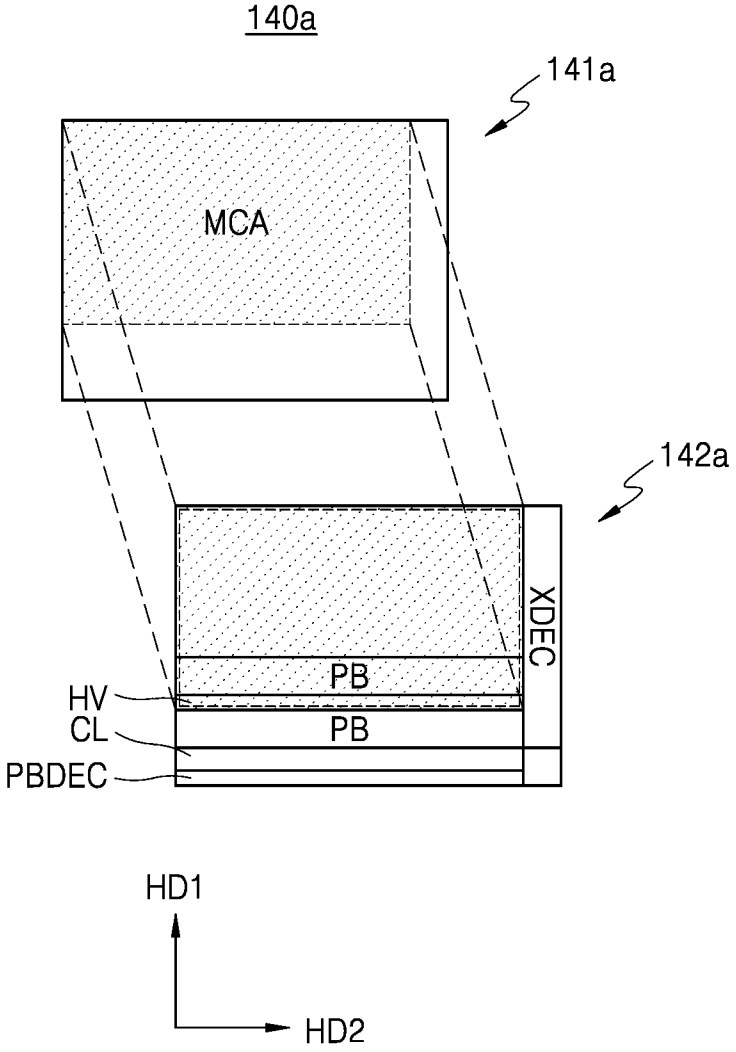


FIG. 14B

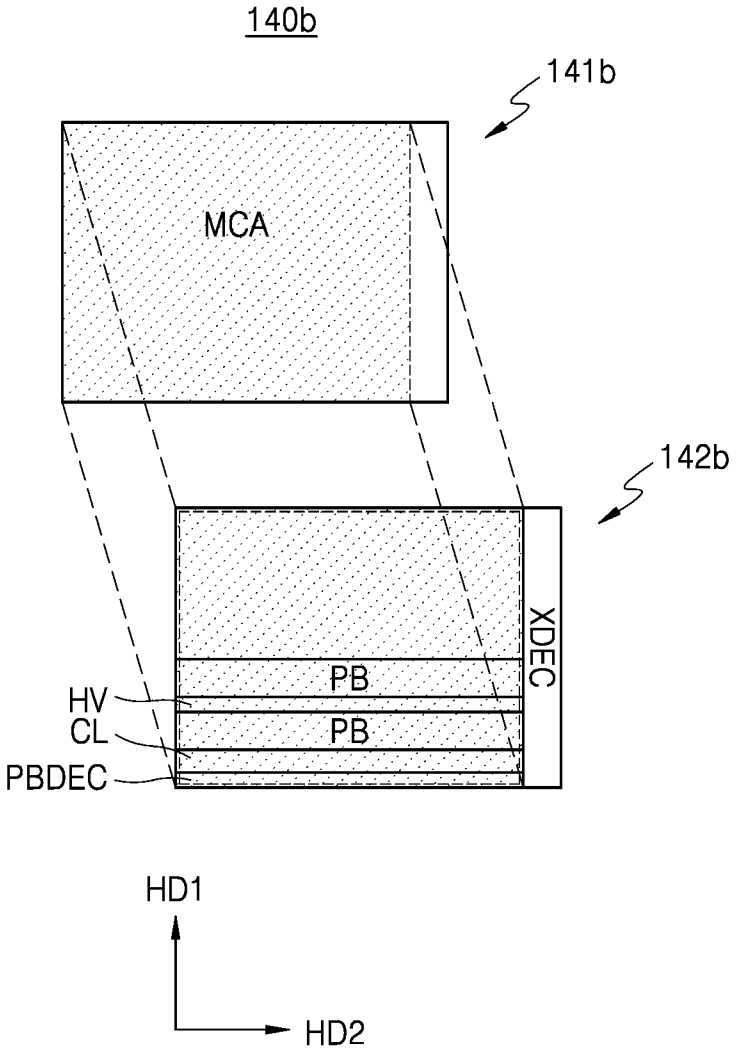


FIG. 15A

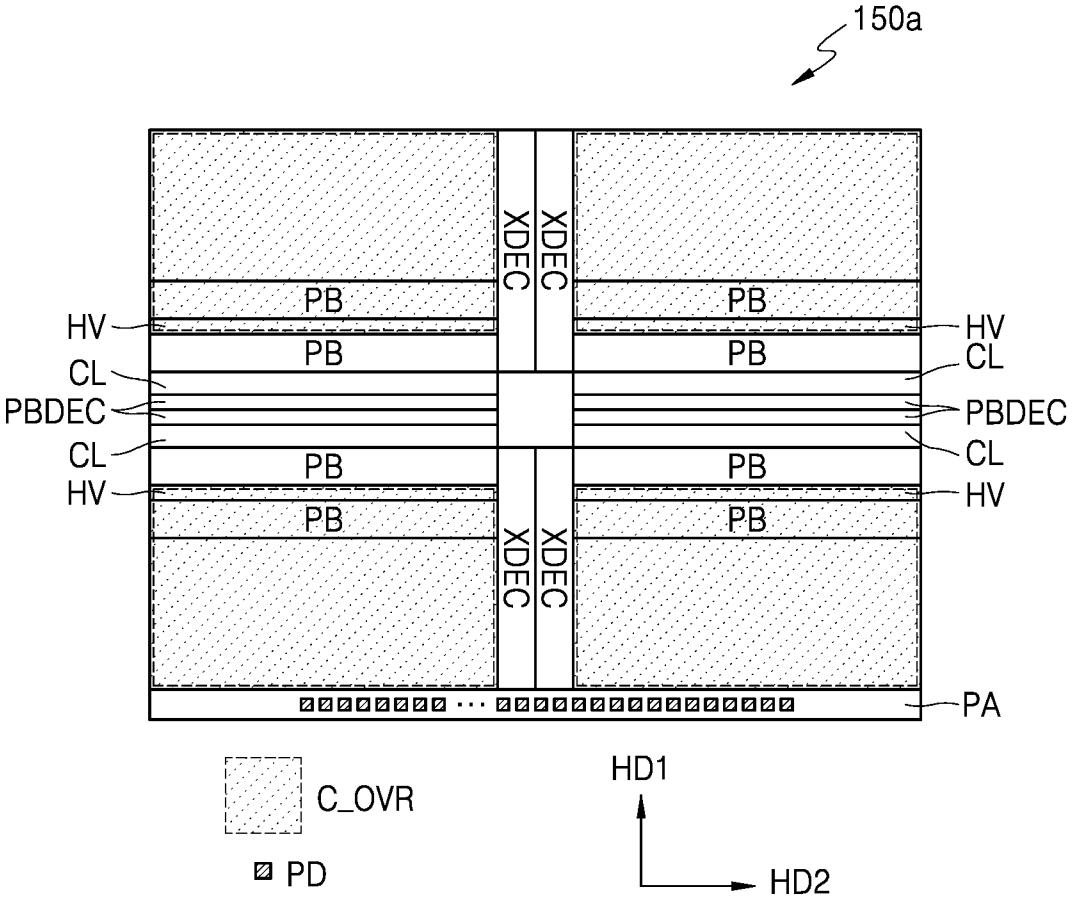


FIG. 15B

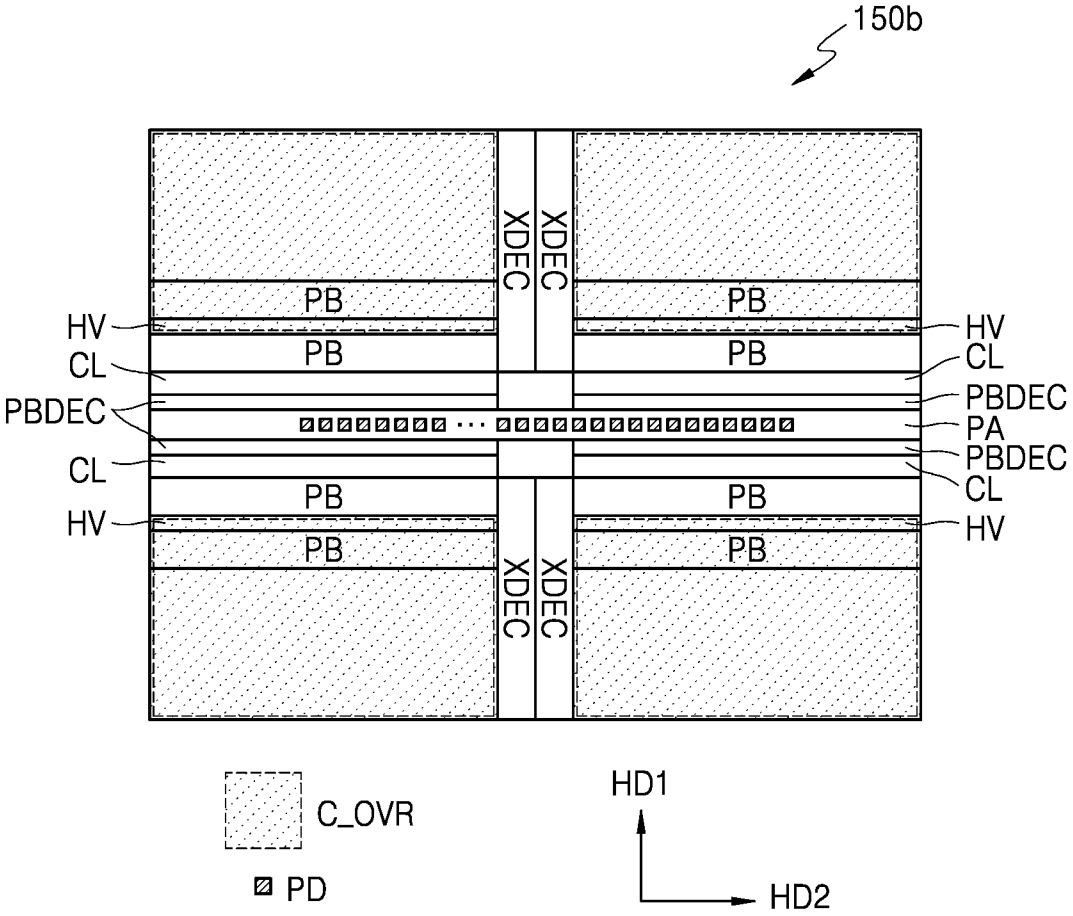


FIG. 15C

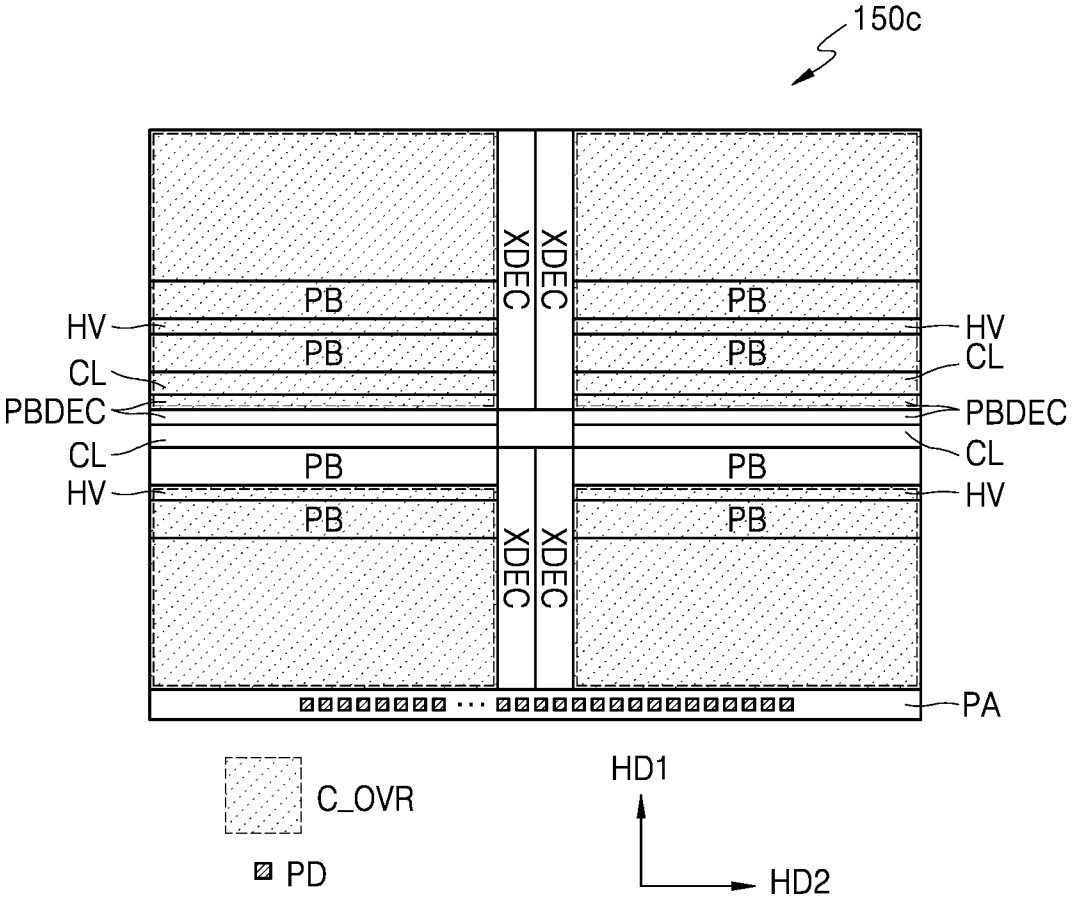


FIG. 15D

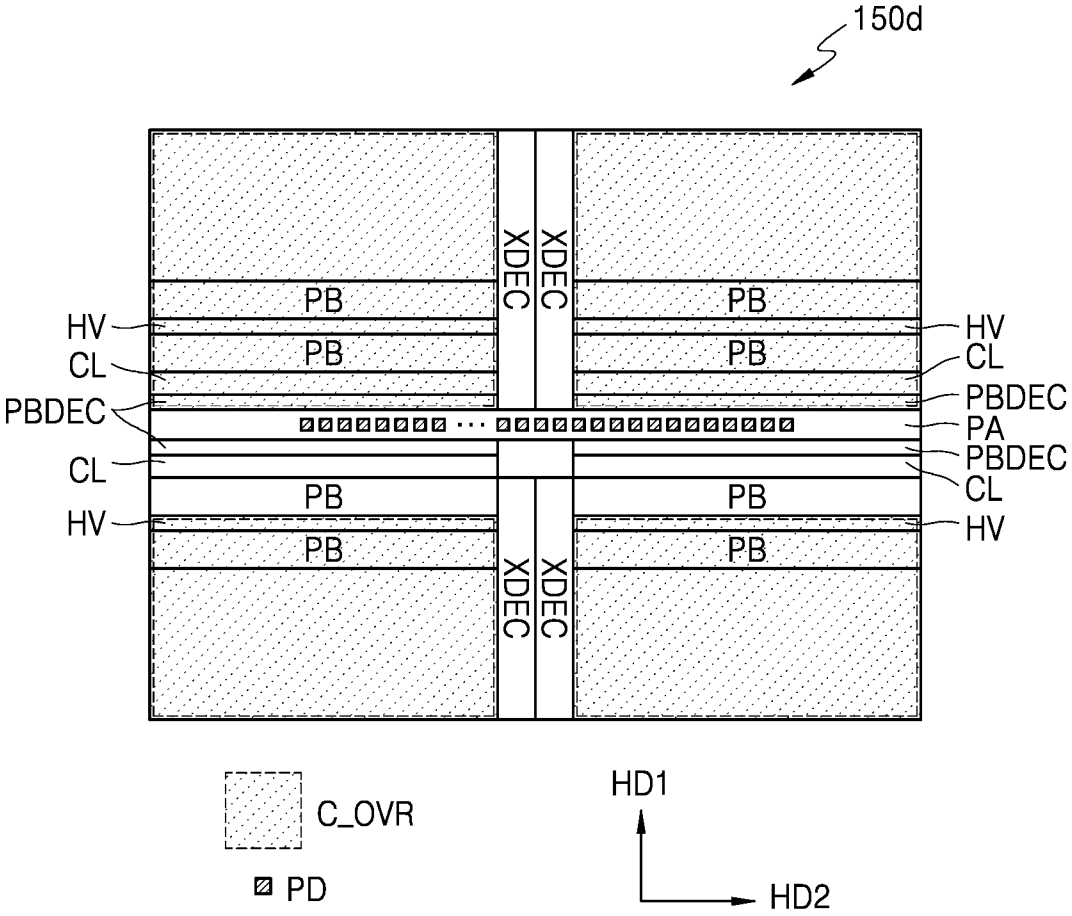


FIG. 16A

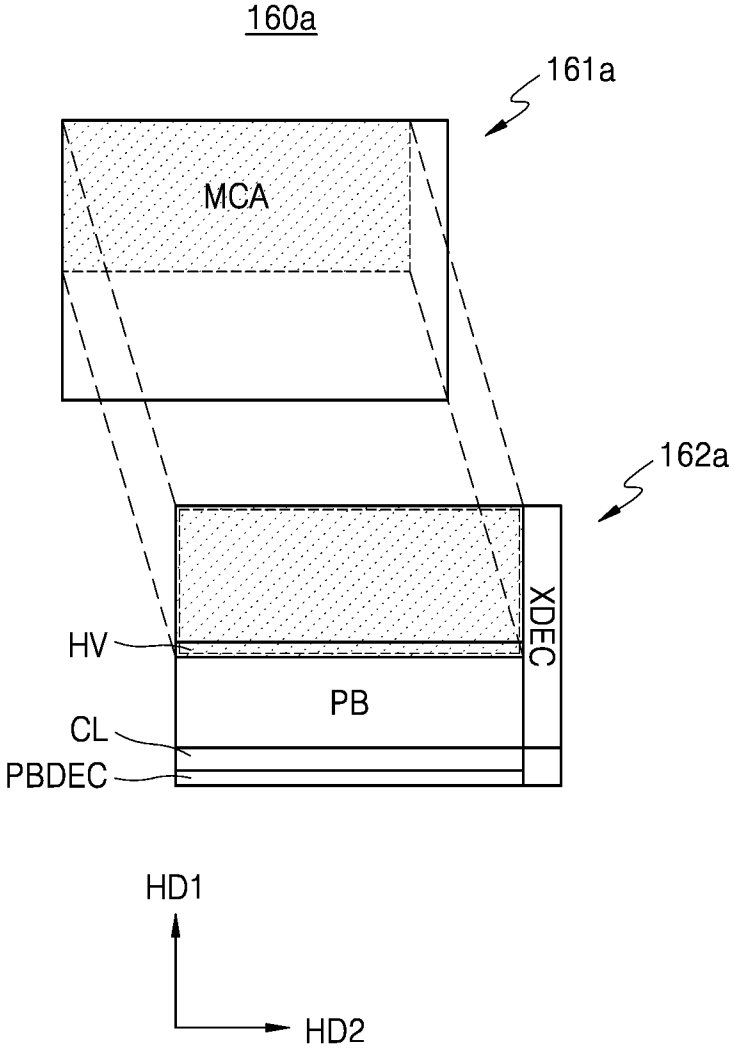


FIG. 16B

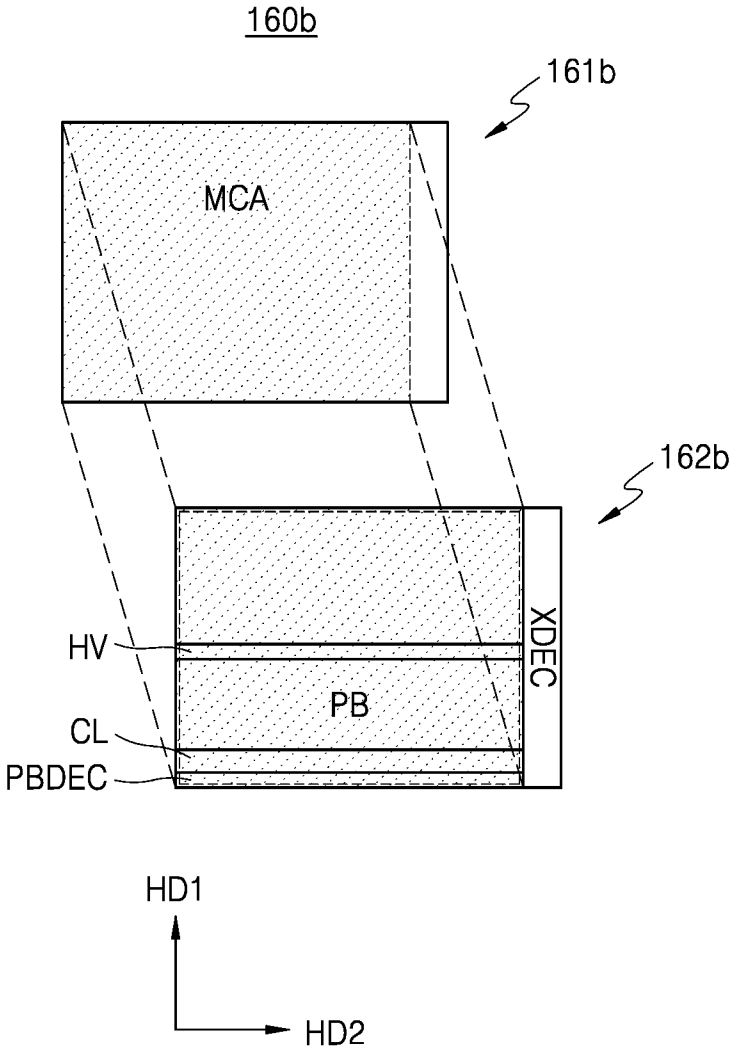


FIG. 17A

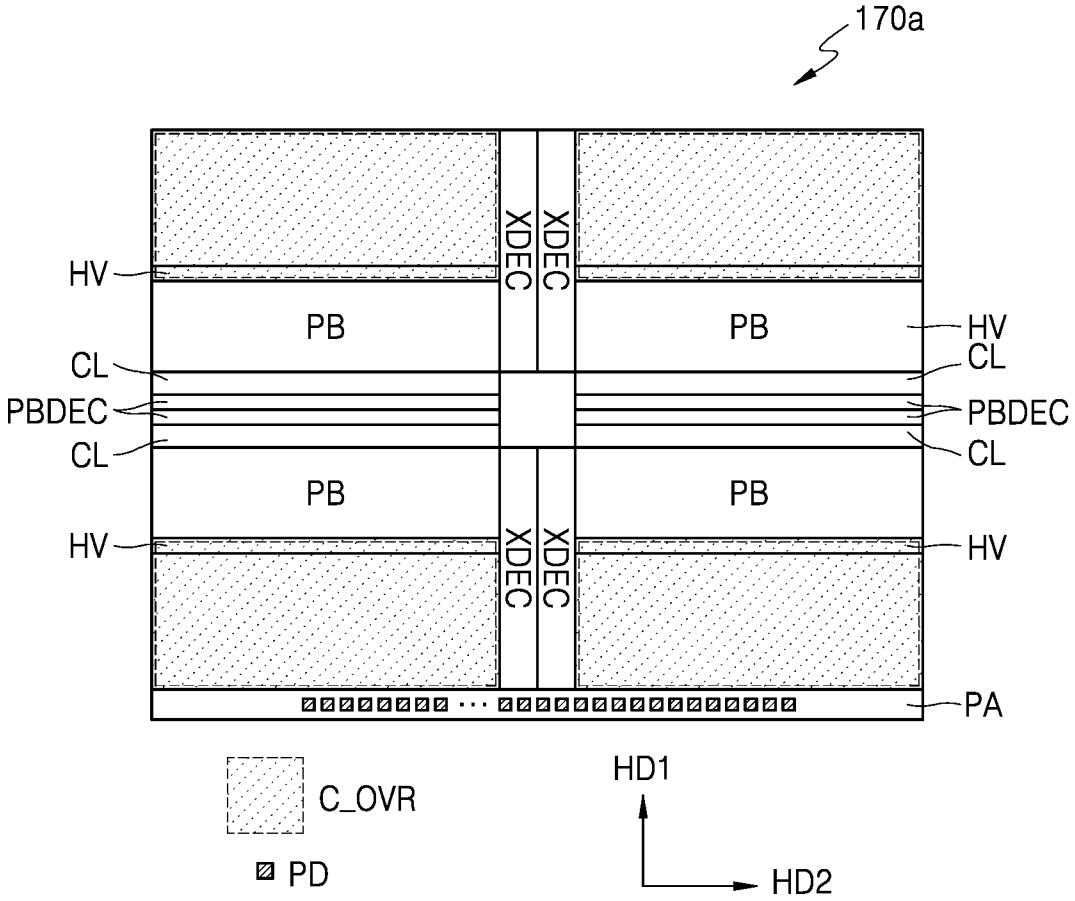

170a
HV
PB
PB
HV
CL
CL
PBDEC
PBDEC
CL
CL
PB
PB
HV
HV
XDEC
XDEC
XDEC
XDEC
PA
C_OVR
PD
HD1
HD2

FIG. 17B

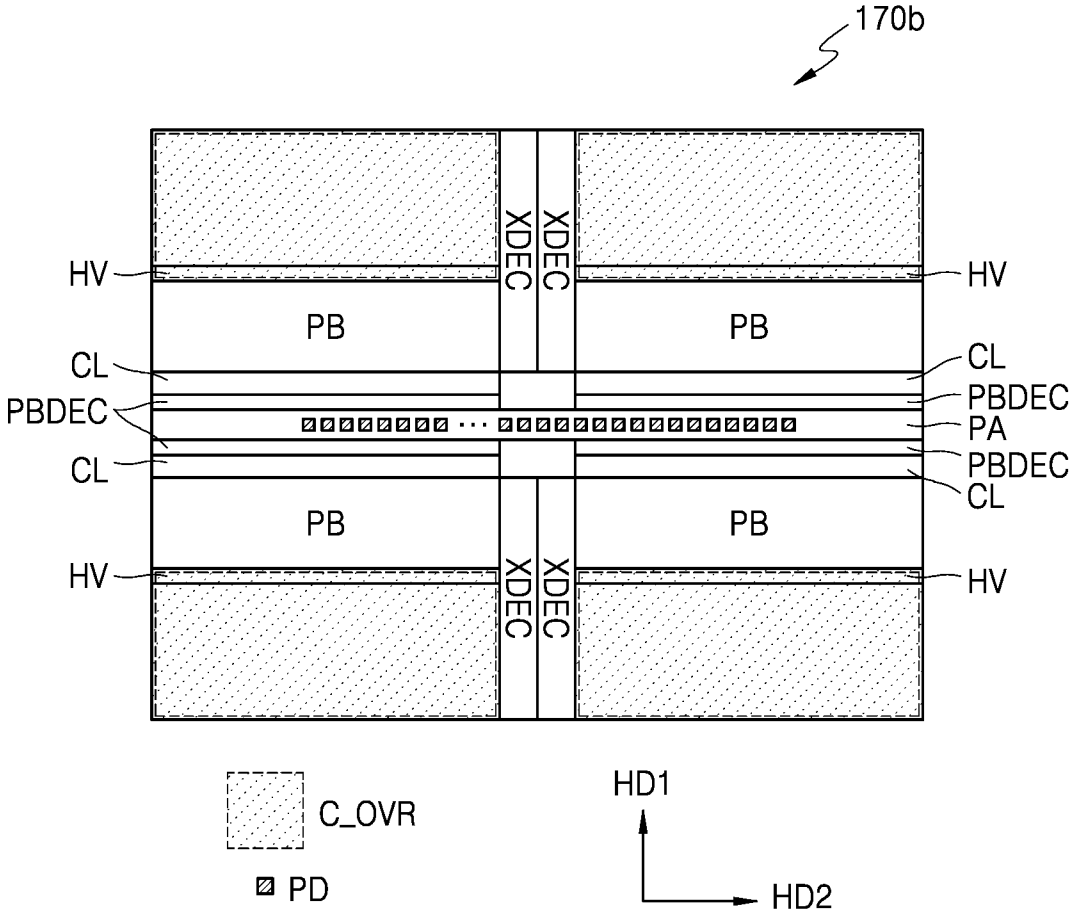

170b
HV
PB
CL
PBDEC
CL
PB
HV
XDEC
XDEC
HV
PB
CL
PBDEC
PA
PBDEC
CL
PB
HV
C_OVR
PD
HD1
HD2

FIG. 17C

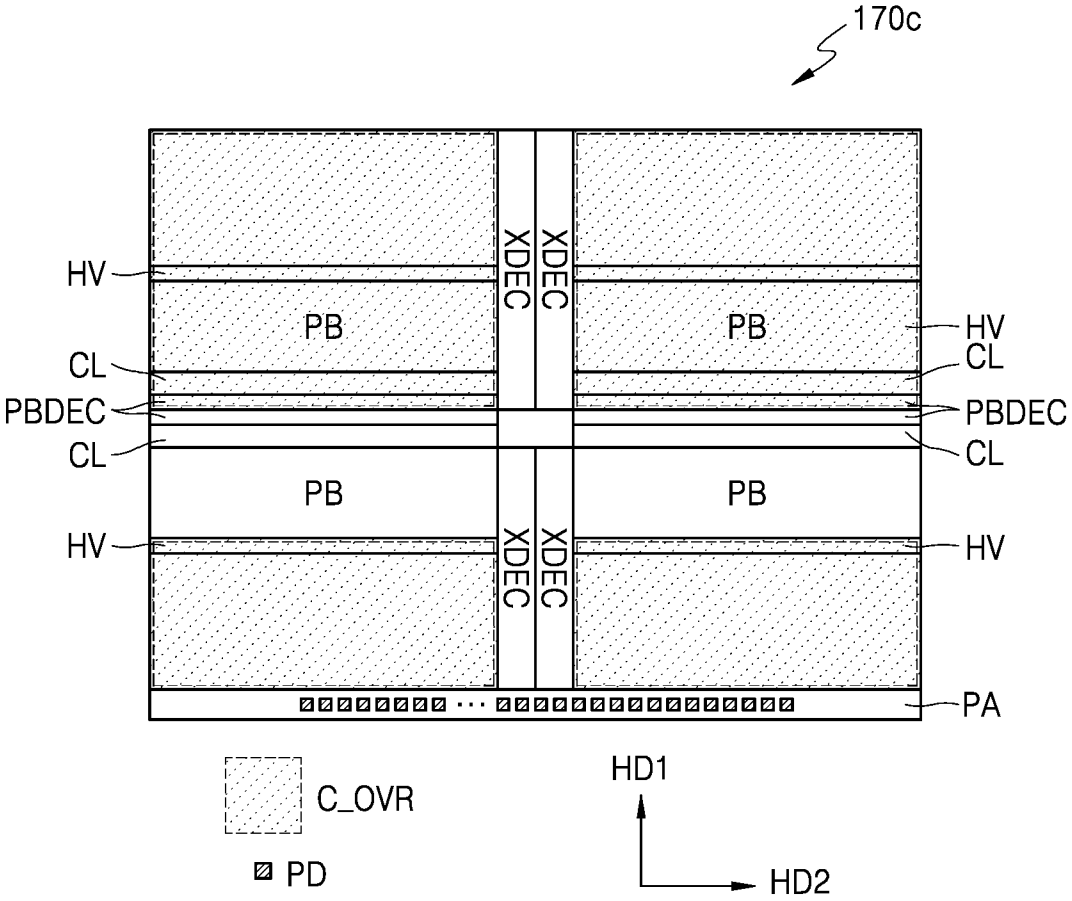

170c
HV
CL
PBDEC
CL
HV
PB
PB
XDEC
XDEC
PB
PB
XDEC
XDEC
HV
CL
PBDEC
CL
HV
PA
C_OVR
PD
HD1
HD2

FIG. 17D

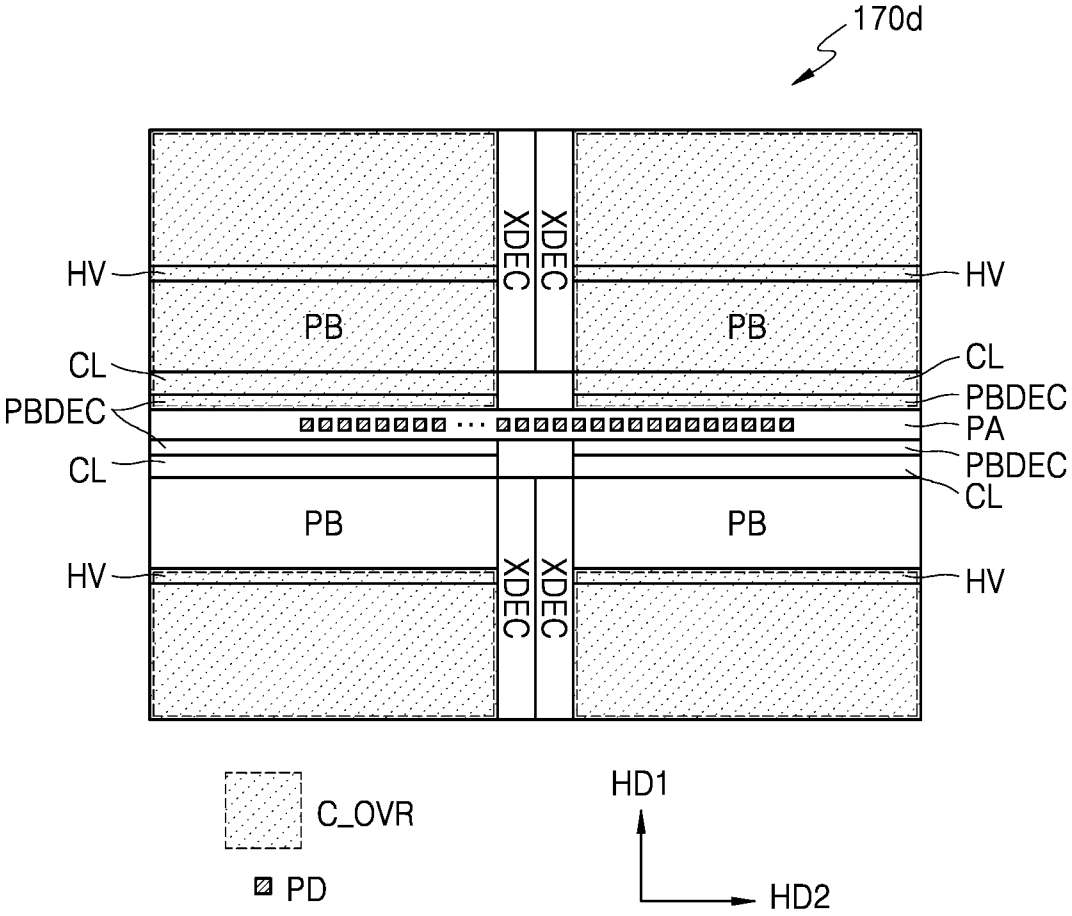

170d
HV
PB
CL
PBDEC
CL
PB
HV
XDEC
XDEC
HV
PB
CL
PBDEC
PA
PBDEC
CL
PB
HV
C_OVR
PD
HD1
HD2

FIG. 18A

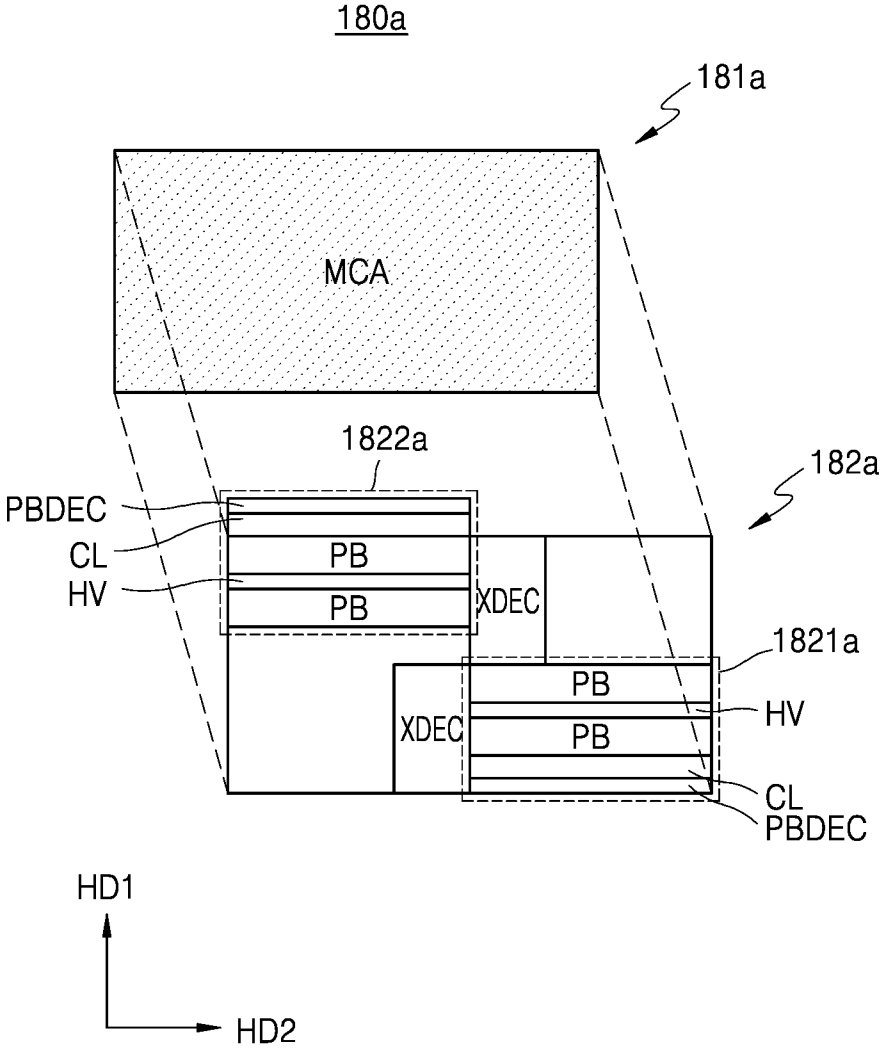

180a
181a
MCA
1822a
182a
PBDEC
CL
HV
PB
PB
XDEC
1821a
PB
HV
XDEC
PB
CL
PBDEC
HD1
HD2

FIG. 18B

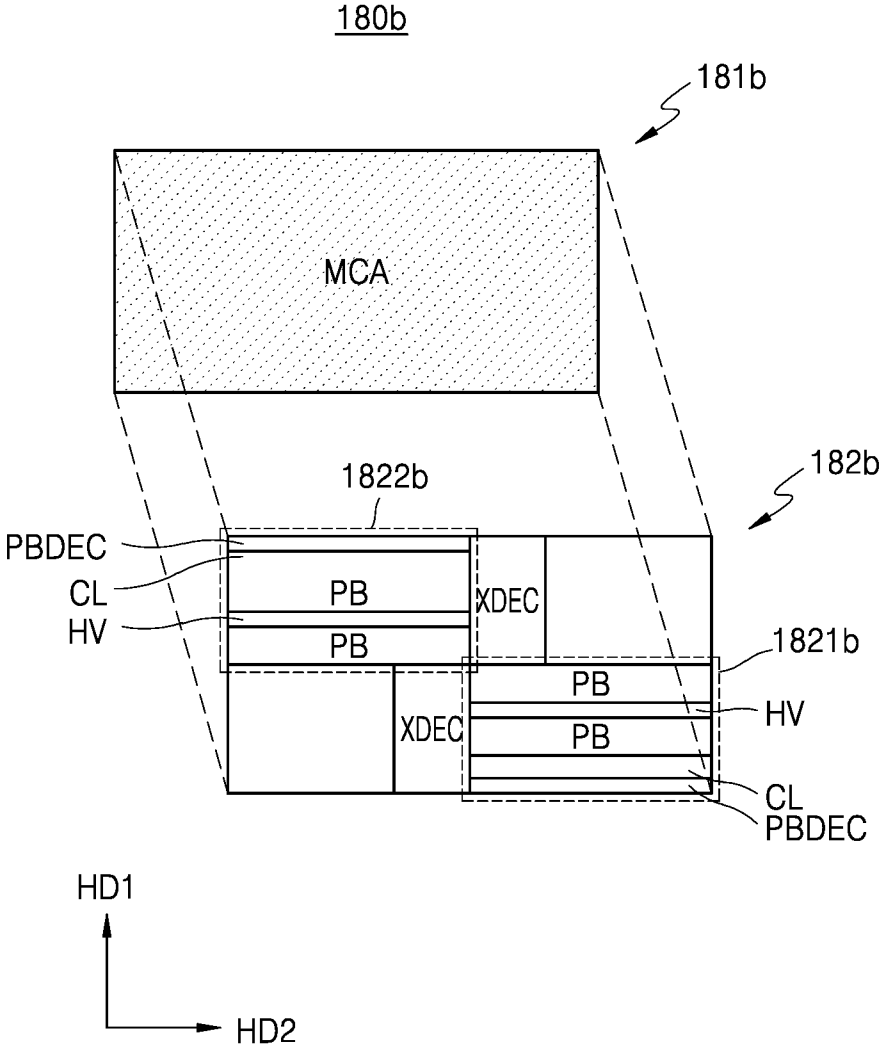

180b
181b
MCA
182b
1822b
PBDEC
CL
HV
PB
PB
XDEC
1821b
PB
HV
XDEC
PB
CL
PBDEC
HD1
HD2

FIG. 19A

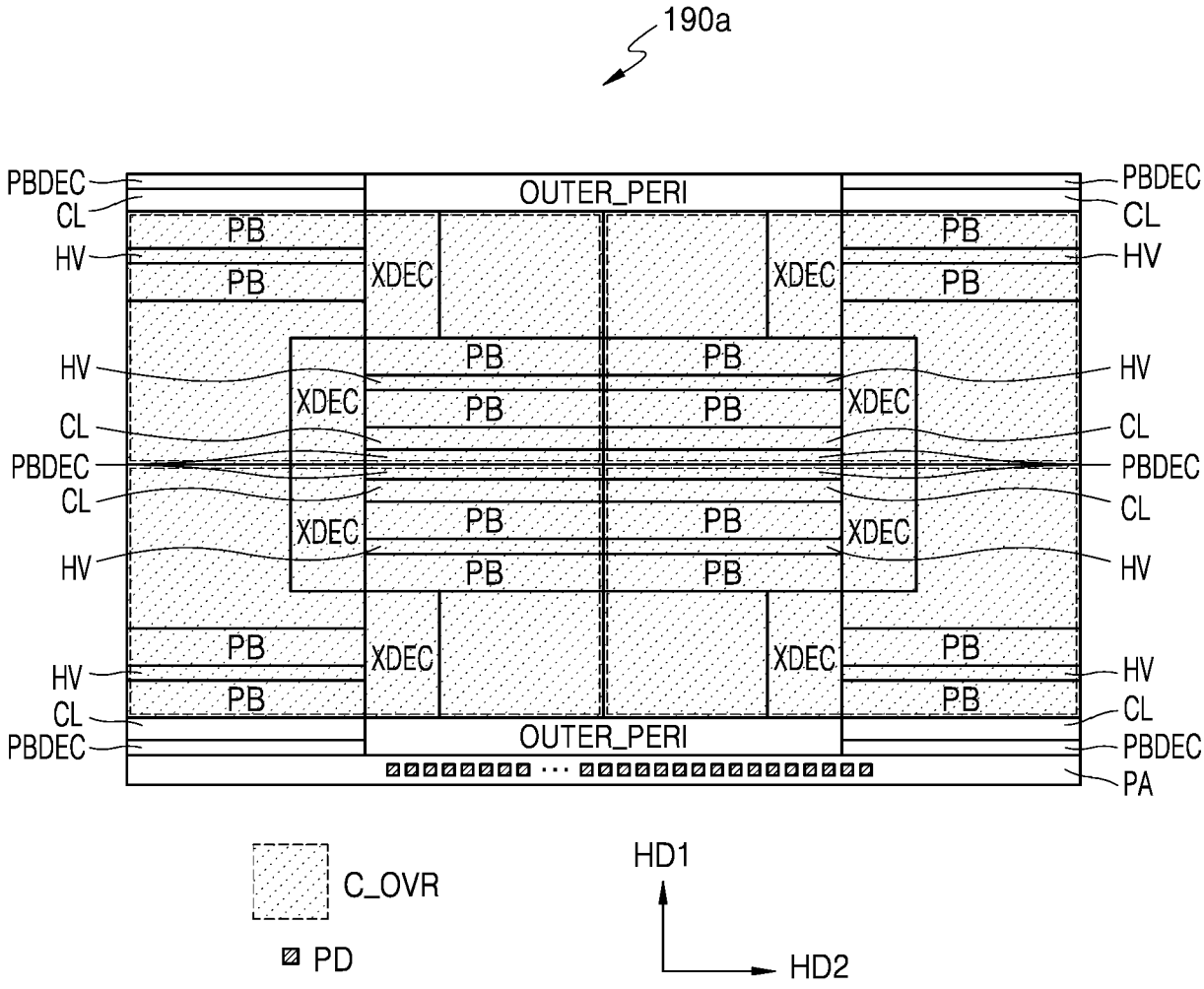


FIG. 19B

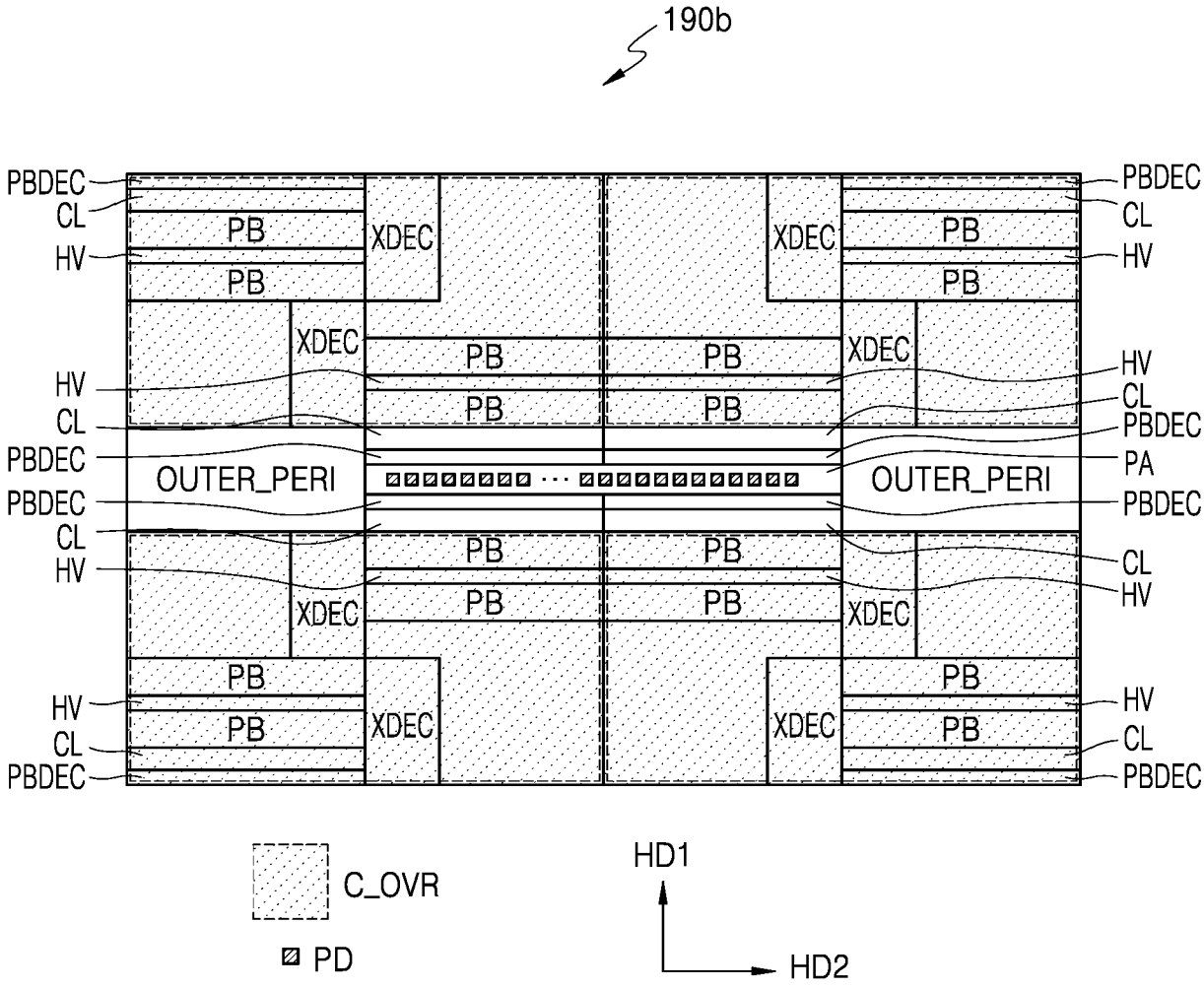


FIG. 19C

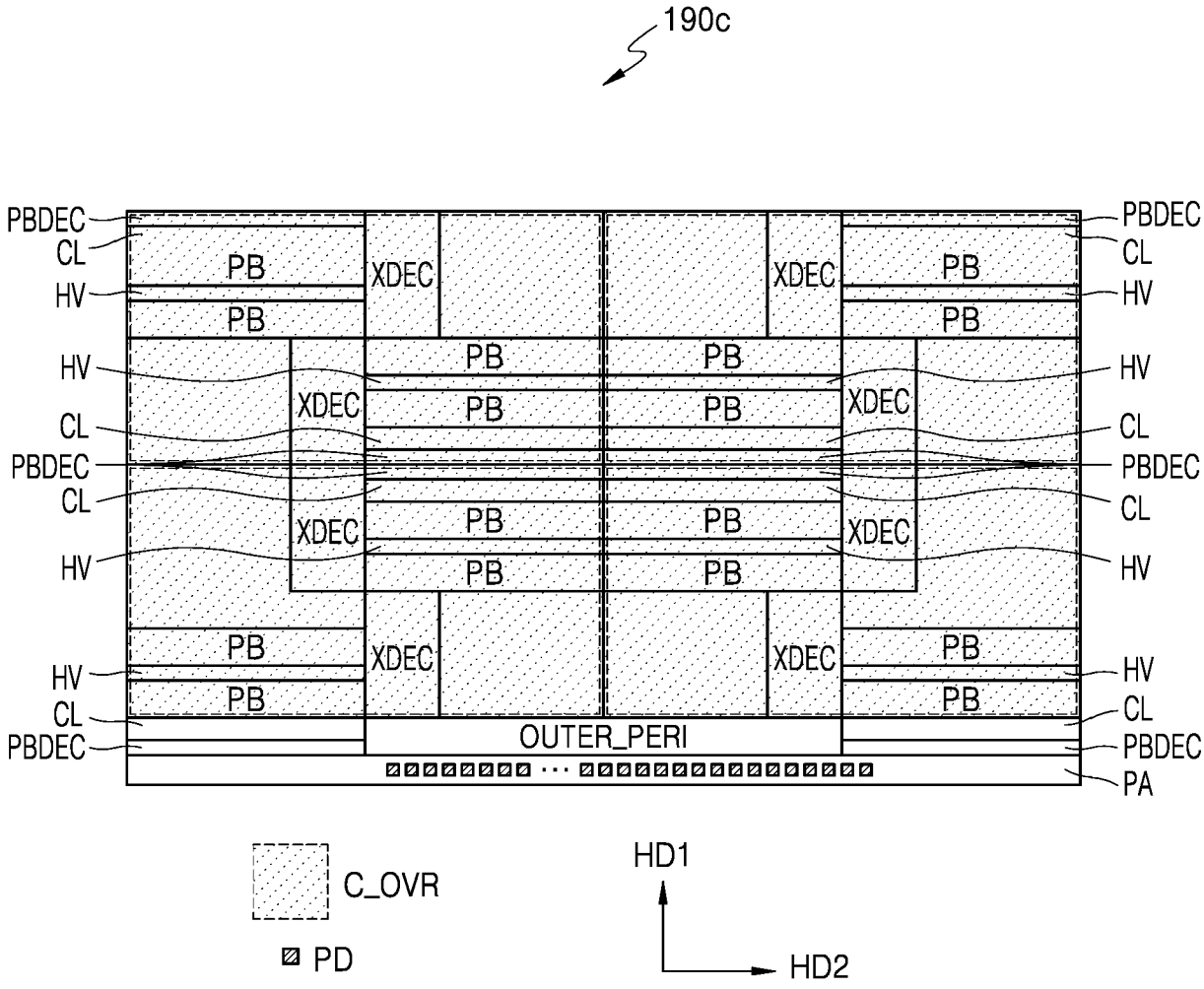


FIG. 19D

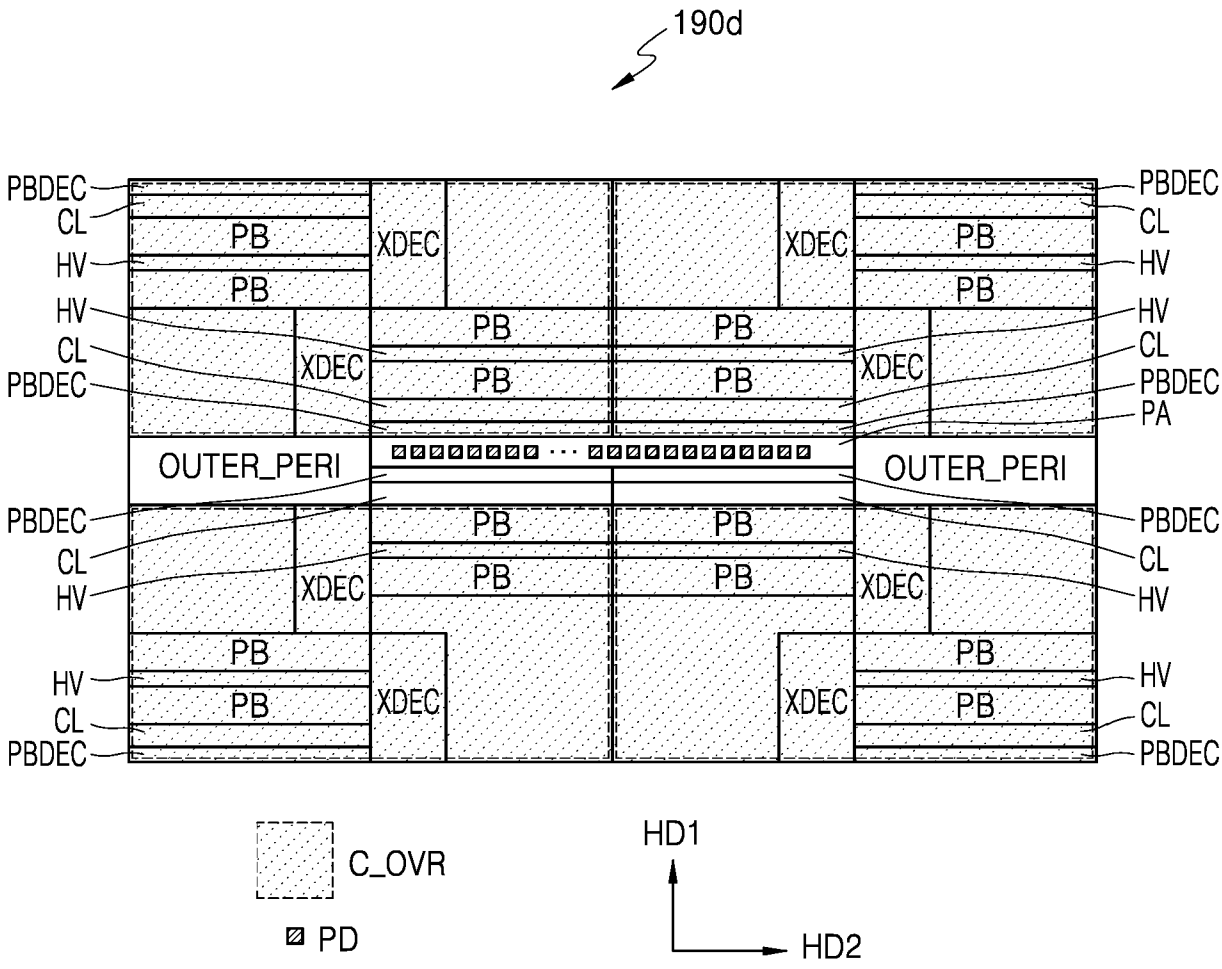


FIG. 20A

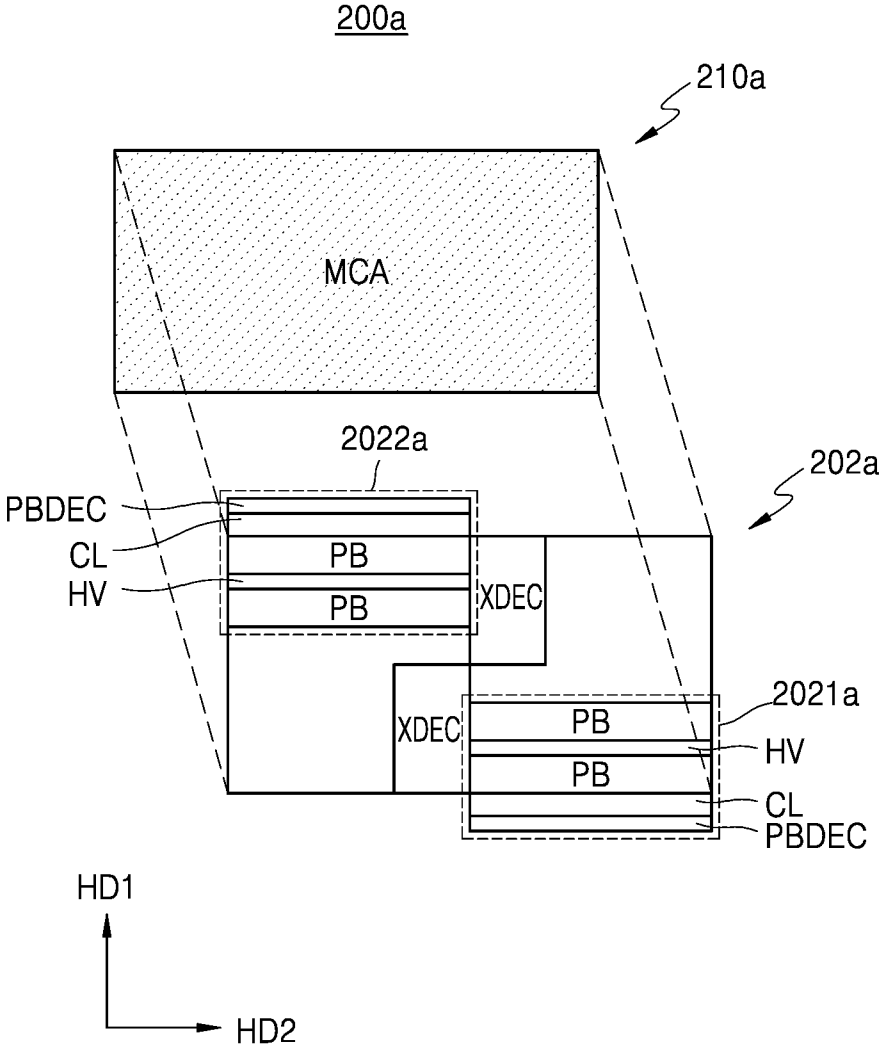

200a
210a
MCA
2022a
202a
PBDEC
CL
HV
PB
PB
XDEC
XDEC
2021a
PB
PB
HV
CL
PBDEC
HD1
HD2

FIG. 20B

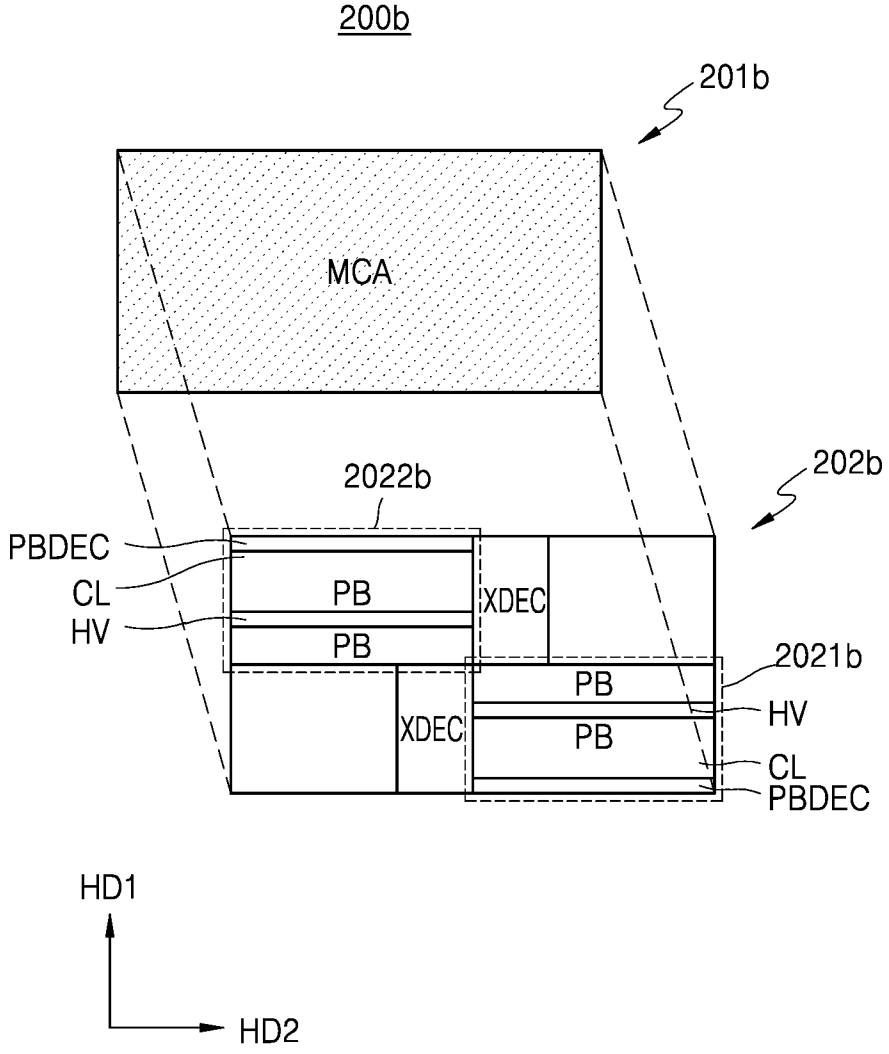

200b
201b
MCA
202b
2022b
PBDEC
CL
HV
PB
PB
XDEC
2021b
PB
HV
XDEC
PB
CL
PBDEC
HD1
HD2

FIG. 21A

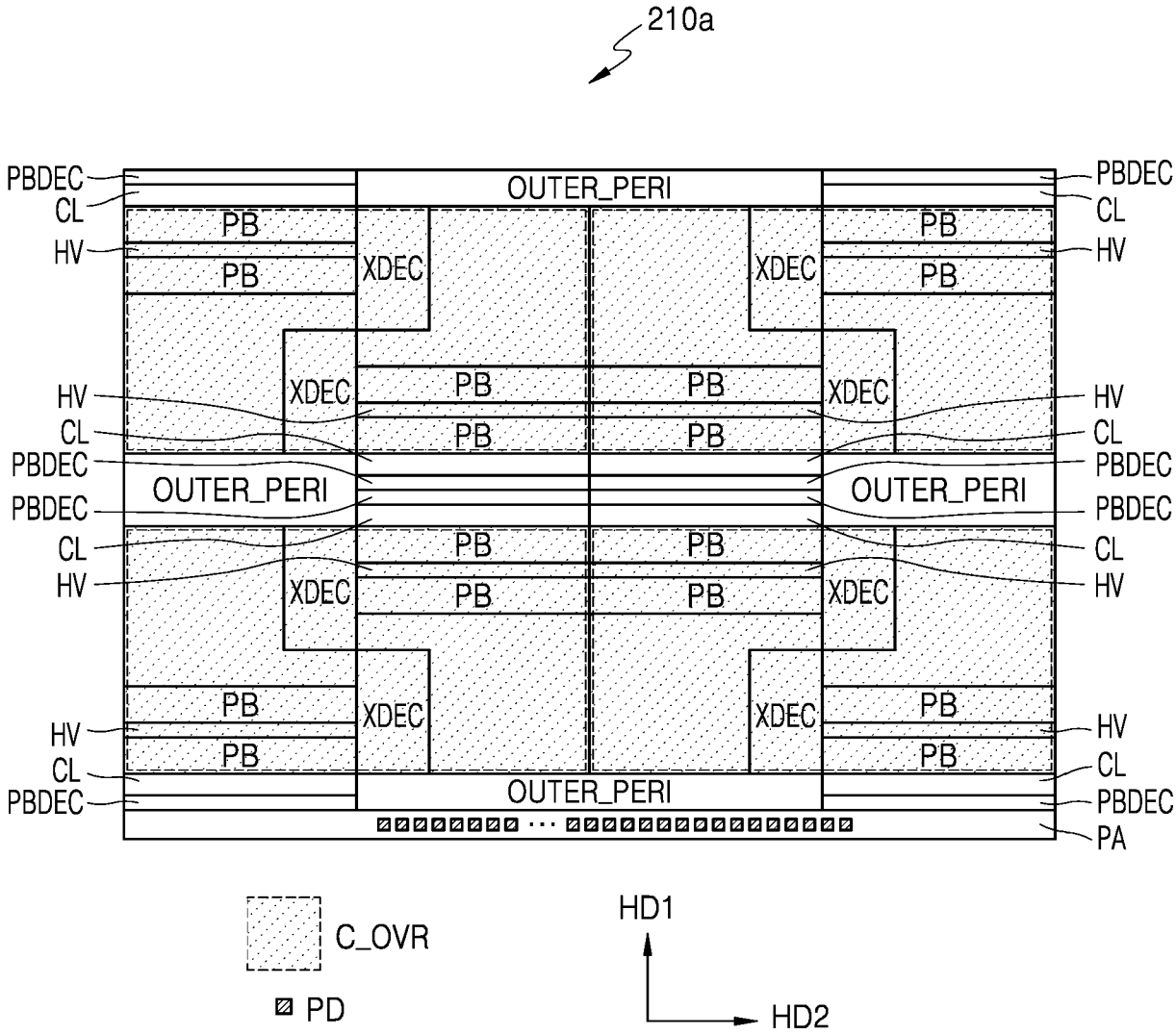


FIG. 21B

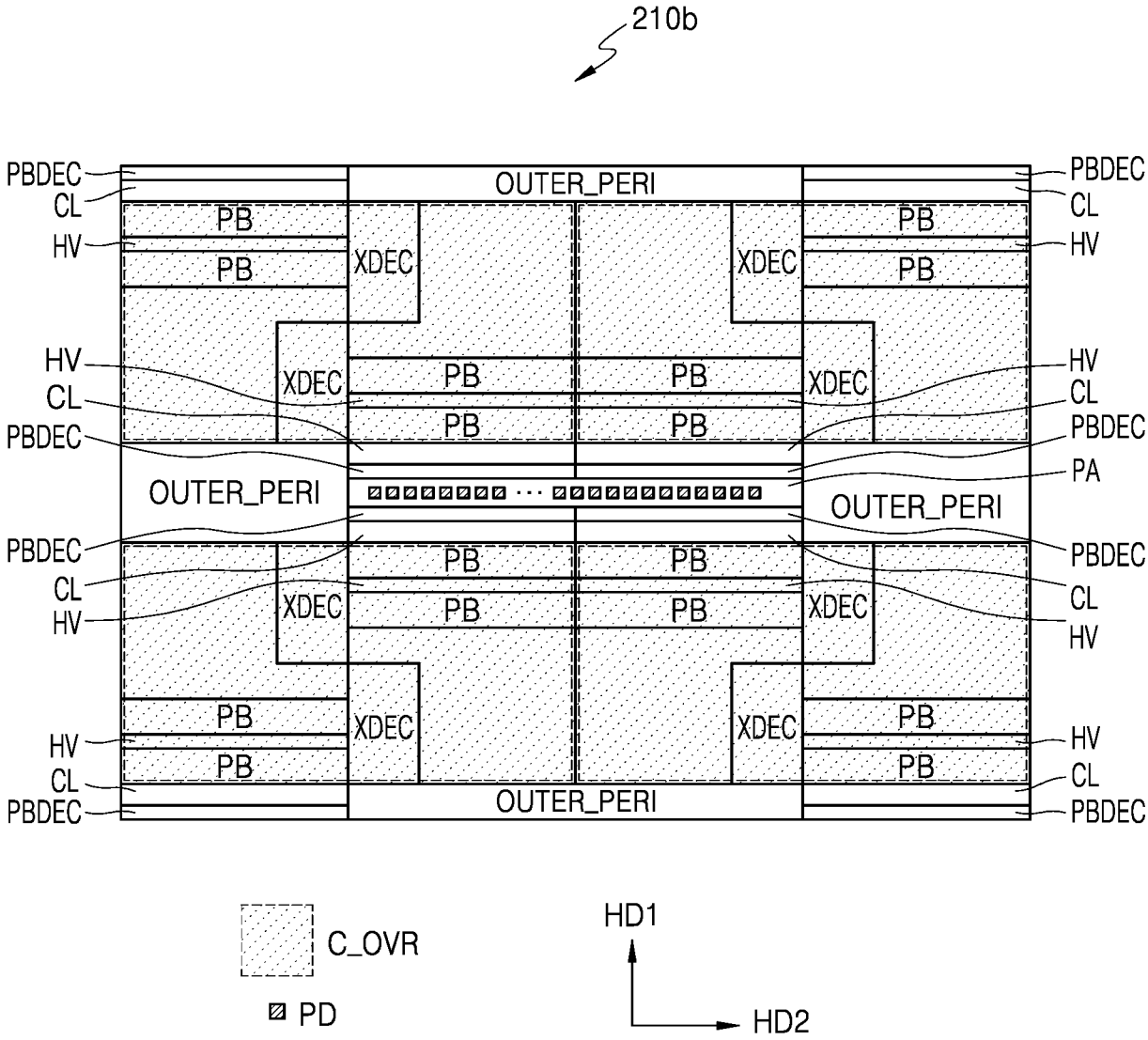


FIG. 21C

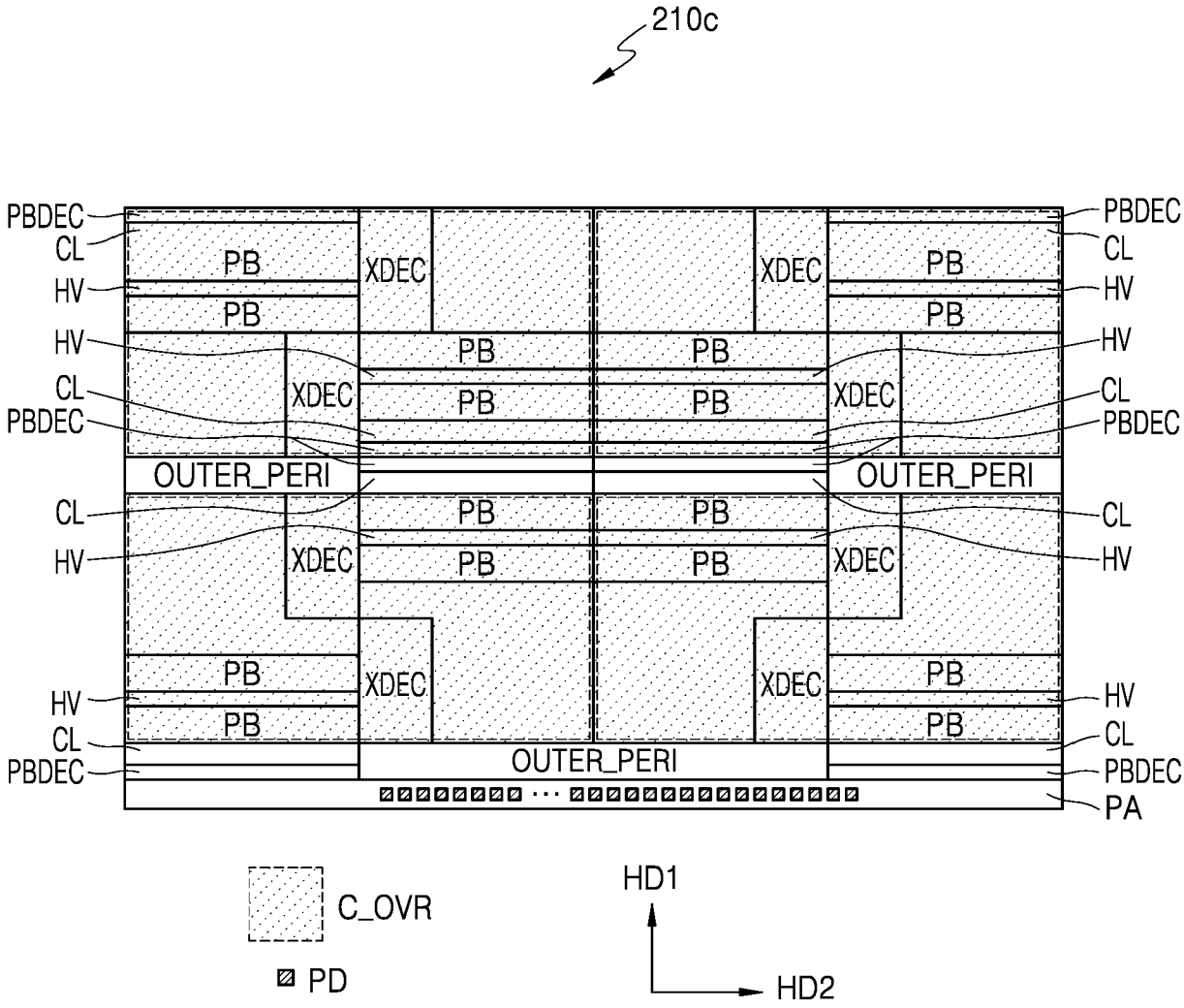


FIG. 21D

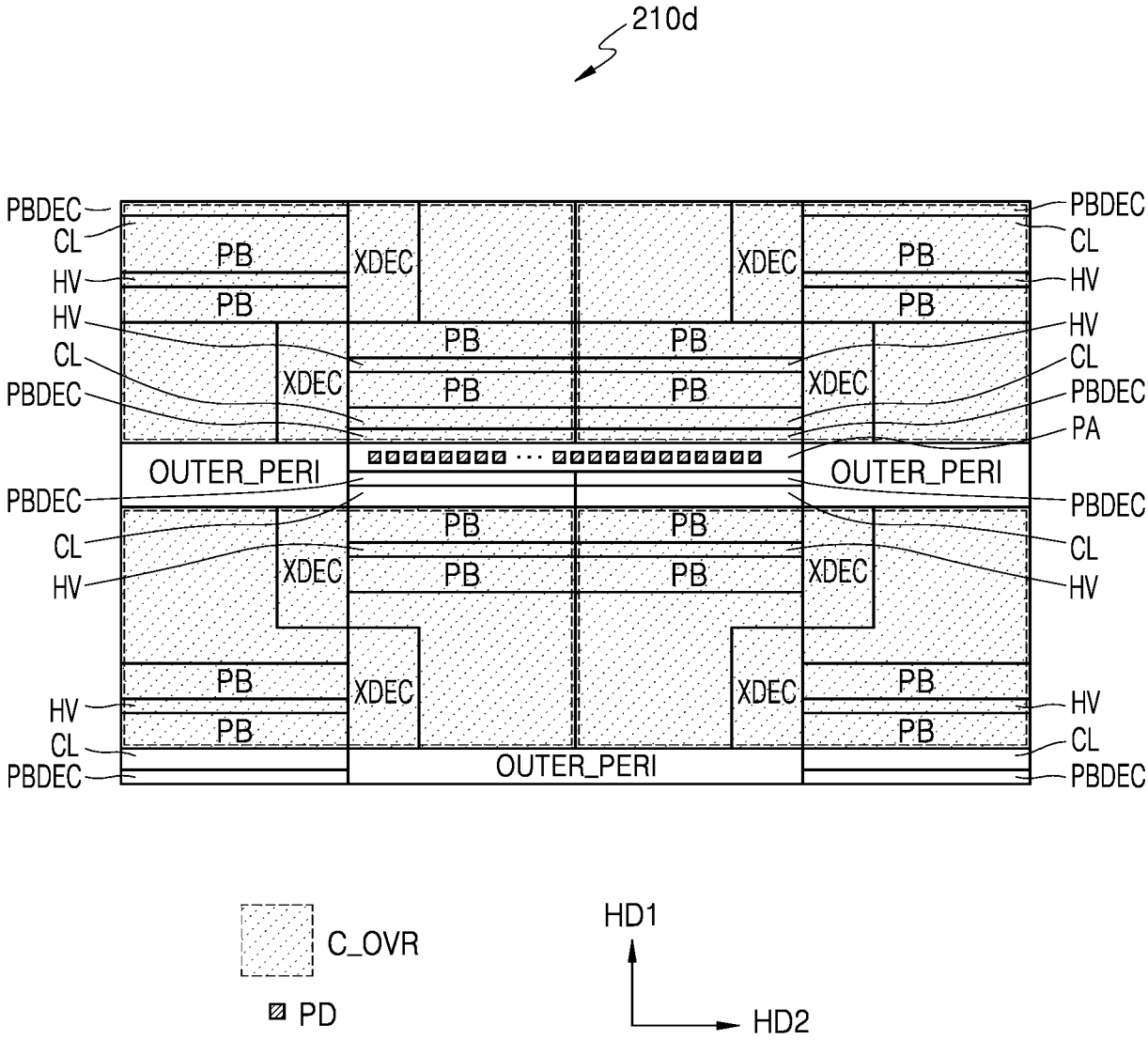


FIG. 22A

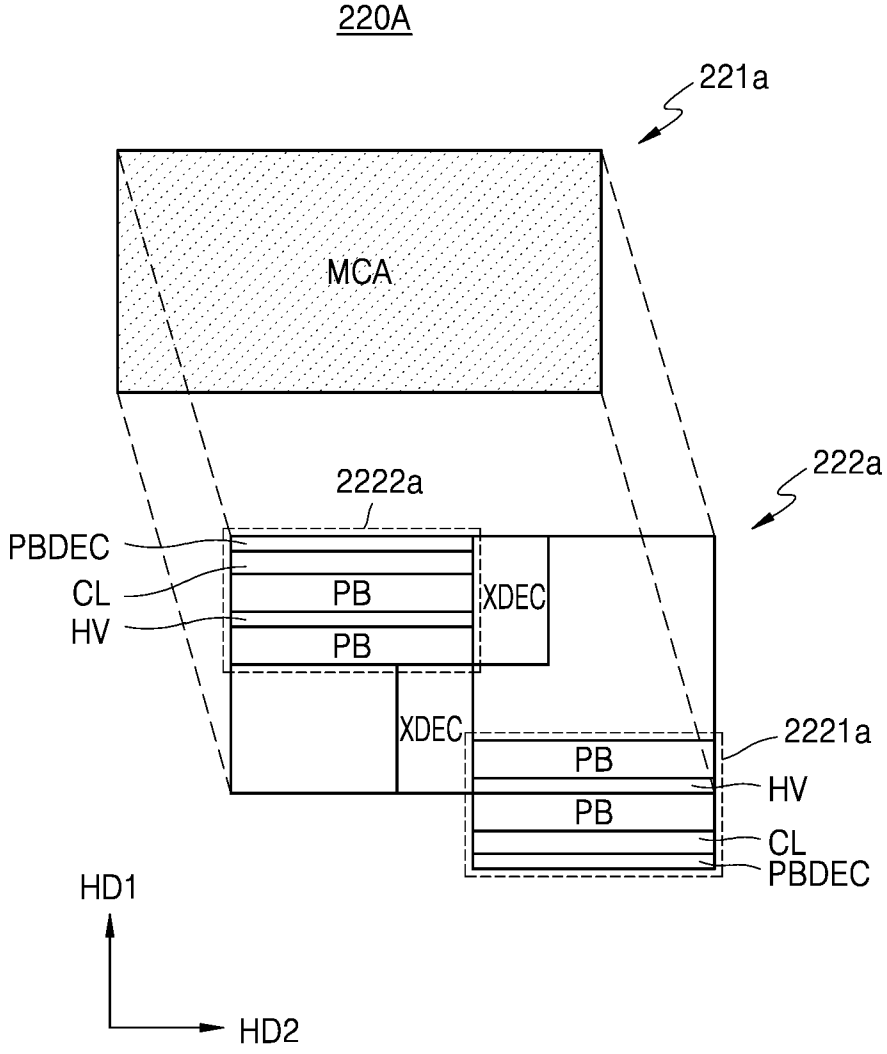

220A
221a
MCA
222a
2222a
PBDEC
CL
HV
PB
PB
XDEC
XDEC
2221a
PB
HV
PB
CL
PBDEC
HD1
HD2

FIG. 22B

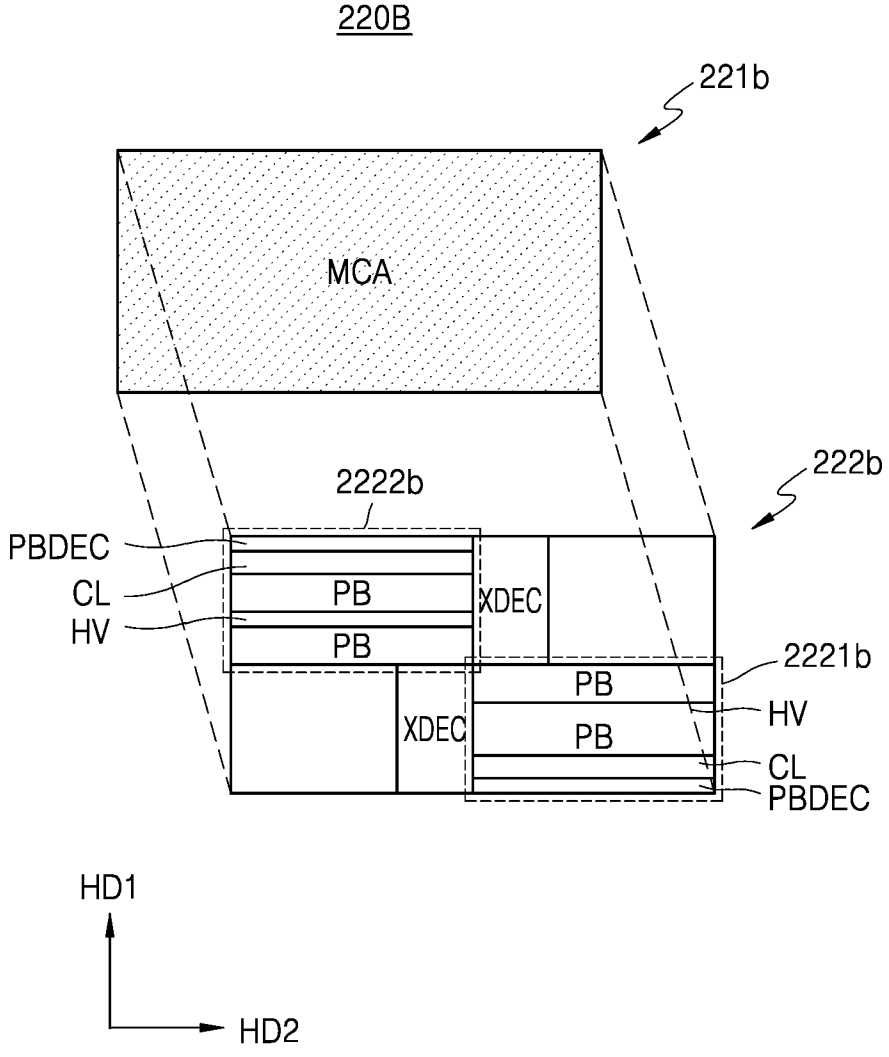

220B
221b
MCA
222b
2222b
PBDEC
CL
HV
PB
PB
XDEC
2221b
PB
HV
XDEC
PB
CL
PBDEC
HD1
HD2

FIG. 23A

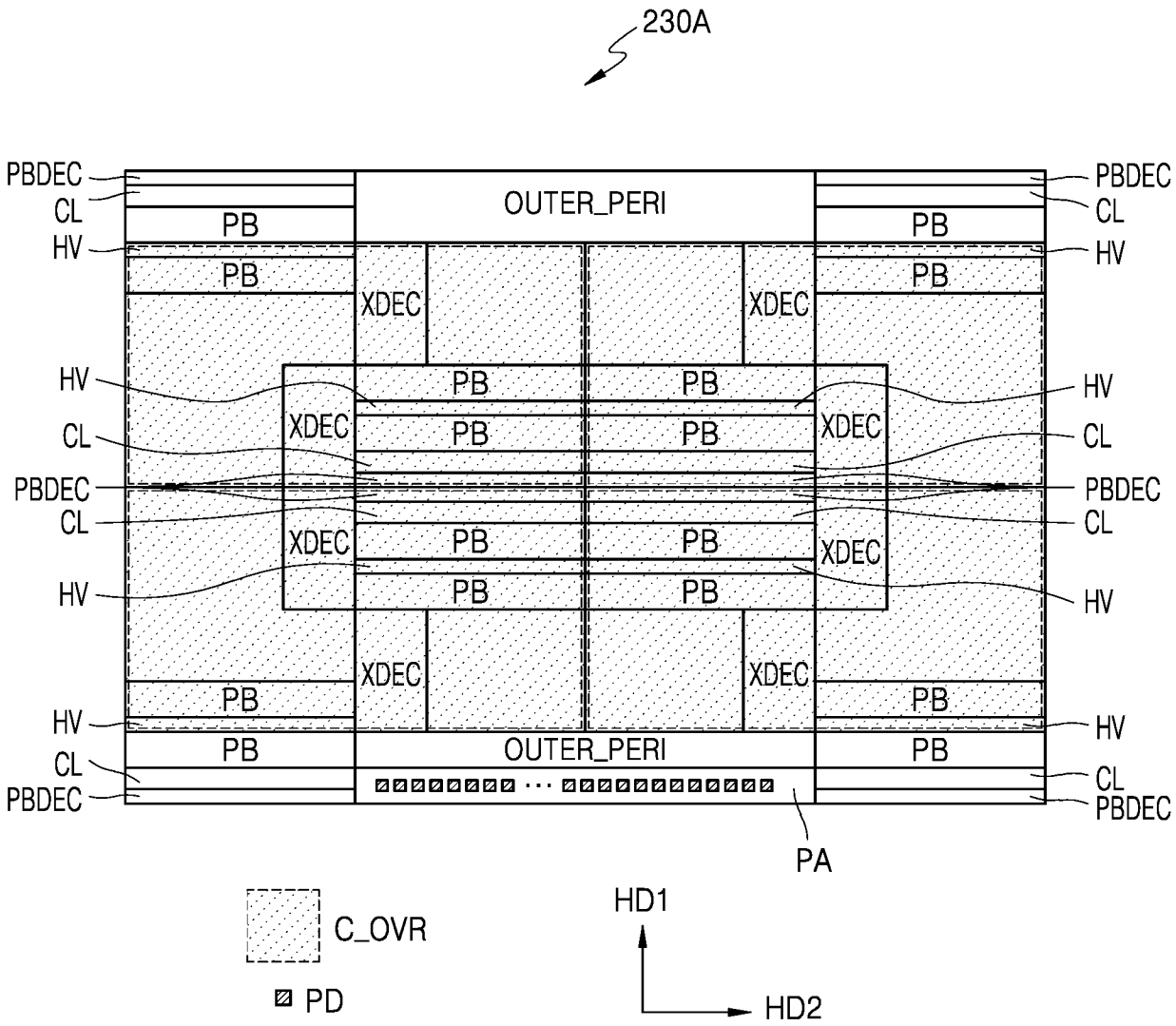


FIG. 23B

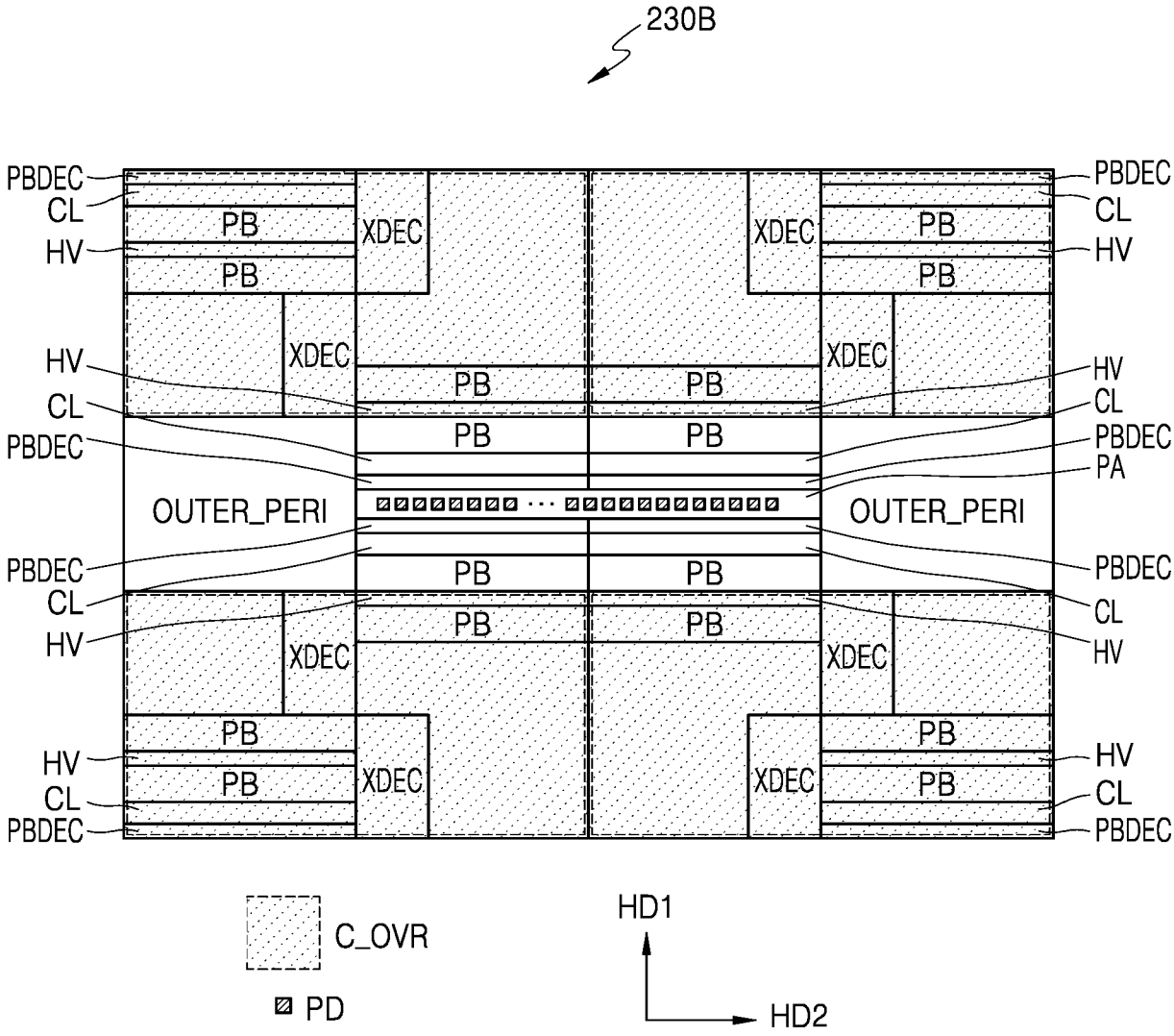


FIG. 23C

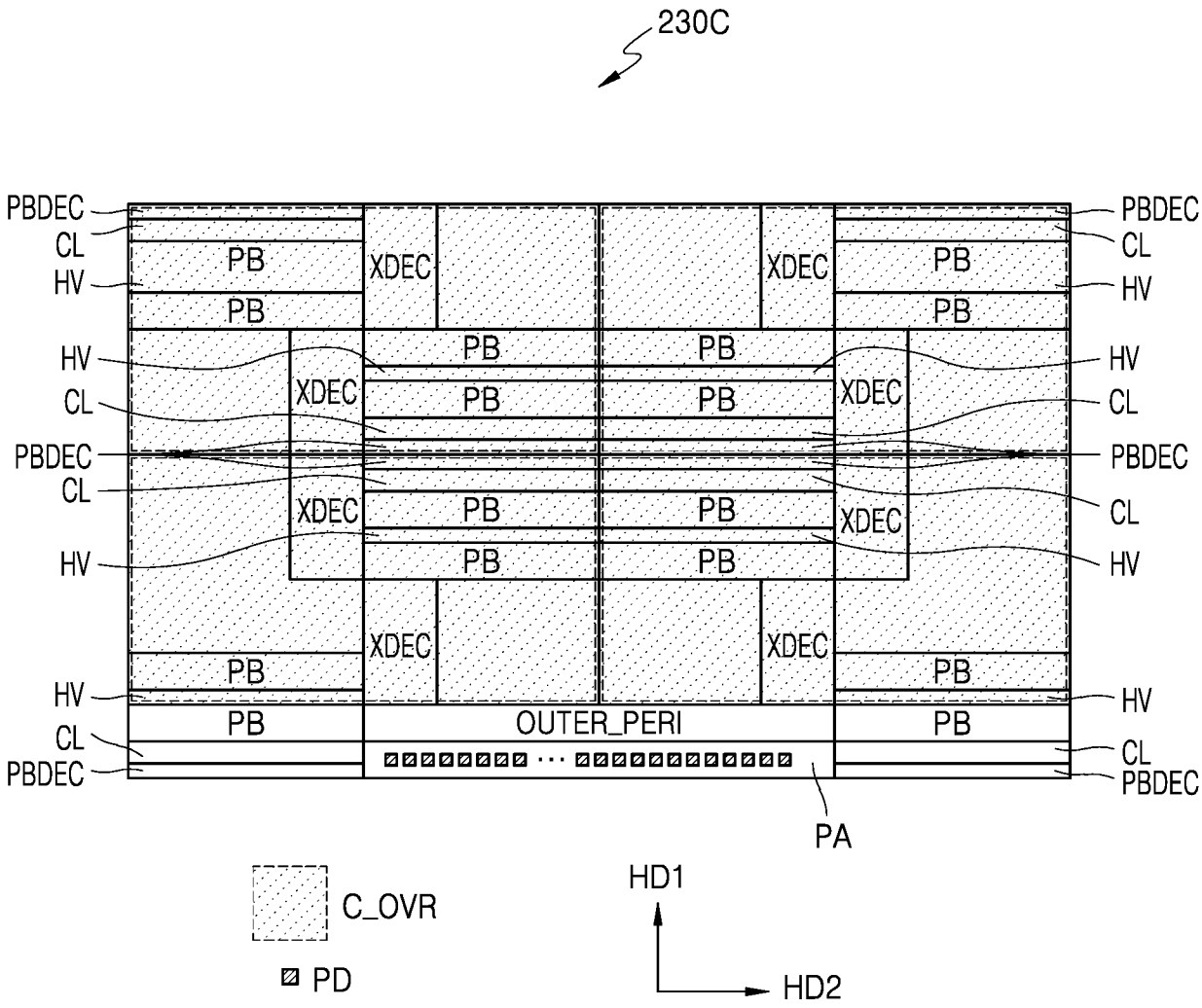


FIG. 23D

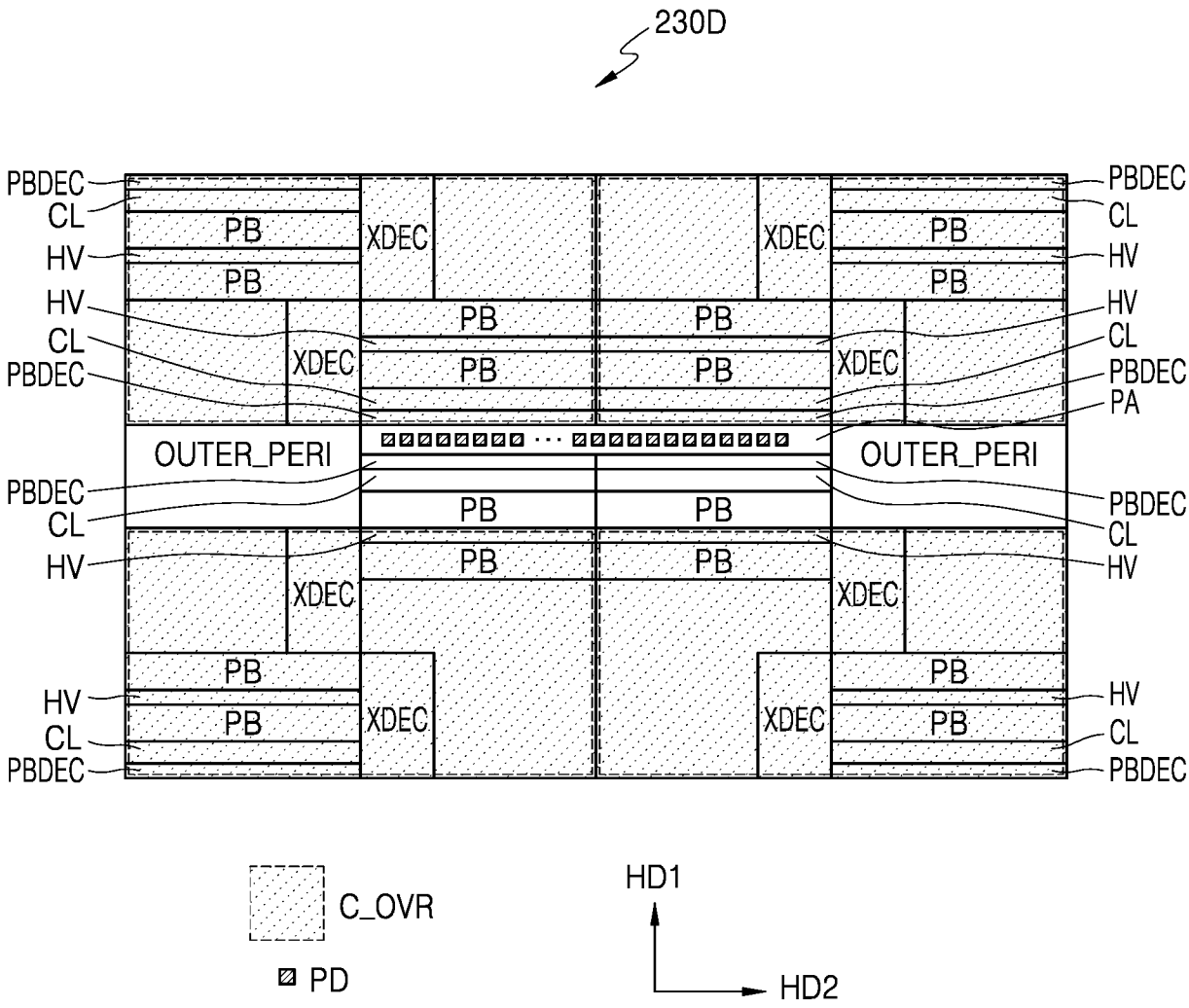


FIG. 24A

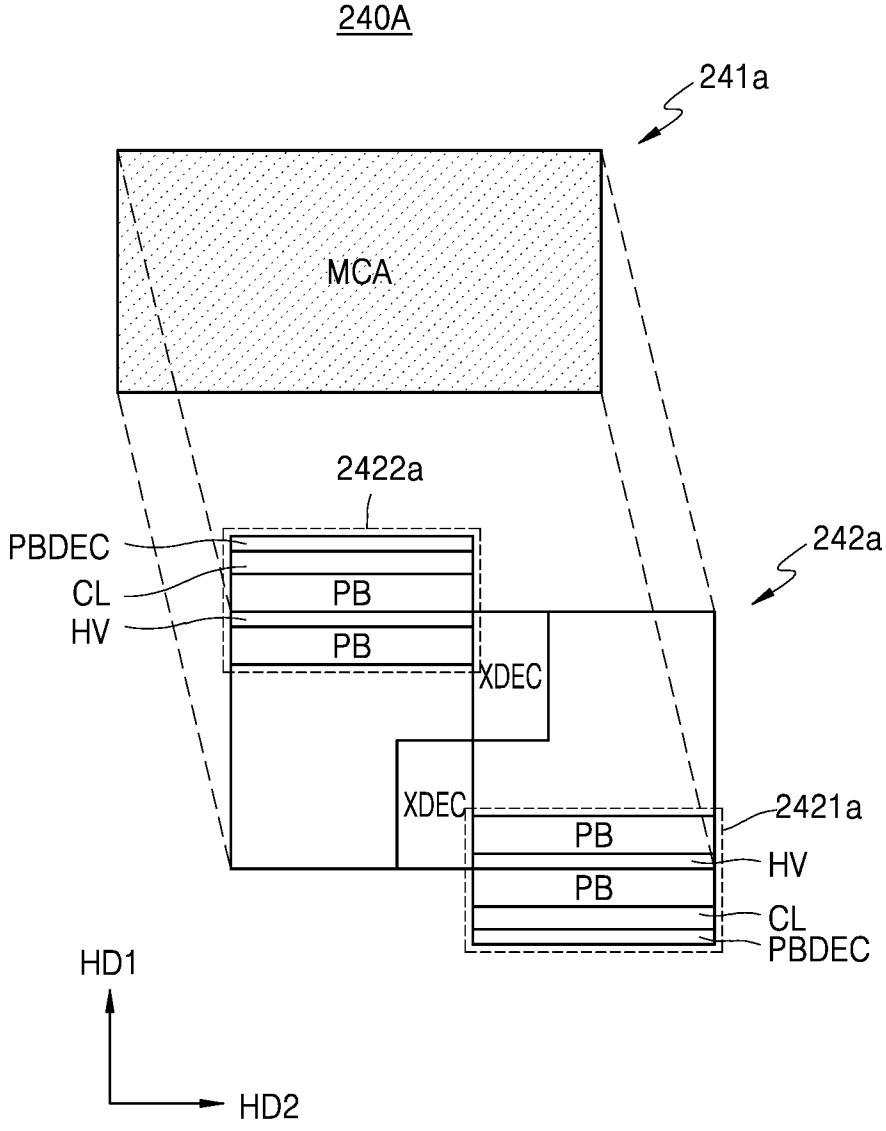

240A
241a
MCA
2422a
242a
PBDEC
CL
HV
PB
PB
XDEC
XDEC
2421a
PB
HV
PB
CL
PBDEC
HD1
HD2

FIG. 24B

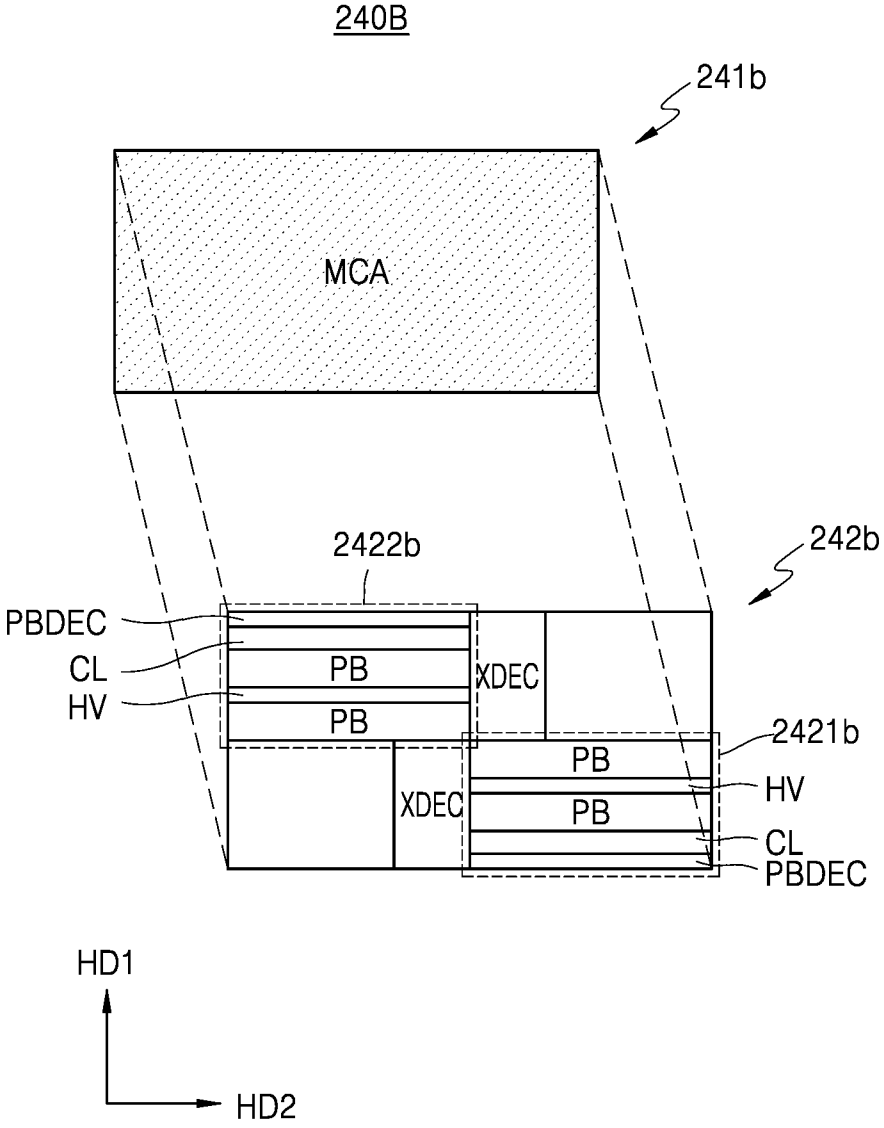

240B
241b
MCA
2422b
242b
PBDEC
CL
HV
PB
PB
XDEC
2421b
PB
HV
XDEC
PB
CL
PBDEC
HD1
HD2

FIG. 25A

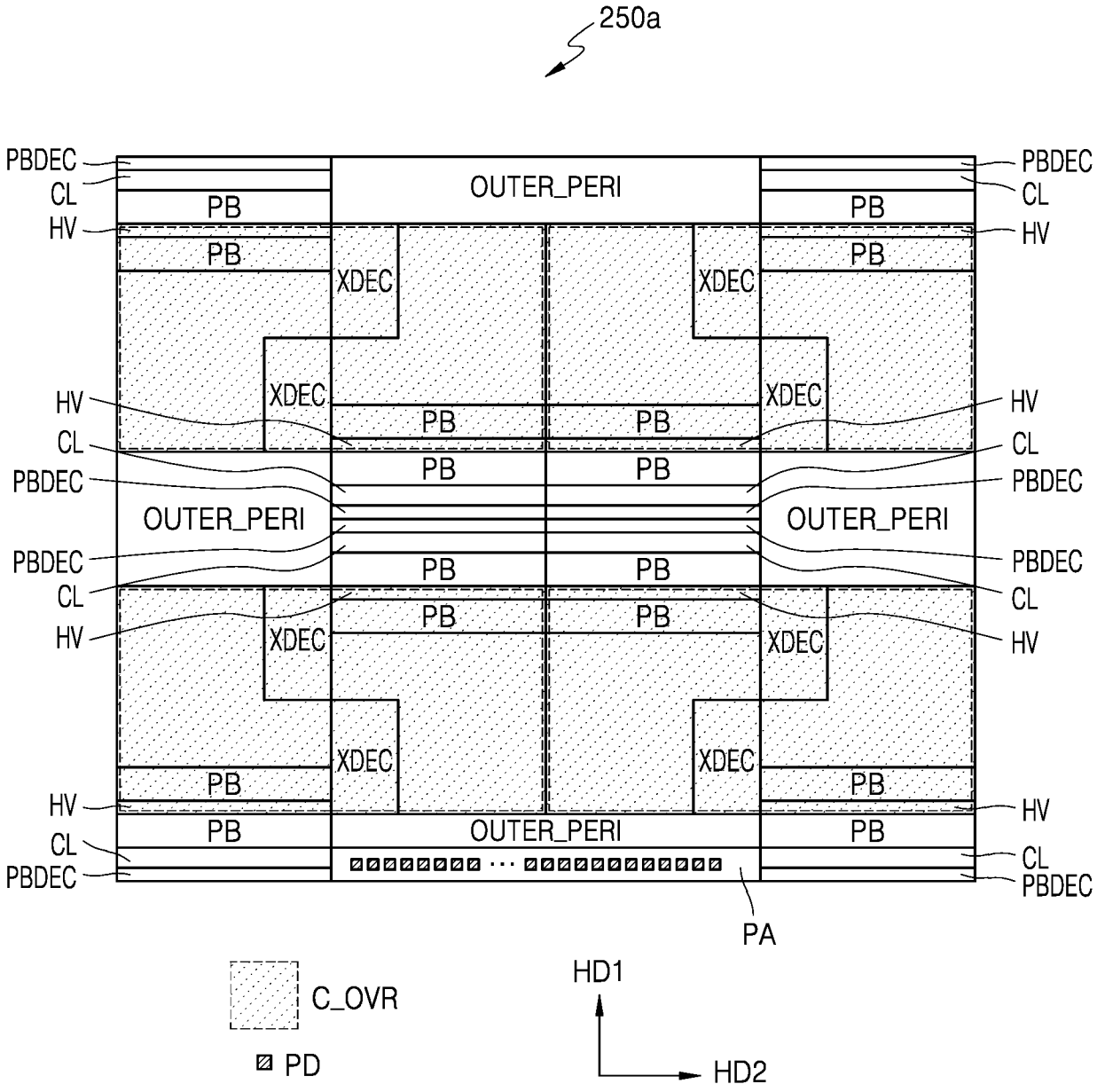


FIG. 25B

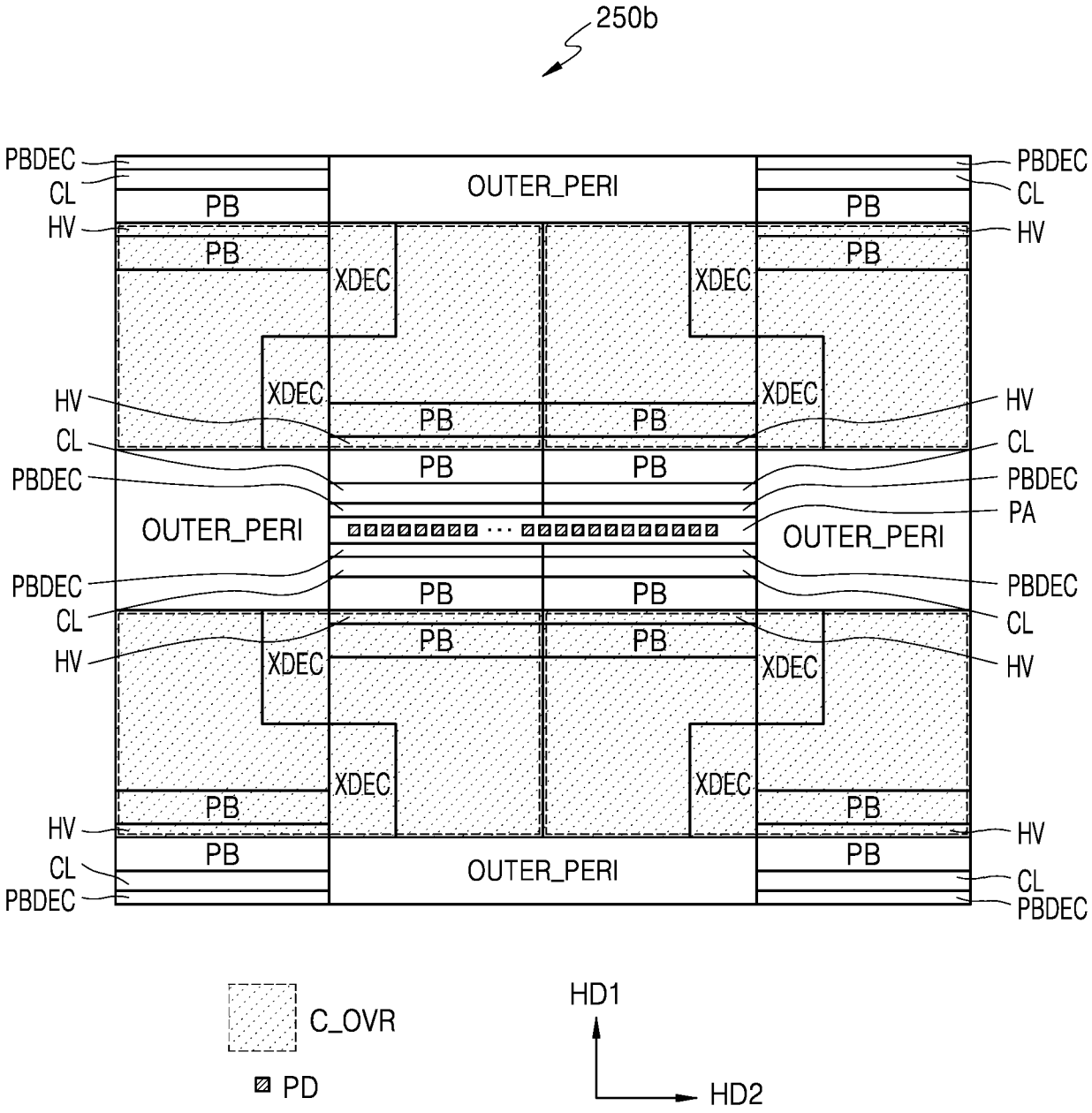


FIG. 25C

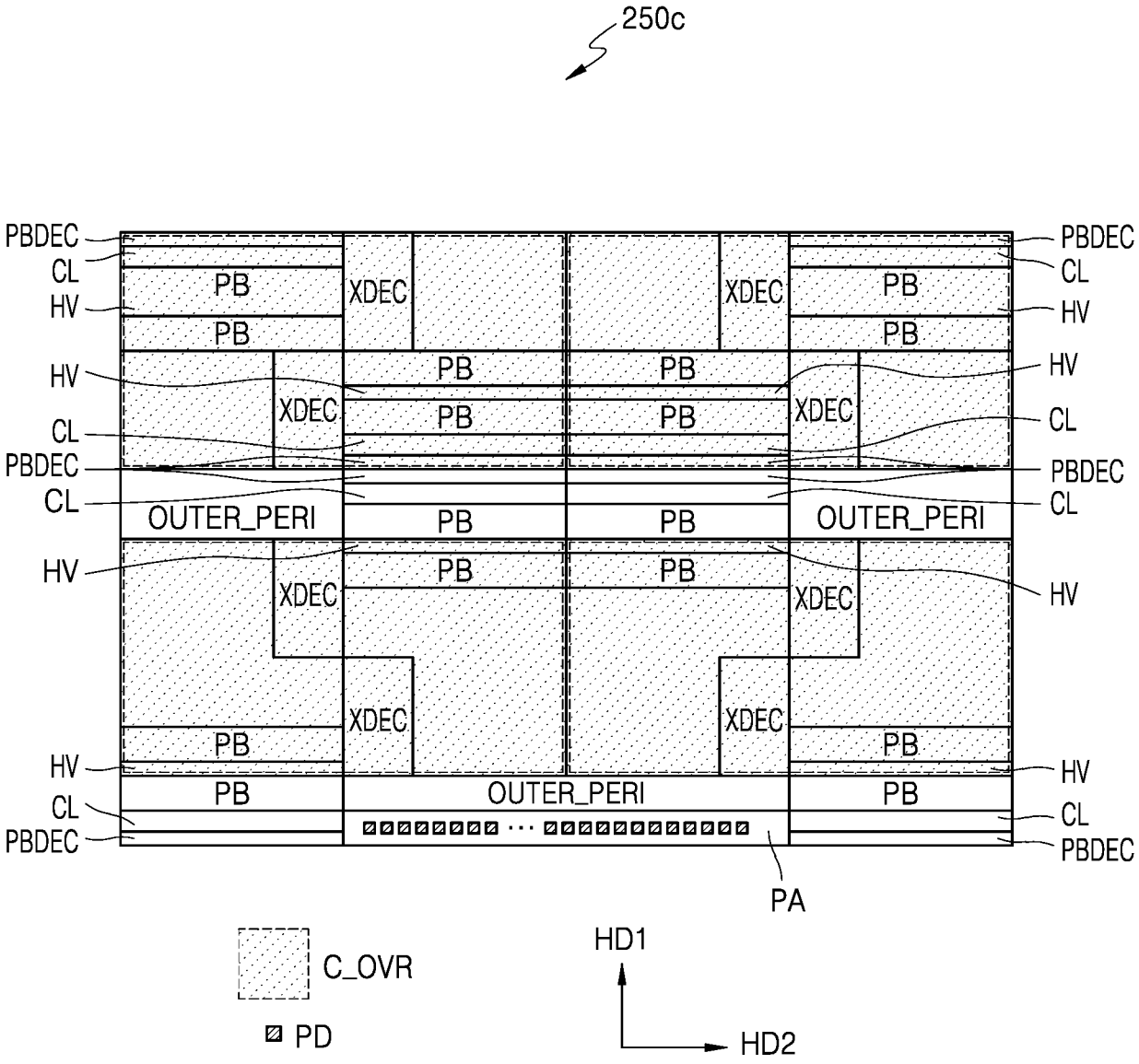


FIG. 25D

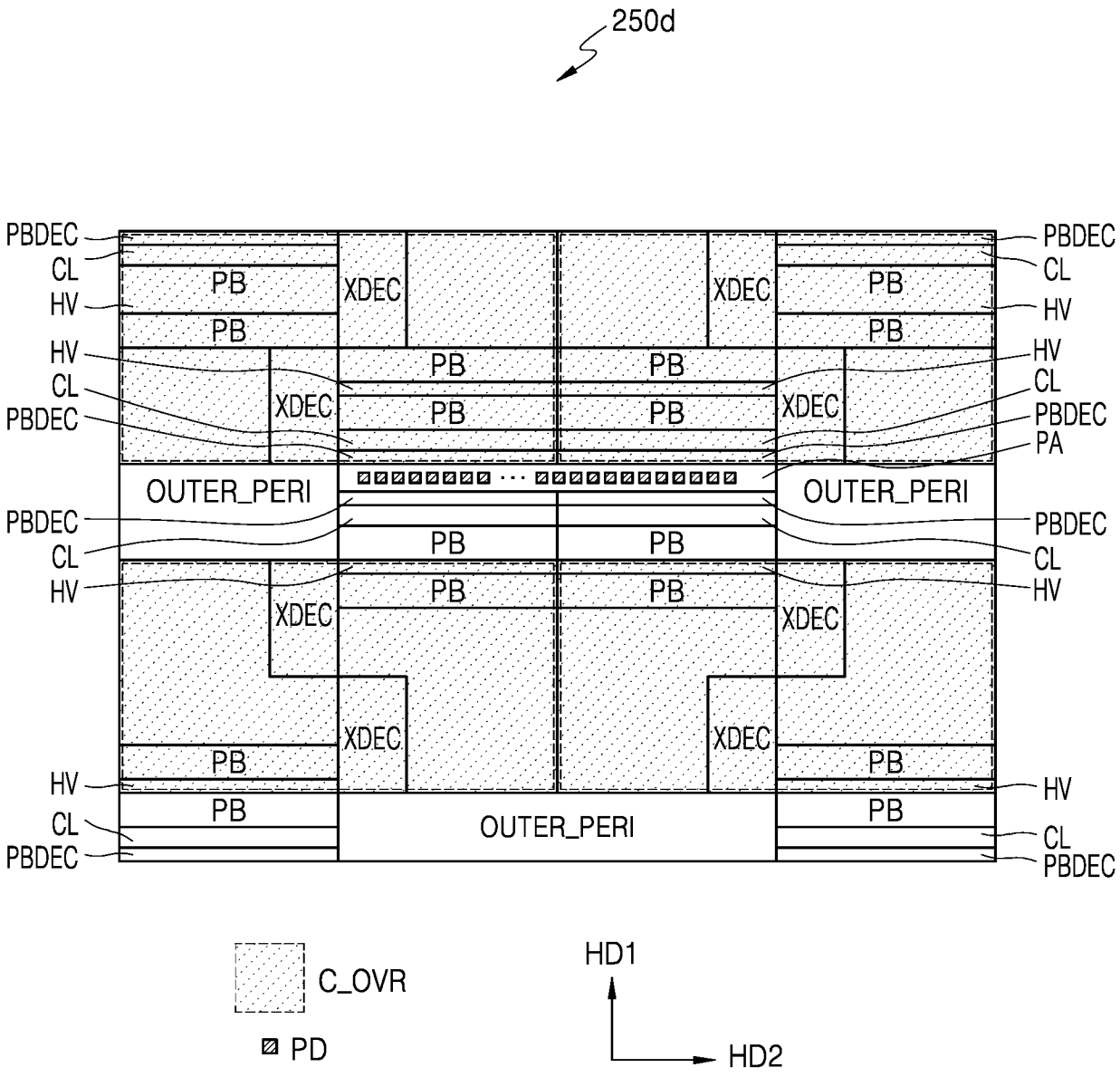


FIG. 26A

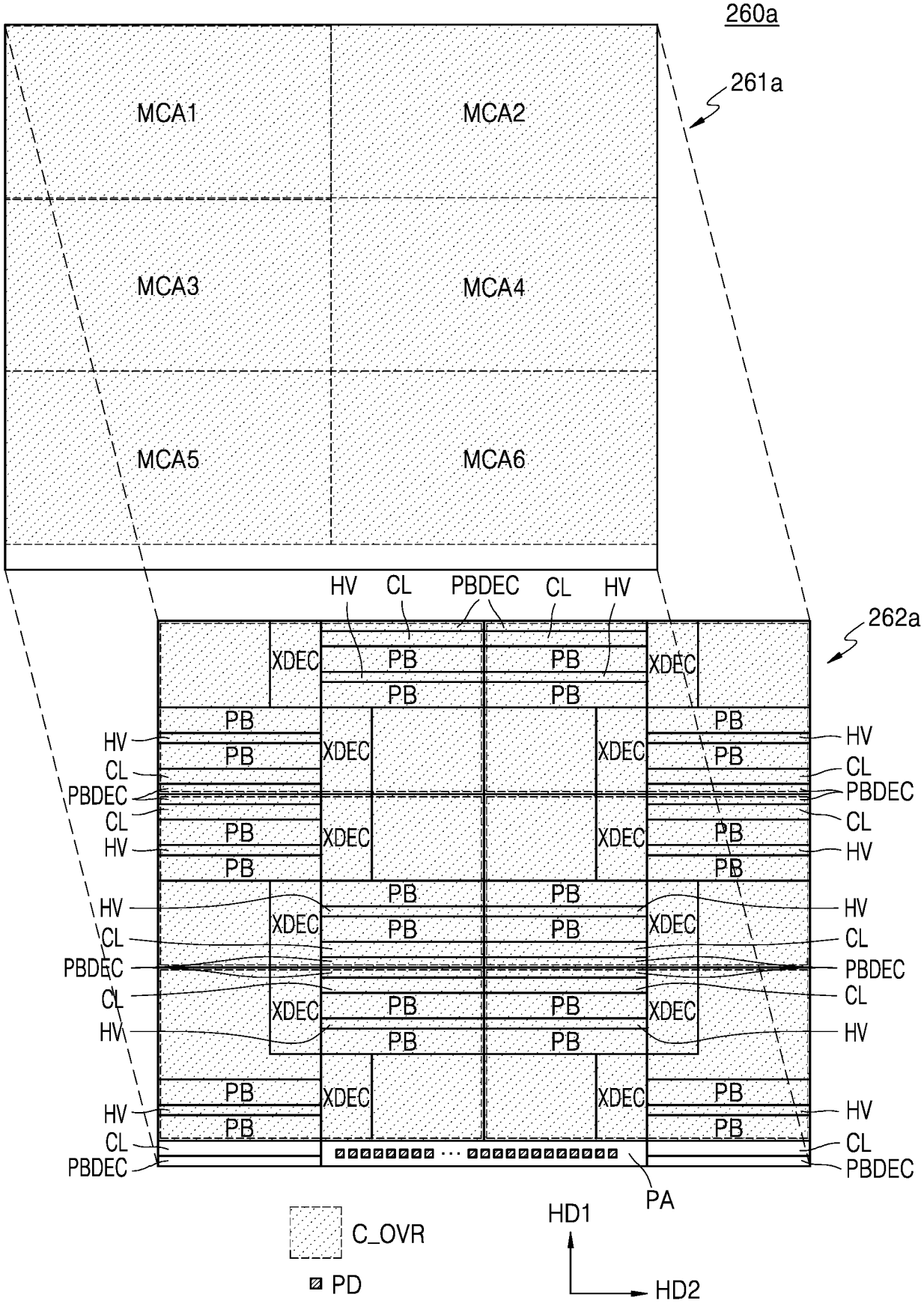

260a
261a
MCA1
MCA2
MCA3
MCA4
MCA5
MCA6
262a
HV
CL
PBDEC
CL
HV
XDEC
PB
PA
C_OVR
PD
HD1
HD2

FIG. 26B

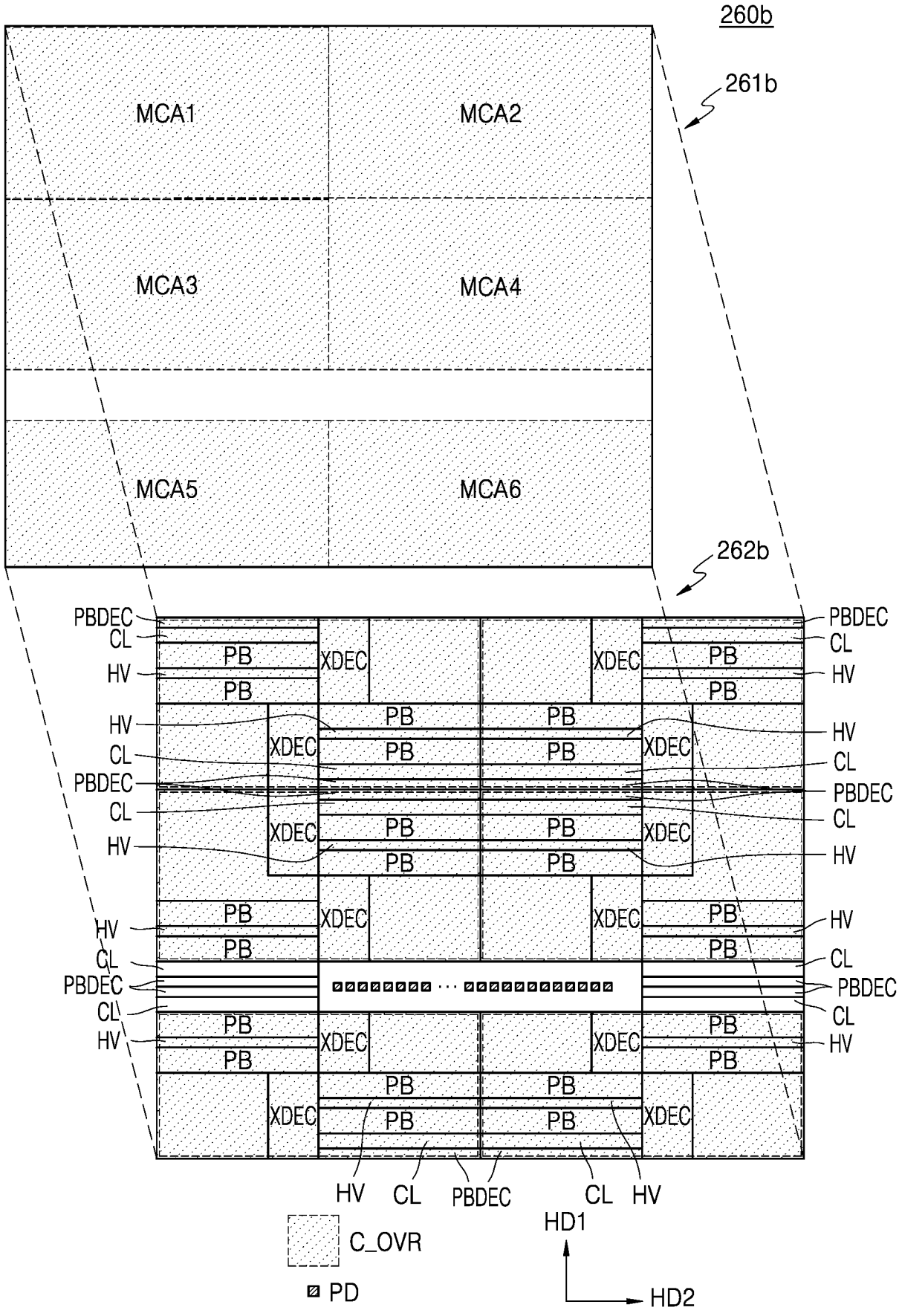
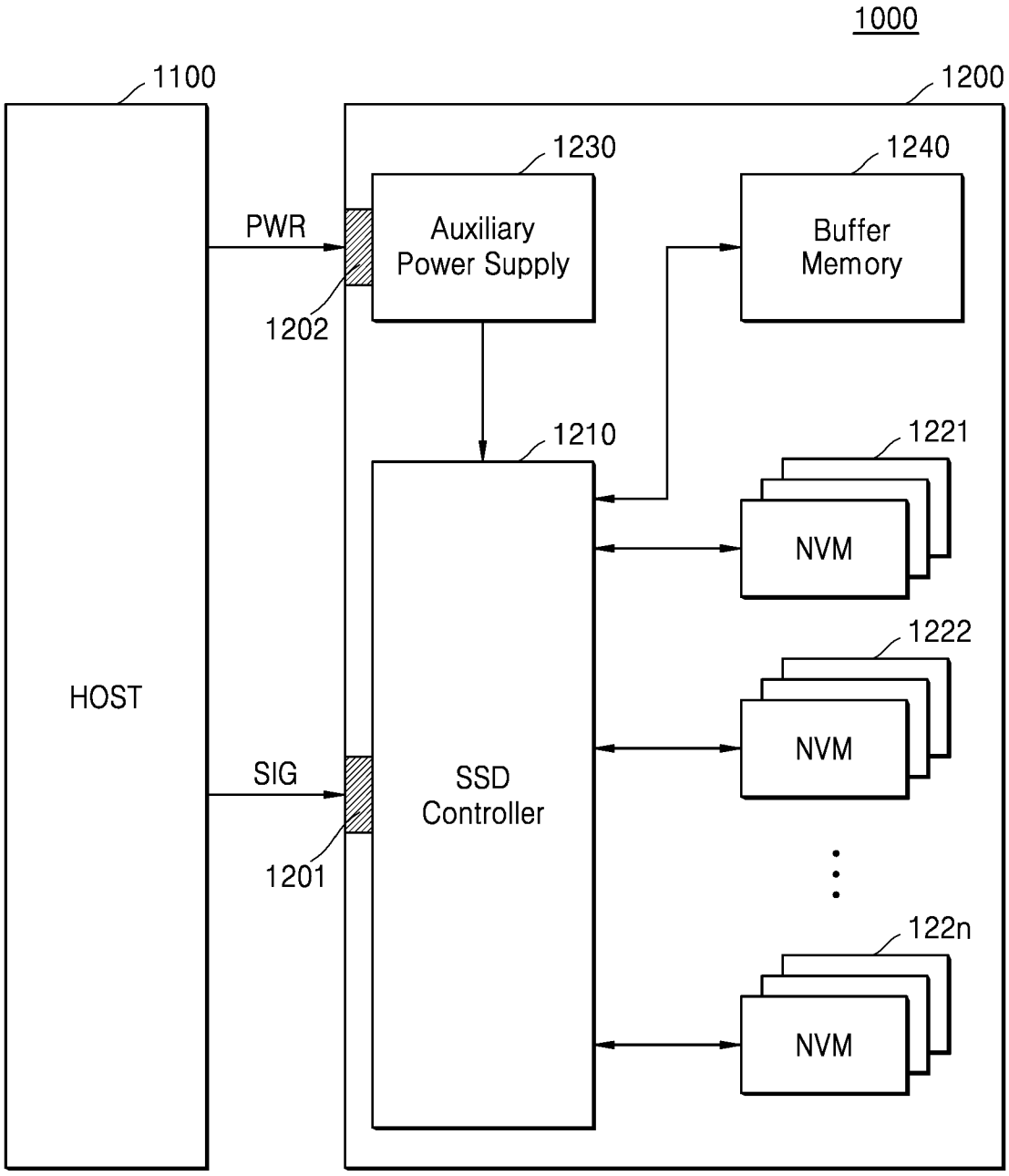

260b
261b
MCA1
MCA2
MCA3
MCA4
MCA5
MCA6
262b
PBDEC
CL
HV
PB
XDEC
C_OVR
PD
HD1
HD2

FIG. 27


1000
1100
1200
1230
1240
PWR
Auxiliary Power Supply
Buffer Memory
1202
1210
1221
NVM
1222
NVM
HOST
SIG
SSD Controller
1201
122n
NVM