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Specification

1. Title of the Invention:

Disk drive apparatus ✓

2. Detailed Description of the Invention:

[0001]

[Field of the invention]

The present invention relates to a disk drive apparatus that is employed in hard disk drives (HDDs), and more particularly to a disk drive apparatus where wiring is performed on a printed-circuit board by a head assembly mounted with a plurality of heads which perform recording/regeneration on a storage medium.

[0002]

[Background art]

Even further miniaturization has been required of an HDD that is employed as the external storage of an information processor. Particularly, a plurality of heads corresponding to a plurality of storage media are mounted on a head assembly, and there is a need to reduce the number of wires between the head assembly and the printed-circuit board.

[0003]

A conventional technique of this kind is described, for example, in IBM Technical Disclosure Bulletin, vol. 39, No. 7, July 1996, pp. 175-176.

[0004]

Figure 13 is a block diagram showing the constitution of the interface circuit of a conventional disk drive apparatus.

[0005]

In Figure 13, an HDD 10 is constituted by a hard disk controller (HDC) 11 for controlling an operation of reading or writing data from or to a magnetic disk, a microprocessing unit (MPU) 12 for controlling the entire operation of the HDD, a preamplifier 13 for performing reading/writing of data on a magnetic head, and a channel module 14 for controlling the preamplifier 13 by various control signals. The HDC 11 and the MPU 12 are constituted as digital systems.

[0006]

The channel module 14 consists of a channel module where a waveform shaping circuit, a phase-locked loop (PLL) circuit, a frequency synthesizer circuit, an encoder/decoder, etc., are made into a module. The channel module 14 converts a digital user data signal to a data write signal and also converts an analog signal from the preamplifier 13 to a digital signal.

[0007]

The channel module 14 is controlled by a read gate control signal, a write gate control signal, a servo gate control signal, a servo data control signal, an in-channel register control signal, and the other control signals connected in parallel. Also, control signals for the preamplifier 13, including some of the aforementioned control signals, are directly connected and controlled, theoretically including inversion, through circuits for noise reduction such as a filter and a buffer by a digital system. In addition, the channel module 14 performs the transmission of a data read/write signal between the digital system and the channel module through a data bus with a few bits.

[0008]

As signals that are input to or output from the preamplifier 13, there are head select signals HSEL0, HSEL1, and HSEL2, current write signals WCURR0 and WCURR1, a head control signal MRBIAS, a preamplifier-fault write signal AEWFAULT, a preamplifier characteristic control signal TA, a write gate signal WGT, and a power save read/write signal RWPS. The signals WGT and RWPS are input to the channel module 14.

[0009]

Also, the preamplifier 13 and the channel module 14 are connected by data write signals WDT+ and WDT- and analog-data read signals RDX and RDY.

[0010]

In addition, the MPU 12 and the channel module 14 are connected by a serial register control signal SENA, a serial clock signal SCLK, and a serial data signal SDT.

[0011]

Between the HDC 11 and the channel module 14, a data and servo switching signal SRVAREA, an AGC hold signal AGCHOLD, a clear signal CLEAR, a burst detection timing specifying signal BURSTW, a POR reset signal POR, a read gate signal RGT, and a clock signal OSC are input from the HDC 11 to the channel module 14, and a servo data signal SRVDT, a reference clock read signal RRCLK, a serial clock signal SRVSC, and a serial data signal SRVSD are input from the channel module 14 to the HDC 11. User data read/write signals NRZ0, NRZ1, NRZ2, NRZ3 are employed as bidirectional signals between the HDC 11 and the channel module 14.

[0012]

[Problems to be solved by the invention]

However, the interface circuit of a conventional disk drive apparatus such as this has the following problems.

[0013]

That is, since a great number of control signals exist between the HDC 11 and the MPU 12, there arises the problem that the number of pins is insufficient between the HDC 11 and the MPU 12. Particularly, in a disk drive apparatus of the next generation, there is a need to increase the number of the signals NRZ0 through NRZ3 (for example, the current 4 signals to 8 signals), so the number of pins is becoming very insufficient.

[0014]

In addition, in Figure 13, although the HDC 11, the MPU 12, and the channel module 14 have been directly connected with one another, in fact the preamplifier 13 is sensitive to noise and therefore if they are directly connected as shown, the error rate will be worse. For this reason, there is the problem that filters must be inserted or buffers having a common power supply must be interposed.

[0015]

Furthermore, where the data rate is becoming even faster, writing of data will not be able to be performed if the inductance of the wire of a head wire is large at the preamplifier. For this reason, the preamplifier is mounted near heads, and consequently, the distance between the preamplifier and the channels on a card will be longer and the preamplifier will easily be influenced by noise. In background art, as described above, since there are a great number of control signals, channels cannot be mounted on a flexible cable near to the preamplifier.

[0016]

The object of the present invention is to provide a disk drive which is capable of reducing a great number of control signals, reducing fabrication cost, and facilitating a measure to counter noise.

[0017]

[Summary of the invention]

A disk drive apparatus of the present invention comprises:

a head for reading or writing data from or to a storage medium;

an amplifier for amplifying data to the head;

a control unit for controlling an operation of reading out servo information for reading or writing data from or to the head; and

a channel for converting a digital data signal to a data write signal and also for converting an analog signal from the amplifier to a digital signal, the channel being controlled by the control unit; and

wherein the control unit performs control of the channel through a bus which transmits or receives a data read/write signal.

[0018]

A disk drive apparatus of the present invention comprises:

a head for reading or writing data from or to a storage medium;

an amplifier for amplifying data to the head;

a control unit for controlling an operation of reading out servo information for reading or writing data from or to the head; and

a channel for converting a digital data signal to a data write signal and also for converting an analog signal from the amplifier to a digital signal, the channel being controlled by the control unit; and

wherein:

a signal line for controlling the channel is replaced with control information;

the control information is transmitted through a bus which transmits or receives a data read/write signal; and

the channel performs control, based on the transmitted control information.

[0019]

The aforementioned disk drive apparatus may also be constructed so that when the channel is performing data communication, the control information is not transmitted. The aforementioned disk drive apparatus may also be constructed so that the control information transmitted through the bus is read out at predetermined bus-cycle intervals in correspondence with requested control.

[0020]

The aforementioned disk drive apparatus may also be constructed so that the channel generates a control signal which controls the amplifier, based on the control information.

[0021]

A circuit of the present invention is used in a storage. The circuit comprises an amplifier for amplifying a data read signal from a storage medium or a data write signal to the storage medium, a channel connected to the amplifier for making a conversion between an analog signal and a digital signal, a control unit for controlling an operation of reading or writing data from or to the storage medium, and a data signal line for transmitting a data signal between the channel and the control unit. The control unit controls the operation of reading or writing data from or to the storage medium, by controlling a signal on the data signal line.

[0022]

[Preferred embodiment]

A disk drive apparatus according to the present invention can be applied to a small HDD where wiring is performed on a printed-circuit board by a head assembly mounted with a plurality of heads which perform recording/regeneration on a storage medium.

[0023]

Figure 1 is a block diagram showing the constitution of a disk drive apparatus according to an embodiment of the present invention and is an example of the disk drive apparatus applied to a parallel arm electronics (AE) application. In the description of the disk drive apparatus according to this embodiment, the same reference numerals will be applied to the same parts and the same signals as the disk drive apparatus shown in Figure 13.

[0024]

In Figure 1 an HDD 100 is equipped with an HDC/MPU (control means) 101 where both an HDC for controlling an operation of reading or writing data from or to a magnetic disk and an MPU for controlling the entire operation of the HDD are constituted as a digital system in a single package. Furthermore, the HDD 100 is equipped with a preamplifier (amplification means) 102 for performing reading/writing of data on a magnetic head and a channel module (conversion means) 103 for making a conversion between a digital data stream and an analog signal and controlling the preamplifier 102.

[0025]

The channel module 103 consists of a channel module where a waveform shaping circuit, a phase-locked loop (PLL) circuit, a frequency synthesizer circuit, an encoder/decoder, etc., are made into a module. The channel module 103 converts a digital user data signal to a data write signal and also converts an analog signal from the preamplifier 102 to a digital signal.

[0026]

The channel module 103 performs the transmission of a data read/write signal between the digital system and the channel module through a data bus with a few bits and is constituted so that the status of the data bus is interpreted as control information on the channel module by a control signal CTRL, and according to the result of the interpretation as control information, the channel module is controlled. Also, control signals for the preamplifier 102 are directly connected and controlled, theoretically including inversion, through circuits for noise reduction such as a filter and a buffer by a digital system.

[0027]

As signals that are input and output between the preamplifier 102 and the channel module 103, there are data write signals WDT+ and WDT-, analog-data read signals RDX and RDY, head select signals HSEL0, HSEL1, and HSEL2, current write signals WCURR0 and WCURR1, a head control signal MRBIAS, a preamplifier-fault write signal AEWFault, a preamplifier characteristic control signal TA, a write gate signal WGT, and a power save read/write signal RWPS.

[0028]

Also, the HDC/MPU 101 and the channel module 103 are connected by a clock signal OSC, a control signal CTRL, a status signal STAT, a reference clock read signal RRCLK, and user data read/write signals NRZ0, NRZ1, NRZ2, NRZ3. The user data read/write signals NRZ0, NRZ1, NRZ2, NRZ3 have both a function as a data bus for transmitting and receiving a data read/write signal and a function as a bus (called an NRZ bus) for sending control information. This control information includes servo data transfer.

[0029]

Between the HDC/MPU 101 and the channel module 103, there is provided an additional control signal CTRL, which interprets the status of the data bus as the control information on the channel module. Also, where the channel module is performing data communication through the data bus, it is interpreted as an end of communication.

[0030]

That is, the HDC/MPU 101 and the channel module 103 are connected by the data bus and the minimum control signals other than that;

control signal CTRL, status signal STAT, and clock signals OSC and RRCLK. Control signals, such as various gate control signals, a servo data control signal, and an interior register control signal, have been omitted.

[0031]

In comparison with the aforementioned disk drive apparatus shown in Figure 13, the serial register control signal SENA, the serial clock signal SCLK, and the serial data signal SDT are omitted between the MPU 12 and the channel module 14. In addition, the data and servo switching signal SRVAREA, the AGC hold signal AGCHOLD, the clear signal CLEAR, the burst detection timing specifying signal BURSTW, the POR reset signal, and the read gate control signal RGT, which are signals that are output from the HDC 11 to the channel module 14, are omitted. Furthermore, the servo data signal SRVDT, the serial clock signal SRVSC, and the serial data signal SRVSD, which are signals that are output from the channel module 14 to the HDC 11, are entirely omitted. Thus, the number of signal lines and the number of pins between the digital system and the channel module have been reduced by approximately half.

[0032]

Note that the aforementioned status signal STAT is one where the concept of the servo data signal SRVDT is generalized and therefore is a similar signal as the servo data signal SRVDT.

[0033]

Figure 2 is a block diagram showing the constitution of a disk drive apparatus according to an embodiment of the present invention and is an example of the disk drive apparatus applied to a serial AE application. The same reference numerals will be

applied to the same parts and the same signals as the disk drive apparatus shown in Figure 1.

[0034]

In Figure 2, an HDD 200 is equipped with an HDC/MPU (control means) 101 where both a hard disk controller (HDC) for controlling an operation of reading or writing data from or to a magnetic disk and a MPU for controlling the entire operation of the HDD are constituted as a digital system in a single package. Furthermore, the HDD 200 is equipped with a preamplifier 201 for performing reading/writing of data on a magnetic head and a channel module 202 for making a conversion between a digital data stream and an analog signal and controlling the preamplifier 201.

[0035]

The channel module 202 performs the transmission of a data read/write signal between the digital system and the channel module through a data bus with a few bits and is constituted so that the status of the data bus is interpreted as control information on the channel module by a control signal CTRL, and according to the result of the interpretation as control information, the channel module is controlled.

[0036]

As signals that are input and output between the preamplifier 201 and the channel module 202, there are data write signals WDT+ and WDT-, analog-data read signals RDX and RDY, a preamplifier-fault write signal AEWFault, a write gate signal WGT, a power save read/write signal RWPS, a serial register control signal SENA, a serial clock signal SCLK, and a serial data signal SDT.

[0037]

Also, the HDC/MPU 101 and the channel module 202 is connected by a clock signal OSC, a control signal CTRL, a status signal STAT, a reference clock read signal RRCLK, and user data read/write signals NRZ0, NRZ1, NRZ2, NRZ3. The user data read/write signals NRZ0, NRZ1, NRZ2, NRZ3 have both a function as a data bus for transmitting and receiving a data read/write signal and a function as a bus (NRZ bus) for sending control information.

[0038]

Between the HDC/MPU 101 and the channel module 202, there is provided an additional control signal CTRL, which interprets the status of the data bus as the control information on the channel module. Also, where the channel module is performing data communication through the data bus, it is interpreted as an end of communication.

[0039]

That is, the HDC/MPU 101 and the channel module 202 are connected by the data bus and the minimum control signals other than that; control signal CTRL, status signal STAT, and clock signals OSC and RRCLK. Control signals, such as various gate control signals, a servo data control signal, and an interior register control signal, have been omitted.

[0040]

The operations of the HDD 100 and HDD 200 constructed as described above will hereinafter be described.

[0041]

A description will first be made of the basic concepts of the present invention.

[0042]

The present inventors have noticed a great number of control signals existing between the HDC, the MPU, and the channel module only instruct timings from the HDC and the MPU to the channel module, and furthermore, when reading or writing is being performed by the user data read/write signals NRZ0 through NRZ3, theoretically there is no possibility that these control signals are input or output. That is, control information can be sent with the signal lines of the user data read/write signals NRZ0 through NRZ3.

[0043]

Therefore, the present invention, in the hard disk drive, reduces the number of control signals by performing both the control of the channel module performing conversion between a digital data stream and an analog signal and the control of the preamplifier through the bus which transmits or receives a data read/write signal. In addition, a signal for controlling the preamplifier sensitive to noise is generated in the channel module by controlling the aforementioned bus, and noise influence is removed by connecting the generated control signal from the digital system (HDC and MPU) directly to the preamplifier.

[0044]

Now, the operation of the disk drive apparatus will be described in detail based on the aforementioned basic concepts. Since the

HDD 100 and the HDD 200 are the same in operation, a description will be made of the HDD 100.

[0045]

A control signal CTRL is provided between the HDC/MPU 101 and the channel module 103, and the status of the data bus is interpreted as control information on the channel module 103 by this control signal CTRL. Also, where the channel module 103 is performing data communication through the data bus, it is interpreted as an end of communication.

[0046]

The read, write, and servo controls, which require time precision, are interpreted in the status of a bus with a short cycle (for example, one cycle for a 4-bit bus or more), and the control of a register or the control of a preamplifier which can take a long time is interpreted in the status of a bus with a long cycle. A control signal to the preamplifier 102 requiring time precision, such as a write gate control signal, is also generated in the channel module 103, based on control information transmitted to the channel module 103 through a data bus. In addition to this, when errors during read and write operations are supposed, a predetermined status signal STAT is output from the channel module 103 to the HDC/MPU 101 which is a digital system.

[0047]

The control signal of the preamplifier 102 is generated in the channel module 103, based on the control signal to the channel module 103. Also, the preamplifier has a serial interface.

[0048]

Figure 3 is a timing chart showing a control timing example. Figure 3(A) shows the conventional example of Figure 13, and Figure 3(B) a method according to this embodiment in comparison with the conventional example.

[0049]

In the conventional example, the channel module 14 and the digital system are controlled by a read gate control signal, a write gate control signal, a servo gate control signal, a servo data control signal, an in-channel register control signal, and the other control signals connected in parallel, and the respective control signals are output, for example, as shown in Figure 3(A).

[0050]

On the other hand, in this method, as shown in Figure 3(B), a control signal to the channel module is given as control information by the values of the buses NRZ0 through NRZ3 when the control signal CTRL is at a high level (CTRL signal is at an active level). Now, the NRZ values (0 through F) that are transmitted by the buses NRZ0 through NRZ3 are caused to correspond to the control information with meanings shown in Figure 3(B). This causes data to be transmitted through the data buses NRZ0 through NRZ3 when the control signal CTRL is at a low level and also causes control information to be transmitted onto the same data buses NRZ0 through NRZ3 when the control signal CTRL is at a high level.

[0051]

For example, at timing shown by (a) in Figure 3(B), control information (4) meaning a servo area start control signal (see "SRVAREA" in Figure 3(A)) is transmitted, and at timing shown by (b) in Figure 3(B), control information (7) meaning an AGC hold control signal (see "AGCHOLD" in Figure 3(A)) is transmitted.

[0052]

In Figure 3(B), when the control signal CTRL is at an active level, the "1" on the NRZ bus means the start of a read operation, and the data on the NRZ thereafter means a data read signal from the channel module. When the control signal CTRL goes to the next active level, the read operation is ended. In this embodiment, while the control signal CTRL has been provided for interpreting the state of the data bus as control information to the channel module 103, data itself may also be interpreted without providing the control signal CTRL. Also, although the control signal has been synchronized with the reference read clock RRCLK, this is merely an example and therefore the timing may also be another synchronous timing or asynchronous timing.

[0053]

Figures 4 through 12 are timing charts showing an actual control timing example in the HDD 100. In the figures a part enclosed by a solid line indicates the aforementioned control information.

[0054]

Figure 4 is a diagram showing the command on the NRZ bus and the timing and showing the relationship between the NRZ value and the command. The relationship between the NRZ value and the command is partially different from that shown in Figure 3.

[0055]

Figures 5 through 9 are diagrams showing a command timing example in a different case. Figure 5 is a diagram showing the read timing to a servo area in a normal case, Figure 6 a diagram showing the read timing to a servo area in an abnormal case, Figure 7 a diagram showing the write timing to a servo area in a normal case, Figure 8 a diagram showing the write timing to a servo area in an abnormal case, and Figure 9 a diagram showing the conventional method and this method in comparison with each other.

[0056]

Figure 10 is a diagram for explaining burst data transmission, and the start of a burst area and the end of a servo area are shown according to conditions shown.

[0057]

Figure 11 is a timing chart showing a command mode (RRCLK stop mode) and the return thereof. The command mode is set so as to satisfy the control conditions shown in Figure 11.

[0058]

Figure 12 is a timing chart showing register access timing, and read and write operations by a 4-bit bus and a 8-bit bus are performed according to conditions shown.

[0059]

As has been described above, the HDD 100 according to this embodiment is equipped with the HDC/MPU 101 for controlling an operation of reading or writing data from or to a magnetic head,

the preamplifier 102 for amplifying the data from the magnetic head, and the channel module 202 controlled by the HDC/MPU 101. The channel module 202 converts a digital data signal to a data write signal and also converts an analog signal from the preamplifier 102 to a digital signal. A signal line for controlling the channel module 202 is replaced with control information, and the control information is transmitted through the NRZ bus which transmits or receives a data signal for reading or writing. The channel module 202 performs control, based on the transmitted control information. Therefore, a great number of control signals to an analog system can be reduced and cost reduction is achievable.

[0060]

Also, if the control of the preamplifier 102 which is easily influenced by noise is performed through the channel module 202, a noise countermeasure can easily be made.

[0061]

In addition, since the signals which are transmitted between an analog system and a digital system can be considerably reduced and controlled through a flexible cable connector with about 20 pins, it becomes possible to mount not only a preamplifier but also a channel module on a flexible cable.

[0062]

In this embodiment, while the present invention has been applied to an HDD, it is not limited to this but it is applicable to any drive if it is equipped with control means for controlling an operation of reading or writing data from or to the aforementioned head. For example, the present invention may also be employed in an external storage other than HDDs, such as an

magneto-optical disk data storage, and similar advantages as the aforementioned embodiment are obtainable.

[0063]

Also, in this embodiment, although the NRZ bus has transmitted 4-bit or 8-bit data, it may also take any form if it transmits control information through a bus which transmits or receives a data signal for reading or writing. In addition, the corresponding relationship between the NRZ value and the command or the relationship between the bus cycle and the read timing may also be of any relationship.

[0064]

Furthermore, it is a matter of course that the type and number of the HDC, the preamplifier, and the channel module constituting the aforementioned disk drive apparatus are not limited to the aforementioned embodiment.

[0065]

[Advantages of the invention]

In the disk drive apparatus according to the present invention, a signal line controls conversion means which converts a digital data signal to a data write signal and also converts an analog signal from amplification means to a digital signal, and the signal line is replaced with control information. The control information is transmitted through a bus which transmits or receives a data read/write signal, and the conversion means performs control, based on the transmitted control information. Therefore, a great number of control signals to an analog system can be reduced and cost reduction is achievable. Furthermore, a noise countermeasure can easily be made.

[0066]

Moreover, it becomes possible to mount not only a preamplifier but also a channel module on a flexible cable.

3. Brief Description of the Drawings:

Figure 1 is a block diagram showing the constitution of a disk drive apparatus according to an embodiment of the present invention;

Figure 2 is a block diagram showing the constitution of the aforementioned disk drive apparatus;

Figure 3 is a timing chart showing the control timing example of the aforementioned disk drive apparatus;

Figure 4' is a timing chart showing the command on the NRZ bus of the aforementioned disk drive apparatus and the command timing and also showing the relationship between the NRZ value and the command;

Figure 5 is a timing chart showing a command timing example of the read timing to a servo area in a normal case of the aforementioned disk drive apparatus;

Figure 6 is a timing chart showing a command timing example of the read timing to a servo area in an abnormal case of the aforementioned disk drive apparatus;

Figure 7 is a timing chart showing a command timing example of the write timing to a servo area in a normal case of the aforementioned disk drive apparatus;

Figure 8 is a timing chart showing a command timing example of the write timing to a servo area in an abnormal case of the aforementioned disk drive apparatus;

Figure 9 is a diagram showing the servo areas of a conventional method and this method of the aforementioned disk drive apparatus in comparison with each other;

Figure 10 is a timing chart for explaining the burst data transmission of the aforementioned disk drive apparatus;

Figure 11 is a timing chart showing the command and the command return of the aforementioned disk drive apparatus;

Figure 12 is a timing chart showing the register access timing of the aforementioned disk drive apparatus; and

Figure 13 is a block diagram showing the constitution of a conventional disk drive apparatus.

[Description of symbols]

100, 200 ... Magnetic disk unit (disk drive apparatus)
101 ... HDC/MPU (control means)
102, 201 ... Preamplifier (amplification means)
103, 202 ... Channel module (conversion means)
NRZ ... Bus



4. Claims:

(1) A disk drive apparatus comprising:

a head for reading or writing data from or to a storage medium;

an amplifier for amplifying data which is read or written through said head;

a control unit for controlling an operation of reading out servo information for reading or writing data through said head;

a channel for converting a digital data signal to a data write signal and also for converting an analog signal from said amplifier to a digital signal, the channel being controlled by said control unit; and

a bus which transmits or receives a data read/write signal, said control unit performing the control of said channel through said bus.

(2) A disk drive apparatus comprising:

a head for reading or writing data from or to a storage medium;

an amplifier for amplifying data which is read or written through said head;



a control unit for controlling an operation of reading out servo information for reading or writing data through said head;

a channel for converting a digital data signal to a data write signal and also for converting an analog signal from said amplifier to a digital signal, the channel being controlled by said control unit; and

a signal line which is able to be replaced with control information for controlling said channel;

whereby said control information is transmitted through a bus which transmits or receives a data read/write signal and said channel performs control, based on the transmitted control information.

- (3) The disk drive apparatus as set forth in Claim 1 or 2, wherein, when said channel is performing data communication, said control information is not transmitted.
- (4) The disk drive apparatus as set forth in Claim 1 or 2, wherein said control information transmitted through said bus is read out at predetermined bus-cycle intervals in correspondence with requested control.
- (5) The disk drive apparatus as set forth in Claim 1 or 2, wherein said channel generates a control signal which controls said amplifier, based on said control information.
- (6) A circuit for use in a storage apparatus, comprising:



an amplifier for amplifying a data read signal from a storage medium or a data write signal to said storage medium;

a channel connected to said amplifier for making a conversion between an analog signal and a digital signal;

a control unit for controlling an operation of reading or writing data from or to said storage medium; and

a data signal line for transmitting a data signal between said channel and said control unit;

whereby said control unit controls the operation of reading or writing data from or to said storage medium, by controlling a signal on said data signal line.