METHOD AND DEVICE TO INCREASE LATCH-UP IMMUNITY IN CMOS DEVICES

ABSTRACT

The preferred embodiment of the present invention overcomes the limitations of the prior art and provides a device and method to increase the latch-up immunity of CMOS devices by reducing the mobility of carriers between the devices. The preferred embodiment uses an implant (106) formed beneath trench isolation between n-channel (602, 604, 606, 608) and p-channel (612, 614, 616, 618) devices. This implant preferably comprises relatively large/heavy elements implanted into the wafer beneath the trench isolation. The implant elements reduce the mobility of the charge carriers. This increases the latch-up holding voltage and thus reduces the likelihood of latch-up. The implants can be formed without the need for additional photolithography masks.

Fig. 6

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